A Highly Efficient AC-PDP Driver Featuring an Energy Recovery Function in Sustaining Mode Operation

Feel-Soon Kang, Sung-Jun Park and Cheul-U Kim

Abstract - A simple sustain driver employing an energy recovery function is proposed as a highly efficient driver of a plasma display panel. The proposed driver uses dual resonance in the sustaining mode operation: a main resonance between an inductor and an external capacitor to produce alternative pulses and a sub-resonance between an inductor and a panel to recover the energy consumption by the capacitive displacement current of the PDP. The operational principle and design procedure of the proposed circuit are presented with theoretical analysis. The operation of the proposed sustain driver is verified through simulation and experiments based on a 7.5-inch-diagonal panel with a 200 kHz operating frequency.
Key words - plasma display panel, sustain driver, energy recovery

1. Introduction

In the display industry, a PDP is considered to be best for manufacturing a wide, flat HDTV. Its advantages include such as ease of producing large panels, rapid response, long lifetime, thinness, wide viewing angle, enhanced memory capability, brightness, and luminous efficiency. PDPs can also retain pixels in the on state without continuous refresh signals, which means that increased brightness can be obtained for the same power and driving circuitry. This advantage also allows for excellent contrast ratios in high ambient illumination. Thanks to these attracting merits, the PDP will likely soon become consumer affordable wall-hanging color TVs with large diagonals [1]-[5].

As shown in Fig. 1, the PDP generally consists of front and rear glass plates with chemically stable rare gases between them. The inner space of the PDP is divided into numerous local cells by the opaque electrode grid lines encrusted on the inner surfaces of glass plates. Like that of fluorescent lamps, the operating principle for each cell is to make use of a gas-discharging-generated ultraviolet ray to excite a visible ray emitting phosphor. However, power consumption is increased due to the low efficiency of the UV generation process. Compared to the well-known discharge lamps with a high lumen efficacy, the loss due to wall recombination of the electrons and ions in a small cell makes the discharge less efficient.

In PDP drivers, frequent discharges occur by alternatively charging each side of the panel to a critical voltage, which causes repeated gas discharges. By means of an address driver, if a pixel has been in the controlled ON state, the sustain driver will maintain the ON condition of that pixel by repeatedly discharging. On the other hand, if a pixel has been driven to OFF state, voltage across the cell is never high enough to cause a discharge and the cell remains OFF. Because the address electrodes are only used during the writing or erasing periods and are normally connected to ground during a sustain mode, the capacitance C_p can be replaced by the equivalent circuit of the PDP as shown in Fig. 2 [5]-[8].

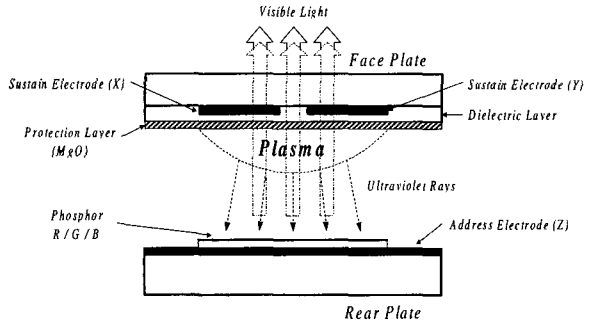

Fig. 1 Illustration of the lighting mechanism for one individual cell of AC-PDP

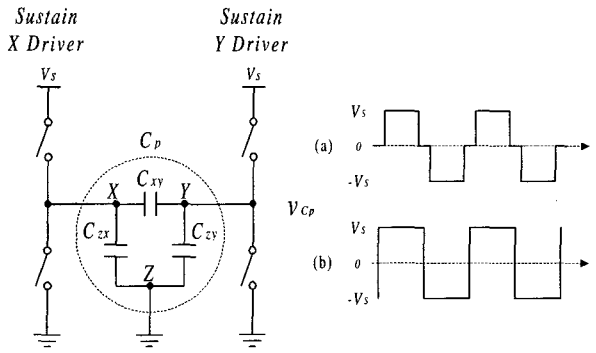

Fig. 2 Equivalent circuit of PDP with its simple driver and waveforms

The authors wish to thank the research engineers of LG PDP Electronics, Inc., in Gumi, Korea for their helpful comments and support.

Manuscript received: Feb. 5, 2002 accepted: July 18, 2002

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During charging and discharging transients, if an inductor is placed in series or parallel with the panel, then C_p can be charged and discharged by means of the inductor. Ideally, there is no power consumption since the inductor would store all of the energy otherwise lost in the non-ideal resistance and transfer it to or from C_p. However, to control the energy flow to and from the inductor when C_p is charged and discharged, switching devices are essential. In this case, the drive circuit can probably be replaced by a resistive factor, and therefore, is comprised of an RC series circuit. When V_S is supplied, the circuit equation can be expressed as

$$V_S = R \cdot i(t) + \frac{1}{C_p}\int i(t) \cdot dt \cdot \quad (1)$$

where the initial condition $V_{Cp}(t = 0) = 0$ and where V_S is the supply voltage; R is total resistance in the circuit, i.e., wire and electrodes resistance, on-resistance of switches, etc.; and C_p is the total capacitance in the PDP.

Rewriting Eq. (1),

$$\frac{di(t)}{dt} = -\frac{i(t)}{RC_P} \cdot \quad (2)$$

From Eq. (2) with the initial condition, the current equation can be obtained as

$$i(t) = \frac{V_S}{R}\exp(-\frac{1}{RC_p} \cdot t) \cdot \quad (3)$$

Therefore, power consumption (P_{loss}) in the circuit can be calculated as

$$P_{loss} = R \cdot i(t)^2 = \frac{V_S^{\,2}}{R}\exp(-\frac{2}{RC_p} \cdot t) \cdot \quad (4)$$

Assuming time constant is sufficiently smaller than unit pulse period, power consumption in a resistive factor can be expressed as

$$\int_0^\infty R \cdot i(t)^2 dt = \frac{1}{2} C_P V_S^2 \cdot \quad (5)$$

From Eq. (5), during charging and discharging transients, when the waveform (a) in Fig. 2 is applied to the PDP, power consumption is $2fC_pV_s^2$ for each cycle. In the case of waveform (b), $4fC_pV_s^2$ is consumed for a complete sustain cycle. It is, moreover, proportional to the operating frequency. In usual driver circuits, the energy is almost dissipated in the non-ideal resistance of the wire and electrode and in the on-resistance of the power MOSFETs.

Recently, to solve the power consumption problem, several AC-PDP sustain drivers employing an energy recovery function have been proposed [7]-[10]. Among them, three prior approaches are investgated and compared with the proposed driver. First, a conventional sustain driver was proposed in [7] and is shown in Fig. 7(a) with its control signals for simulation. This circuit basically utilizes the resonance between an external inductor and capacitance of the panel. Although this circuit can save a large amount of energy, it has a complex configuration that results in a high cost. Secondly, a regenerative circuit based on the full-bridge converter has been presented in [8]. Its configuration with its control signals is illustrated in Fig. 7(b). A remarkable point of this driver is a simpler structure than conventional drivers. During charging and discharging transients, this sustain driver directly recovers the energy from the panel via external inductors, and hence it saves a large amount of energy due to soft-transition of switches and diodes. Nevertheless, to form a zero level, current might be continuously flowed through the inductor and power MOSFETs during the reset or address periods. The continuously flowing current via power MOSFETs causes an increase in the energy loss because of their on-resistance; therefore, no energy is saved during those periods. Finally, as shown in Fig. 7(c), a novel energy recovery sustain driver using the parallel resonance is presented [9]. The parallel resonance between the inductor and the intrinsic capacitance of the panel can recover the energy lost by the capacitive displacement current of the PDP. Even though the parallel resonance saves a large amount of energy thanks to zero-voltage switching of switches and diodes, it is still complex, moreover, a complete soft-transition is uncertainly to overall periods because the total capacitance of panel is always changing according to the pixel conditions.

In this paper, an effective sustain driver for an AC-PDP is presented and compared with the conventional circuit. It has a simple structure compared with the conventional approaches. The most outstanding characteristic of proposed driver is its use of dual resonance, which results in high recovery efficiency. The operational principle and design procedure of proposed circuit are explained with theoretical analysis. Then, the validity of the proposed sustain driver is verified through the simulated and experimental results based on a 7.5-inch-diagonal panel with a 200 kHz operating frequency.

2. Proposed sustain driver

2.1 Circuit Configuration

Fig. 3 shows the configuration of the proposed sustain circuit for driving the AC-PDP. It consists of one inductor paralleled with a panel, the diode D_A to form a main resonant path, and four switches equipped with their internal diodes (S_2, S_4) and without others (S_A, S_1, S_3), respectively. The inductor paralleled with the panel resonates with the external capacitor. In a full-bridge structure, a sufficient dead time must be given to protect pole-switches from an arm-short. This time is used for the sub-resonance of the proposed sustain driver, i.e., during a dead-time the stored energy in

the inductor is transferred to the parallel connected panel in a resonant manner, changing the voltage polarity. As a result, the displacement and discharging current of the panel is directly recovered to the inductor, and then the recovered energy in the inductor is retransferred to the external capacitor through the diode D_1 or D_3 in resonantly when switches are turned on again, i.e., the main resonance. Main resonance occurs prior to sub-resonance in order to change the polarity of voltage across the panel repeatedly. It produces alternative pulses for charging and discharging the equivalent capacitance of the panel.

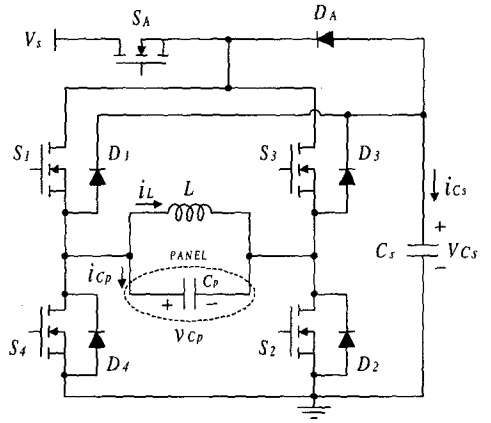


Fig. 3 Proposed sustain driver

2.2 Operational Principle

To simplify the circuit analysis, we ignore the effect of discharging the current and assume the value of C_P is constant. All components are ideal, and electrode resistance is neglected. Fig. 4 shows the operational waveforms of the proposed sustain driver. Because the left-side and right-side drivers show the same operation, we only consider a half cycle.

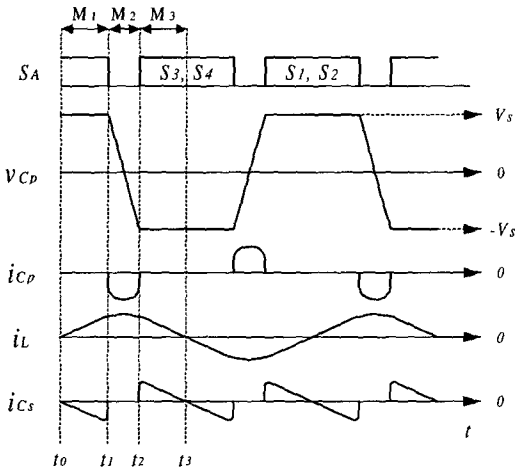


Fig. 4 Operational waveform

Mode 1 (t_0 - t_1)

Before t_0, S_1, S_2, and S_A are conducting and S_3 and S_4 are in a turned-off state; therefore, voltage across the panel v_{Cp} equals V_S is voltage across the external capacitor v_{Cs} is assumed as V_{Csm}. At t_0, the inductor starts to resonate with the external capacitor; hence, the stored energy in the external capacitor is transferred to the inductor via D_A, S_1, L, and S_2, shown as bolded lines in Fig. 5(a). In this mode, the inductor current can be written as

$$i_L(t) = V_{Csm} \cdot \sqrt{\frac{C_S}{L}} \cdot \sin \omega_m (t - t_0) \tag{6}$$

where $\omega_m = \frac{1}{\sqrt{LC_S}}$, $i_L(0) = 0$, and $v_{Cs}(0) = V_{Csm}$.

Voltage across the external capacitor can be derived as

$$v_{Cs}(t) = V_{Csm}[1 - \cos \omega_m (t - t_0)] \tag{7}$$

Mode 2 (t_1 - t_2): Before t_1, voltage across the panel is maintained as V_S by means of S_A conducting and the external capacitor voltage becomes V_S with the complete resonance. At t_1, S_1 and S_2 are turned off at the same time, resulting in the instantaneous blocking of the main resonant path. Consequently, the inductor current will flow through the panel resonantly as shown in Fig. 5(b). With initial condition, the circuit equation can be expressed as

$$i_L(t) = V_s \cdot \sqrt{\frac{C_p}{L}} \cdot \sin \omega_s (t - t_1) + I_{M1} \cdot \left[\omega_s + \frac{1}{\omega_s}\right] \cdot \cos \omega_s (t - t_1) \tag{8}$$

where $\omega_S = \frac{1}{\sqrt{LC_P}}$, $v_{Cs}(0) = V_{Csm}$, and $i_L(0) = I_{M1}$.

Due to the resonance between the inductor and the panel, the voltage polarity of the panel is changed from positive V_S to negative V_S at the end of resonance. This mode is in the sub-resonance to recover the energy consumption by the capacitive displacement current of the PDP and to change the polarity of the voltage across the panel.

Mode 3 (t_2 - t_3): At t_2, voltage across the panel becomes negative V_S, and current flowing through the panel is null. S_3 and S_4, the terminal of mode 2, are turned on simultaneously to sustain the voltage across the panel negative V_S. Then the main resonant path between the inductor and the external capacitor is reformed by D_3 and D_4, as indicated in Fig. 5(c); therefore, the stored energy in the inductor is transferred to the external capacitor. During this mode, the circuit equation can be derived as

$$i_L(t) = V_s \cdot \sqrt{\frac{C_s}{L}} \cdot \sin \omega_m (t - t_2) - I_{M2} \cdot \left[\omega_m + \frac{1}{\omega_m}\right] \cdot \cos \omega_m (t - t_2) \tag{9}$$

where $\omega_m = \frac{1}{\sqrt{LC_S}}$, $v_{Cs}(0) = V_S$, and $i_L(0) = I_{M2}$.

During the prior mode, if the resonance was complete, or

voltage across the panel became negative V_S exactly, the input current supplied from the power supply through S_A will be zero. However, it is somewhat difficult because of electrode resistance, on-resistance of the power MOSFETs, and other non-ideal factors. A complete resonance during the prior mode can guarantee that voltage across the panel sufficiently became negative V_S. It is important in the viewpoint of recovery efficiency because voltage across the panel is sufficiently increased by the resonance during the mode 2, a lower input current will be needed to sustain a constant panel voltage.

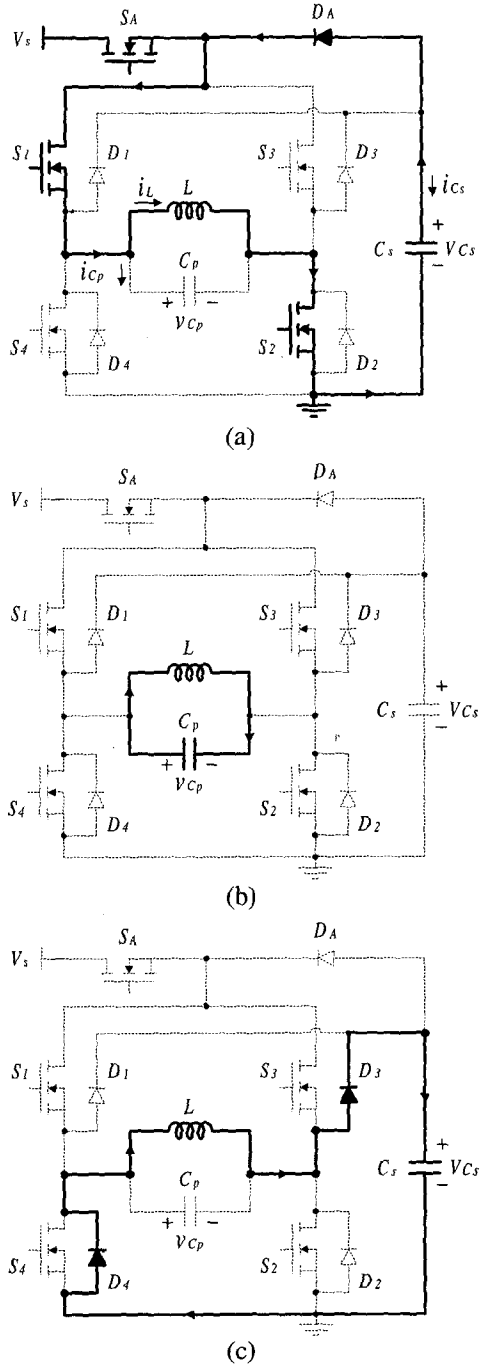


Fig. 5 Operational modes: (a) Mode 1, (b) Mode 2, (c) Mode 3

2.3 Design Considerations

According to the characteristics of the PDP, the operating frequency is determined. In practical applications, the PDP is usually operated from 80 to 200 kHz. Under the fixed operating frequency, the following design procedure indicates how to calculate the proper values of the inductor and external capacitor to achieve a complete dual resonance. Generally, when series connected switches are used, a sufficient dead-time should be set to protect pole-switches from an arm short. To obtain a high contrast ratio, the sustain period that is clamped by V_S is generally set to about 1-1.2 μs in the 200 kHz operating frequency. As a result, half of the balance can be used for sub-resonance time and is determined by

$$t_2 - t_1 = t_5 - t_4 \geq \pi\sqrt{L \cdot C_P}\,. \tag{10}$$

Because the panel capacitance C_P is usually determined by the panel size, inductor value can be obtained from Equation (10). Main resonance occurs prior to sub resonance in order to repeatedly change the polarity of voltage across the panel and should happen twice in a complete cycle. Therefore, the frequency of main resonance between the inductor and the external capacitor should be equal to the operating frequency. Hence, the value of the external capacitor can be calculated as

$$f_S = \frac{1}{2\pi\sqrt{L \cdot C_S}} \tag{11}$$

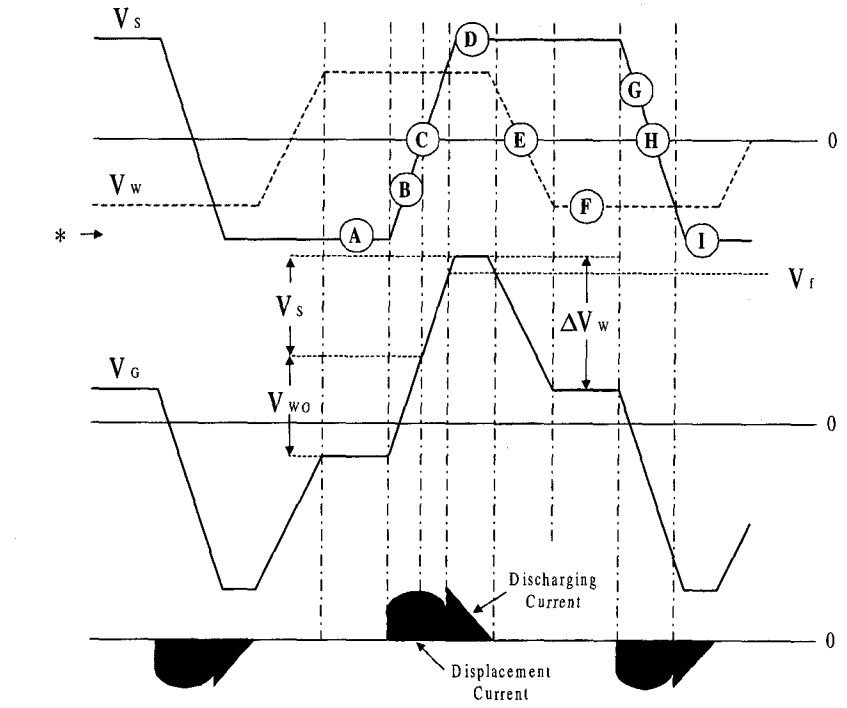
where f_S is the operating frequency of the PDP. For practical purposes, obtaining the exact value of elements is very difficult due to non-ideal components, such as stray capacitance, inductance, and other unexpected factors; moreover, the total capacitance of the panel is always changing according to the condition of the pixels. Therefore, the optimal values might be obtained by trial-and-error through simulation or experimentation considering the panel condition.

2.4 Relationship Between the Wall-Voltage and the Applied Voltage

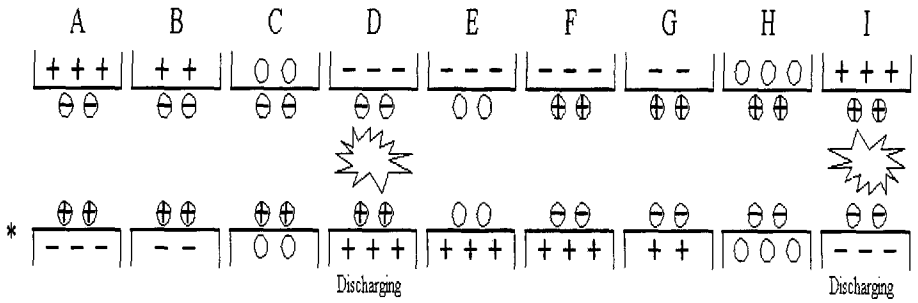
In general, the AC-PDP driver utilizes its inherent memory characteristic via the accumulated wall charge in a discharge space.

Fig. 6 illustrates the relationship between the wall voltage V_W and the applied voltage V_S in the discharge space. Fig. 6 also shows the relative conditions of ions and electrons that depend upon the voltage variation of the discharge space. In this figure, V_G means the voltage across the discharge space. To simplify its explanation, we ignored the address electrode and it was regarded as simple electrodes.

As shown in Fig. 6, the wall-voltage generated by accumulated wall-charges affects the igniting of the panel. When the voltage of discharge space V_G is lower than the discharge



(a)



(b)

Fig. 6 Relationship between wall-voltage and applied voltage: (a) Variation of the voltage in a discharge space, and the displacement and discharging current, (b) Arrangement of ions and electrons according to the polarity of supplied voltage and wall-voltage

inception voltage V_f, no igniting occurs as described from A through C (or from F to H) in Fig. 6. During the period from B to C (or from G to H), the displacement current just flows through the panel due to the variation of V_S. On the other hand, V_G becomes higher than V_f, the panel starts to ignite, and the discharging current flows through the panel as shown in case D (or I). At this moment, wall-charges are accumulated on the dielectric layers, decreasing the effective voltage of the discharge space. The igniting stops when V_G becomes critically lower than V_f. The next discharge starts when the polarity of the applied pulse is reversed. Consequently, once the discharge is begun, it repeats again and again as long as the sustain voltage is alternatively supplied to the panel. Thanks to the memory characteristic of the panel, a sustain voltage lower than the discharge inception voltage V_f can operate the AC-PDP, emitting visible light.

3. Simulated and Experimental Results

Fig. 7 shows the configurations of the three mentioned sustain drivers with their control signals. To assess the validity of proposed sustain driver, the three prior circuits, i.e., Weber's, Hsu's, and Liu's sustain drivers, are simulated with Pspice. The used components are listed in detail in Table I. Fig. 8 shows the simulated results of voltage across and of current flowing through the panel in each circuit at the sustain voltage V_S=180 V; therefore, only displacement current flows through the panel. The simulated waveforms of voltage across the panel of Weber's and Hsu's sustain drivers are analogous to that of Fig. 2(a). On the other hand, the operational waveforms of the proposed circuit is very similar to that of Liu's driver.

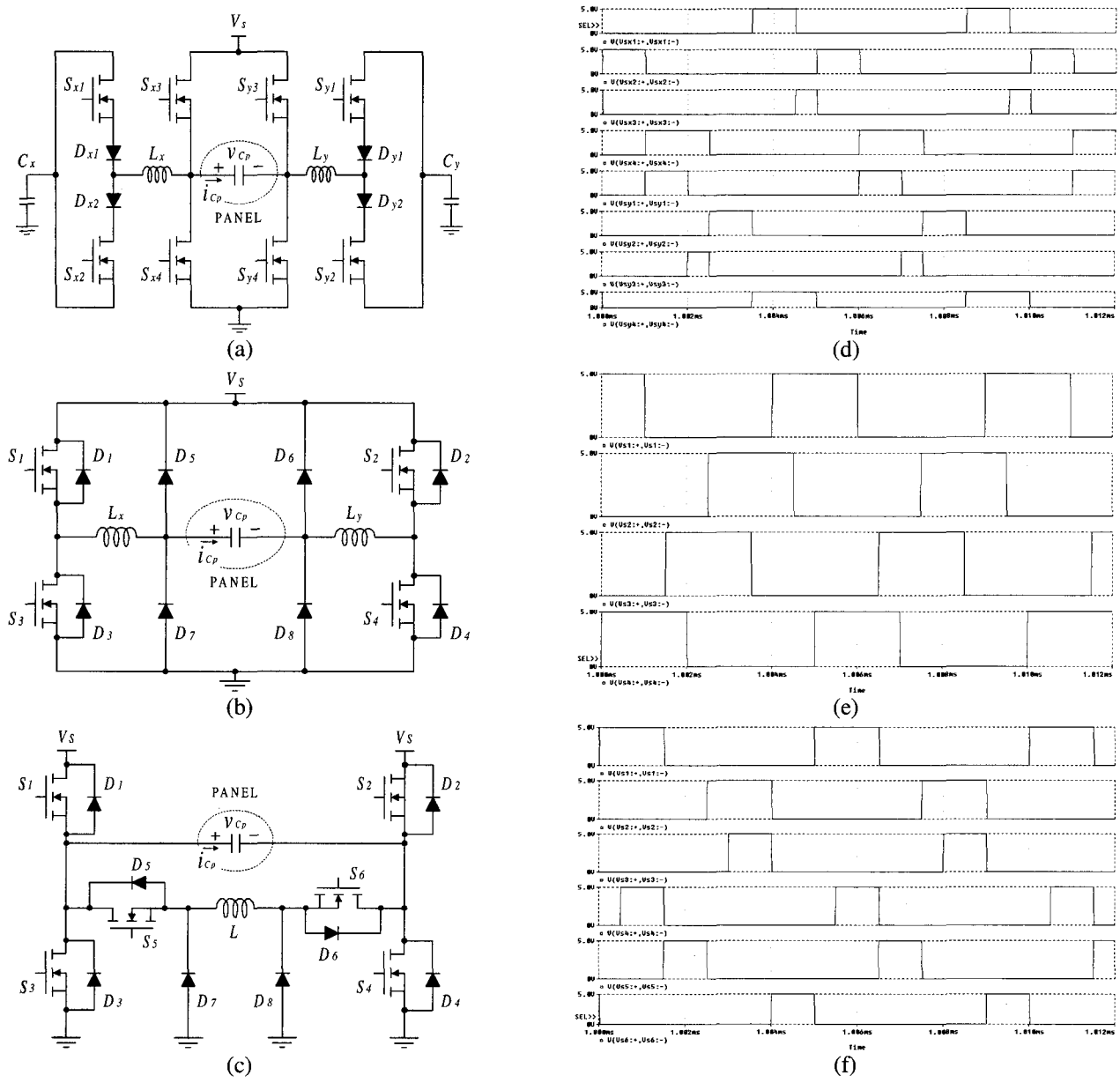


Fig. 7 The prior sustain drivers and their gate signals for simulation at V_s=180 V: (a) Weber's circuit, (b) Hsu's circuit, (c) Liu's circuit, (d) Gate signal of (a), (e) Gate signal of (b), (f) Gate signal of (c)

Table 1 Components list of each sustain driver for simulation

Items \ Sort	Weber's		Hsu's		Liu's		Proposed	
	Symbol	Value	Symbol	Value	Symbol	Value	Symbol	Value
switch	Sx1-Sx4 Sy1-Sy4	IRF460	S1-S4	IRF460	S1-S6	IRF460	SA/S1-S4	IRF460
diode	Dx1, Dx2 Dy1, Dy2	mbr4040	D1-D4 D5-D8	internal mbr4040	D1-D6 D7, D8	internal mbr4040	D1, D3, DA	mbr4040
inductor	Lx, Ly	20 μH	Lx, Ly	40 μH	L	55 μH	L	120 μH
external capacitor	Csx, Csy	220 nF	-	-	-	-	Cs	220 nF
ESR of inductor/capacitor	0.02 / 0.01 ohm, respectively							
Panel	Before igniting = 1.5 nF, After igniting = 3 nF							

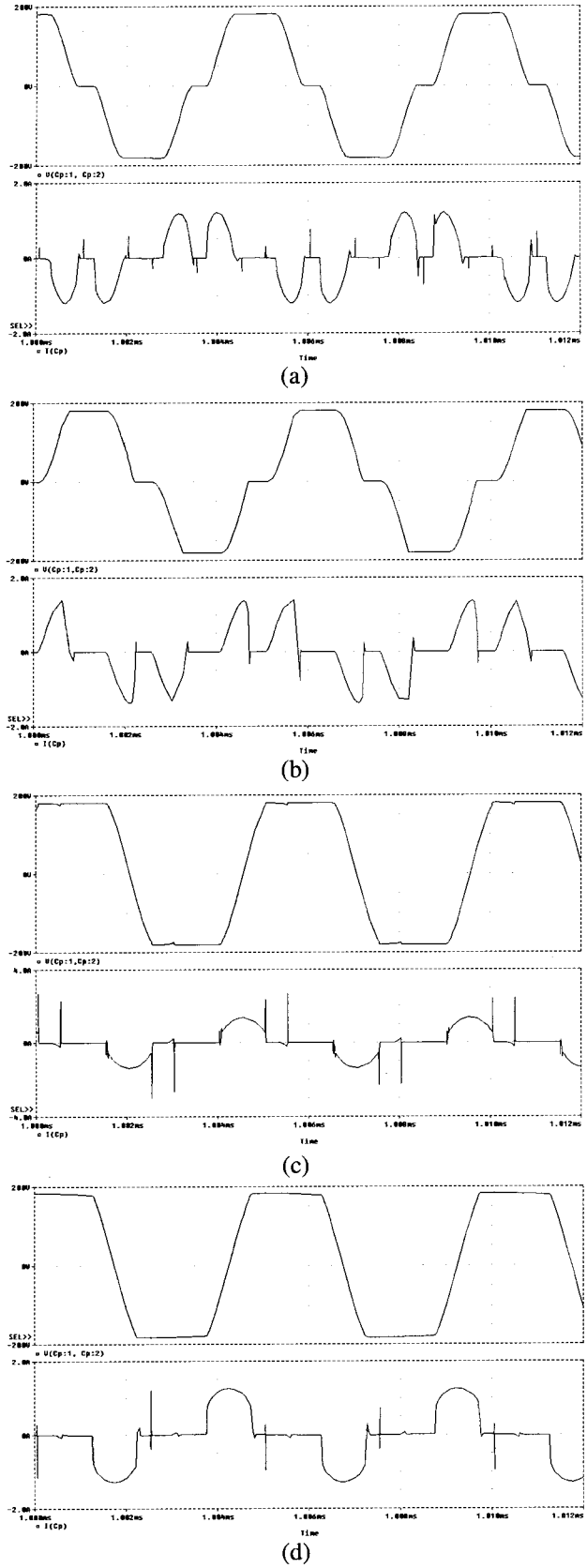


Fig. 8 Simulated waveforms of panel voltage and current in each sustain driver at V_S=180 V: (a) Weber's circuit, (b) Hsu's circuit, (c) Liu's circuit, (d) Proposed circuit

Fig. 9 shows the simulated results of the proposed sustain driver employing an energy recovery function to verify the theoretical analysis at the supplied voltage V_S = 180 V. From the waveforms of v_{Cp}, i_{Cp}, i_{Cs}, and i_L, the dual resonant operation can be found: $i_{Cp} + i_{Cs} = i_L$. One is the main resonance between the inductor and external capacitor, and the other is the instantaneous sub-resonance between the inductor and the panel.

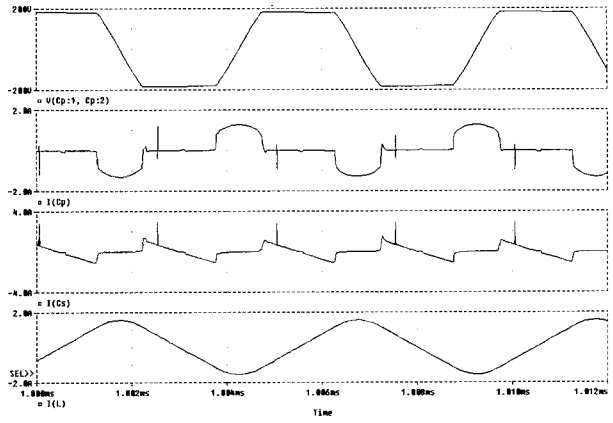


Fig. 9 Simulated waveform of proposed circuit, V_S=180V

Based on the simulated results, a prototype for the implementation was manufactured according to Table II. The prototype was equiped with a 7.5-inch-diagonal panel that has the maximum value of capacitance approximately 3 nF when all pixels of the PDP are igniting. The operating frequency is set to 200 kHz, and the control signals were generated by the ALTERA using the VHDL (Very High Speed Integrated Circuit Hardware Description Language). In the experiment, when voltage across the panel is higher than that of discharge inception, all the pixels of the panel are ignited displaying a white image, since no reset and address periods were considered.

Fig. 10 shows the experimental waveforms of the proposed sustain driver before and after igniting. Figs. 10(a) and (b) show the voltage across and the current flowing through the panel, inductor, and external capacitance when no light is emitted. During a dead-time, the mentioned sub-resonance between the inductor and panel can be verified from the experimental waveforms. In this case, only displacement current is flowing through the panel due to the variation of applied voltage. When voltage across the PDP is increased up to the discharging inception level, the panel will start to ignite the pixels, showing visible light. At this moment, the discharging current flows through the panel in addition to the displacement component. The discharging current appears in the tail of the current flowing through the panel as shown in Fig. 10(d), and we find that voltage across the panel is slightly affected by gas as shown in Fig. 10(c). Since we considered no driving voltages added from an address driver, which could influence the sustain voltage of the next display period, a higher voltage, i.e., over 200 V, is required to ignite the panel.

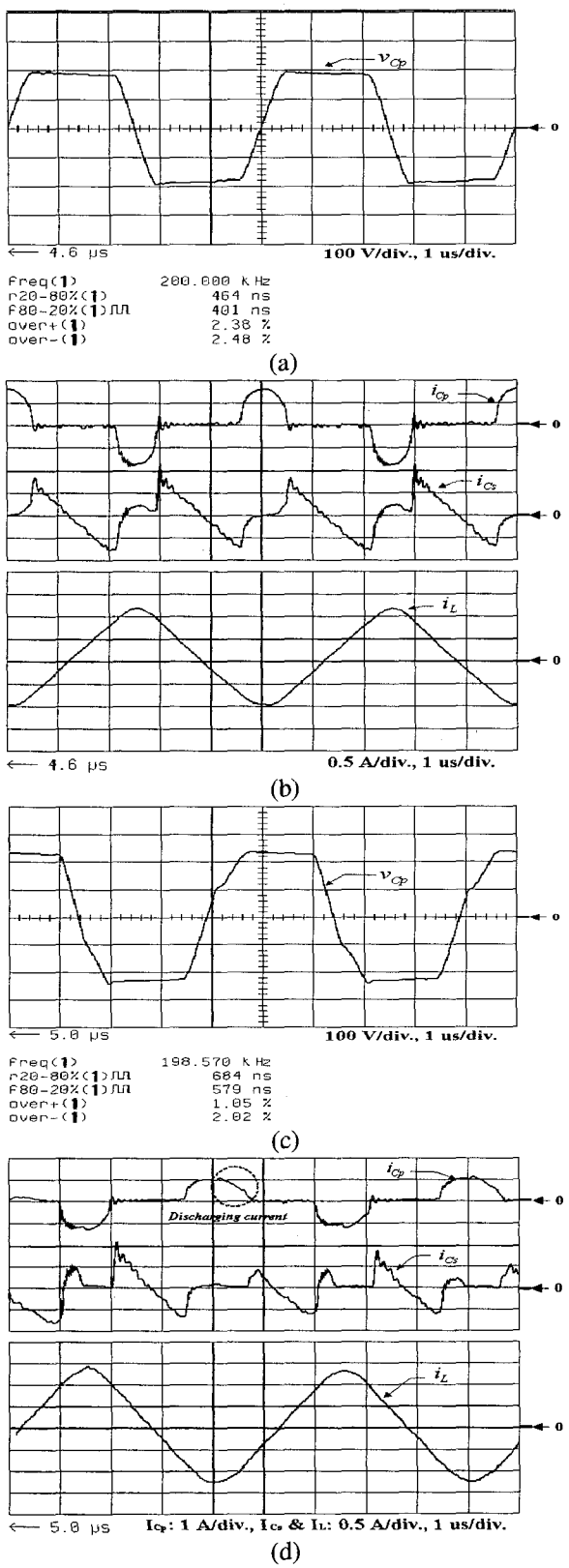


Fig. 10 Experimental waveforms of the proposed sustain driver employing the energy recovery faculty: (a) Before light emission, V_S=180 V, (b) During light emitting, V_S=240 V

Table 2 Components of the proposed sustain driver

Items	Symbol	Value or Type	Manufacturer
Panel	Cp	7.5 inch AC PDP	LG Electronics Inc.
Power MOSFET	S1-S4	IRFP460	Inretnational Rectifier
Diode	D1, D3,DA	FE6D	General Semiconductor
Inductor	L	150 μH / Aircore	-
External capacitor	Cs	220 nF / Metallized Polyester Film	
Gate Amp	-	TLP250 / Photocoupler	Toshiba
Signal Generation	-	EPM7064LC84 using VHDL	ALTERA

This paper provides a new sustain driver that will recover the energy otherwise lost in charging and discharging the panel capacitance, *Cp*. The efficiency with which the sustain circuit recovers the energy, the recovery efficiency, is expressed by the provided input current from a power supply.

$$E_R = \left(\frac{I_{wo} - I_w}{I_{wo}}\right) \times 100 = \left(1 - \frac{I_w}{I_{wo}}\right) \times 100 \ \% \qquad (12)$$

where I_{wo} and I_w are the averaged input current without and with the energy recovery circuit, respectively. Notice that the recovery efficiency is not equivalent to conventional power efficiency, defined in terms of the power delivered to a load, since no power is delivered to the capacitor, *Cp*; it is simply charged and then discharged [7]. The recovery efficiency of each circuit according to the variation of applied voltage is shown in Fig. 11. The recovery efficiency was compared using the simulated results, and Table I details the simulation conditions. As shown in Fig. 11, a steep increase or decrease in the slope of the indicates that the cells starts to discharge. In the case of proposed circuit, the recovery efficiency before igniting is to almost 95 percent regardless of the variation of sustain voltage. After igniting, the recovery efficiency decreases to 90 percent. The other circuit's recovery efficiency increases. This difference occures because charging and discharging operations in the proposed circuit occurs during a dead-time period and it does not occur during such a period in the other circuits.

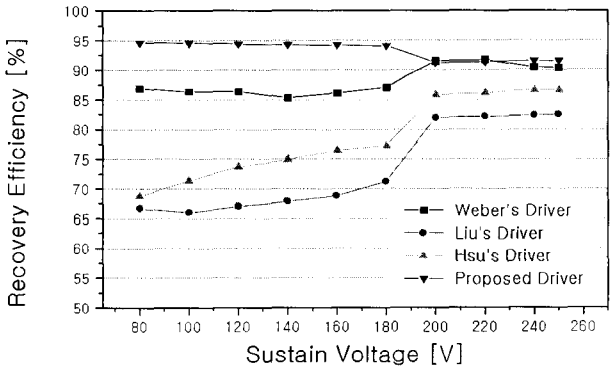


Fig. 11 Comparison of the recovery efficiency of each sustain driver

5. Conclusion

Based on dual resonance, a sustain driver employing the energy recovery faculty is proposed for an efficient drive of a plasma display panel in sustaining mode operation. The proposed driver has a simple structure compared with the conventional approaches. The most outstanding characteristic of proposed driver its use of dual resonance: the main resonance between the inductor and the external capacitor to generate alternative pulses and a sub- resonance between the inductor and the panel to recover the energy consumption by the capacitive displacement current of the PDP. Thus dual resonance results in a high recovery efficiency. The operational principle and design procedure of the proposed circuit are presented with theoretical analysis. The validity of proposed circuit is verified through simulation and experimental results based on a 7.5-inch-diagonal panel with a 200 kHz operating frequency.

References

[1] A. Sobel, "Plasma Displays," *IEEE Trans. on Plasma Science*, vol. 19, no. 6, pp. 1032-1047, Dec. 1991.

[2] M. Seki, et al., "Improved 40-inch Plasma Display for Wall-Hanging HDTV Receiver," *IEEE Trans. on Broadcasting*, vol. 42, no. 3, pp.208-214, Sept. 1996.

[3] D. W. Parker, et al., "The TV on the Wall-Has Its Time Come?" *Proc. of International Broadcasting Convention*, pp.575-580, 1997.

[4] Y. K. Shin, et al., "The Voltage-Pulsing Effects in AC Plasma Display Panel," *IEEE Trans. on Plasma Science*, vol. 27, no. 5, pp. 1366-1371, Oct. 1999.

[5] K. Yoshikawa, et al., "A Full Color AC Plasma Display with 256 Gray Scale," *Proc. of International Display Research*, pp. 605-608, 1992.

[6] John G. Webster, et al., *The Measurement, Instrumentation, and Sensors Handbook*, CRC & IEEE Press, vol. 2, pp. 93/1-30, 1999.

[7] L. F. Weber, et al., "Power Efficient Sustain Drivers and Address Drivers for Plasma Panel," U.S. Patent 4 866 349, Sept. 1989.

[8] H. B. Hsu, et al., "Regenerative Power Electronics Driver for Plasma Display Panel in Sustain-Mode Operation," *IEEE Trans. on Industrial Electronics*, vol. 47, no. 5, pp. 1118-1125, Oct. 2000.

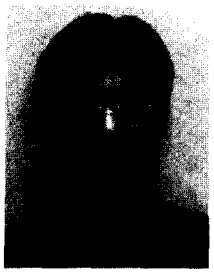
[9] C. C. Liu, et al., "A Novel Energy-Recovery Sustaining Driver for Plasma Display Panel," *IEEE Trans. on Industrial Electronics*, vol. 47, no. 6, pp. 1271-1277, Dec. 2000.

[10] M. Ohba, et al., "Energy Recovery Driver for a Dot Matrix AC Plasma Display Panel with a Parallel Resonant Circuit Allowing Power Reduction," U.S. Patent 5 670 974, Sept. 1997.

[11] L. F. Weber, "Measurement of Wall Charge and Capacitance Variation for a Single Cell in AC Plasma Display Panel," *Proc. of Society for Information Display*, vol. 18, no. 1, pp. 80-85, 1977.

Acknowledgment

The authors wish to thank the research engineers of LG PDP Electronics, Inc., in Gumi, Korea for their helpful comments and support.



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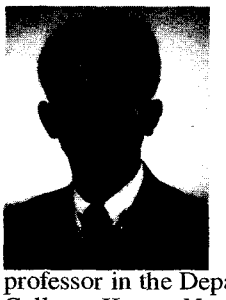

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