Anomalous Subthreshold Characteristics of Shallow Trench-Isolated Submicron NMOSFET with Capped p-TEOS/SiN

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In sub-1/4 ㎛ NMOSFET with STI (Shallow Trench Isolation), the anomalous hump phenomenon of subthreshold region, due to capped p-TEOS/SiN induced defect, is reported. The hump effect was significantly observed as channel length is reduced, which is completely different from previous reports. Channel boron dopant redistribution due to the defect should be considered to improve hump characteristics besides considerations of STI corner and recess.
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Keywords: MOSFET, STI, Hump, Subthreshold

1. INTRODUCTION

Locos Oxidation of Silicon (LOCOS) has been the ftraditional choice for isolation between devices in past Metal Oxide Semiconductor Field Effect Transistor (MOSFET) technologies. However, STI has been challenged widely as a substitute for the LOCOS isolation. It eliminates the LOCOS bird's beak and is fully planar with the Si surface. Inherent to this geometry are fringing gate fields that enhance carrier inversion within the Si corner at the isolation edge. As a result, there exists a parasitic transistor of low threshold voltage (V_t) in parallel with the main MOSFET channel region. N-channel MOSFET with this parallel corner device shows hump in subthreshold current characteristics, which results in the increase of standby leakage current. In this paper, anomalous hump phenomenon in subthreshold region, due to capped p-TEOS/SiN interlayer induced defect, is reported. Furthermore, it is mentioned that a parasitic transistor can be formed under local boron channel depletion induced by defect in a short channel N-type Metal Oxide Semiconductor Field Effect Transistor (NMOSFET). This results in significant hump effect as the channel length is reduced.

2. EXPERIMENTAL

Figure 1 shows a schematic cross section of Light Doped Drain (LDD)[1] NMOSFET with capped interlayers. The capped interlayers consist of a p-TEOS, or High temperature Low pressure Dielectric (HLD) oxide of 500nm under a LPCVD SiN of 30nm, or only a HLD oxide of 500nm. In NMOSFET process, 40keV B ions with a dose of 3e12/㎠ were implanted a tilt-angle of 30 degrees for halo pocket. As (20keV, 3e14/㎠) and P (20keV, 2e13/㎠) ions for n-implant are performed to reduce source/drain parasitic resistance and hot carrier effect, followed by formation of SiN sidewall spacer of 70nm. Gate oxide thickness is 6.7nm. In STI process, CVD oxide deposited to fill trenches, followed by densification. CMP[2,3] was applied to planarize the CVD oxide. The trench angle is 74.5 degrees and depth is 350nm. Fig. 2 shows cross-sectional SEM micrograph of STI with a round corner and recess of about 20nm.

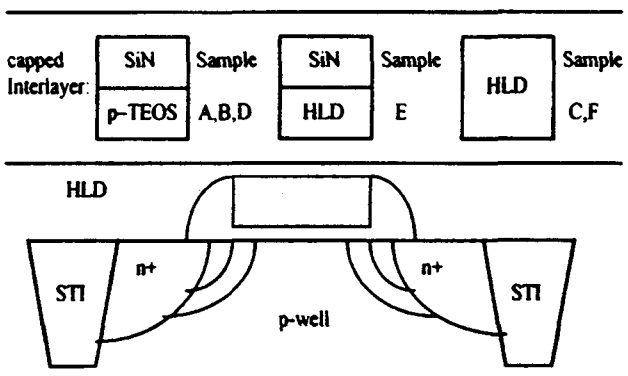

Fig.1. Schematic diagrams of sample structures.

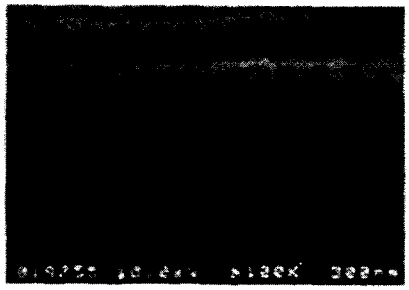

Fig. 2. Cross-sectional SEM micrograph of STI profiles.

3. RESULTS AND DISCUSSION

Table 1 shows NMOS process parameters of split samples. In Fig. 3, hump effect of sample A which has capped layers of SiN/p-TEOS increases as channel length is reduced. This phenomenon is completely different from that reported by several authors[4] previously. It is well known that for short channel transistors, the hump effect almost disappears. This was due to the reduced sensitivity of the corner transistor to the short channel effect in comparison with that of the main transistor. For sample C which has a capped interlayer of only HLD, any hump effects, regardless of

Table 1. NMOS Sample Parameters.

Sample	A	B	C	D	E	F
Gate Oxide	SiO2	SiO2	SiO2	SiO2/NO	SiO2/NO	SiO2/NO
STI Recess	~20nm	~20nm	~20nm	~20nm	~20nm	~20nm
Channel (B+, 20KeV)	2E12	1.4E13	2E12	4.6E12	4.6E12	4.6E12
Capped Interlayer	SiN/ p-TEOS	SiN/ p-TEOS	HLD/ HLD	SiN/ p-TEOS	SiN/ p-TEOS	HLD/ HLD

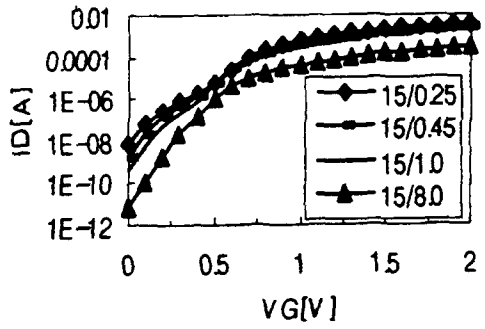

Fig. 3. Hump characteristics with different gate lengths of sample A.

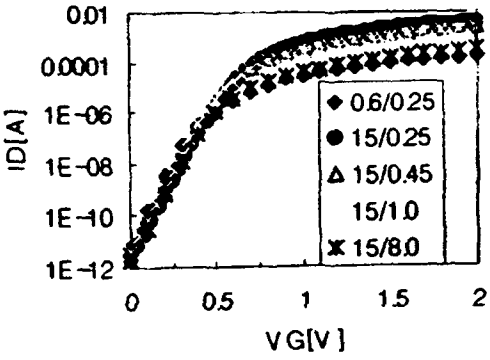

Fig. 4. Id-Vg characteristics of sample C with different Lg/W.

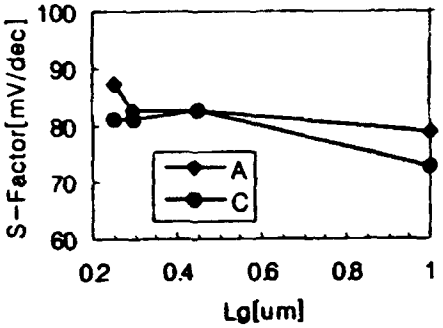

Fig. 5. S-factor (V_{bs} =—5V) vs. gate length of sample A and C.

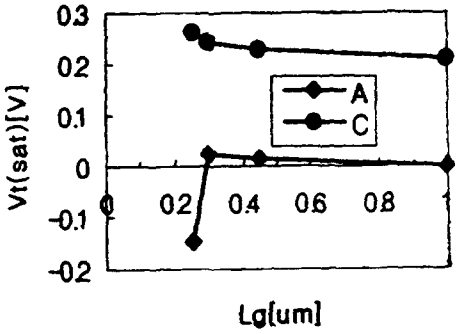

Fig. 6. Vt (sat) roll-off characteristics of sample A and C.

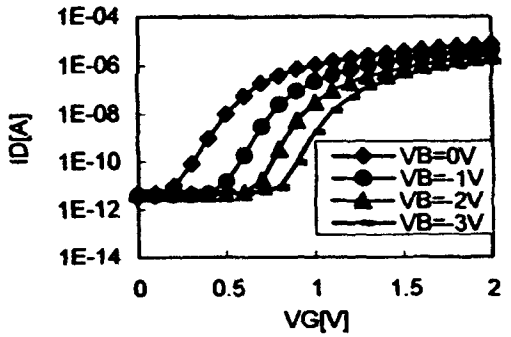

Fig. 7. Id-Vg characteristics of sample B.

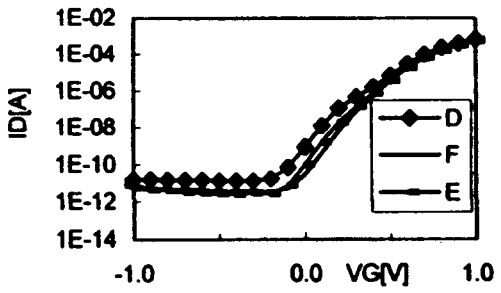

Fig. 8. Id-Vg characteristics of sample D, E and F.

channel length, are not shown in Fig. 4. Carbon[5] defect due to the TEOS- based oxide under SiN and Hydrogen[6] defect due to the SiN capping layer have been reported previously. Theses defects may diffuse to the gate channel edge of high oxide field near Shallow Trench Isolation (STI). Channel boron dopant diffusivity is proportional to the defect concentration, which results in B-depletion at gate edge locally. In long channel length, sufficient boron dopant is provided from center to the gate edge. This prevents generation of a local parasitic transistor of low Vt. In a short channel length, there is not sufficient dopant in the channel center. The resulted local B-depletion[7] makes a parasitic transistor of low Vt and enhances Vt roll-off. In Fig. 5, S-factor under strong back bias of sample A and C are compared with respect to the gate length. Sample A has more interface defects than those of sample C because S-factor under strong back bias is proportional to gate interface defect density. In Fig. 6, sample A shows significant Vt roll-off characteristics via weak reverse short channel effect in comparison of those of same channel dose of sample C. Vt(sat) was measured at a normalized drain current of 0.1nA* (W/L) at Vds=2.5V. For sample B, even under SiN/p-TEOS induced defect, hump characteristics are not shown owing to the high channel dose in Fig. 7. In Fig. 8, a hump effect is the most significant in the sample D and not shown in sample F which has only a HLD interlayer.

4. CONCLUSION

Interlayer, p-TEOS/SiN induced defect may diffuse to the gate channel edge of the high field near STI and make local boron channel depletion. This results in a parasitic transistor of low Vt and enhances Vt roll-off. Significant hump effect was observed as channel length is reduced, which is completely different from previous reports. In Shallow Trench Isolated NMOSFET, channel dopant redistribution due to defects should be considered to improve hump characteristics in the subthreshold region besides STI corner shape and recess.

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