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New Energy Recovery Concept for AC PDP Sustaining Driver Using Current Injection Method (CIM)

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ABSTRACT

New concept of energy recovery for plasma display panel (PDP) is proposed. Different from conventional LC resonant sustaining drivers, the current built up before inverting the polarity of the panel electrodes is utilized to change the panel polarity together with energy previously charged in panel capacitance. This operation provides zero-voltage-switching of switches and reduction of EMI by rejecting the surge current when the sustain switches are turned on. The build-up current helps to reduce transition time of panel polarity and may produce more stable light waveforms. This method shows a desirable characteristic that the circuit loss is similar to that of series resonant type energy recovery circuit which is very effective method.

Keywords: Plasma Display Panel, Sustain Driver, LC resonance

1. Introduction

Plasma display panel (PDP) takes an advantage over other flat panel display by the wide view angle, large screen, high brightness and thinness. Thanks to the attractive merits, the PDP is expected to be a promising candidate in the display market[1]. Fig. 1 shows the simplified PDP structure with three electrodes. It consists of two glass plates with chemically stable rare gases filled between them. The scanning and sustaining electrodes are built on the front glass, which is coated with dielectric layer and the addressing electrode is on the rear glass. A desired color light can be obtained by exciting the phosphors on the addressing electrode to emit visible light with the ultraviolet photons generated by gas discharge[2]. The operation of PDP is divided into three periods of setup, addressing, and sustaining periods. During the setup period, all of the PDP cells are erased and prepared to carry out addressing by forming an adequate wall charges.

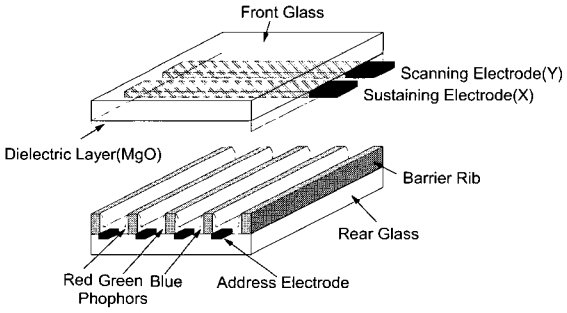

Fig. 1. Simplified PDP structure with three electrodes.

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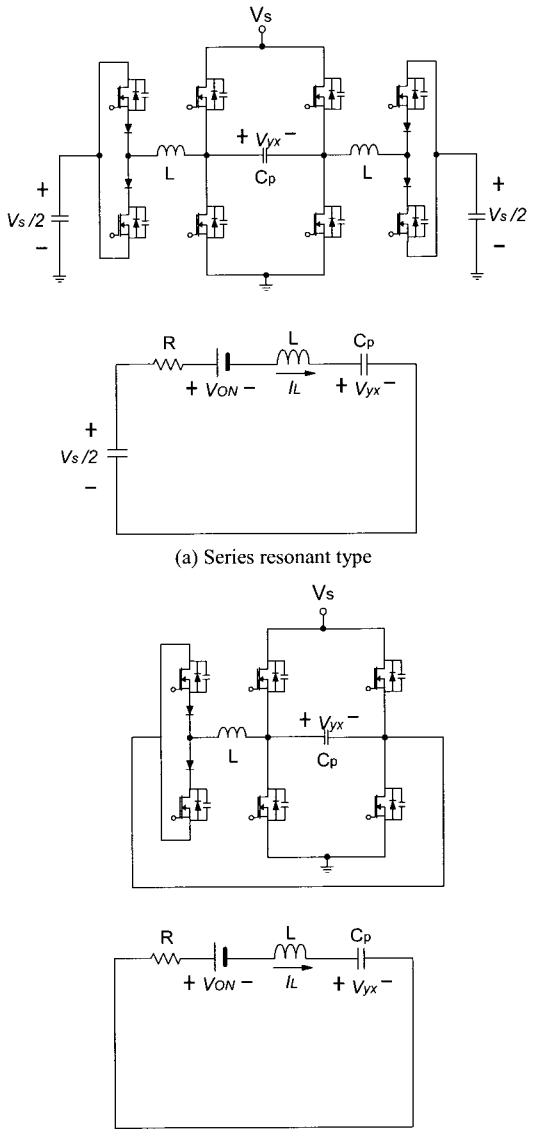
After that, selective write discharges to form an image are ignited by applying data and scanning pulses to the addressing and scanning electrodes, respectively[3]. Since addressing discharge itself emits an insufficient visible light, a high voltage AC square pulses are continuously applied between sustaining and scanning electrodes for strong light emission of selective cells. The high voltage pulses can be generated by using a simple full bridge driver and most of the PDP power is consumed during this sustaining period. Since a dielectric layer is incrusted on sustaining and scanning electrodes, capacitance between two electrodes exits inherently. When applying a sustaining pulse on electrodes, an amount of energy is dissipated in switches and parasitic resistances of wire during charging and discharging transients, where C_p is panel capacitance and V_s is sustain voltage. If an average frequency of sustaining pulse is , then the total dissipated power is [4]. Without a proper method to recover the energy, a large amount of surge current causes EMI and heating problem of switching devices. To solve the problems, L. F. Webber, et al. suggest an energy recovery circuit(ERC) using series LC resonant concept[5]. It features a high efficiency and good circuit flexibility to cope with various driving method, which leads many PDP makers. M. Ohba, et al. have reduced this circuit supporting parallel LC resonance[6]. Afterwards, several researchers have studied various circuit types to improve performances and reduce circuit volumes[4]. However, due to the considerable circulating current, efficiency and flexibility are not good compared with conventional PDP drivers, which make difficult to produce on a commercial scale.

In this paper, new concept of energy recovery using current injection method (CIM) is proposed. Before inverting the polarity of the panel electrodes, the inductor current is built up and it is used to invert the panel polarity together with energy previously charged in panel capacitance. This operation helps to achieve the zero-voltage-switching of switches and reduce the EMI by rejecting the surge current. In addition, it helps to reduce transition time of panel polarity, which may produce more stable light waveforms. By reducing the circulating current, the good circuit efficiency can be obtained in the prototype driver for 42 inch PDP.

2. Prior Approaches

Fig. 2 shows the prior approaches suggested by L. F. Webber and M. Ohba using series or parallel LC resonance and their equivalent circuits during LC resonant period. The sustain voltages go up or down to some voltage level in resonant manner and sustain switches are turned on to hold a sustain voltage. At that moment, a large surge current occurs. In this figure, R means the parasitic resistance including on-resistances of switches and V_{ON} means the diode forward drop.



(a) Series resonant type

(b) Parallel resonant type

Fig. 2. LC resonant type PDP driving circuits and their equivalent circuit during resonance.

Based on this figure, the panel voltage V_{yx} can be obtained as follows:

Series resonant type:

$$V_{yx}=\left(\frac{V_s}{2}-V_{ON}\right)\left[1-e^{-t/\tau}\left(\cos\omega t+\frac{\omega R}{L}\sin\omega t\right)\right] \quad (1)$$

Parallel resonant type:

$$V_{yx}=-(V_s-V_{ON})e^{-t/\tau}\left(\cos\omega t+\frac{\omega R}{L}\sin\omega t\right)-V_{ON} \quad (2)$$

where, $\tau=\frac{2L}{R}$ and $\omega=\sqrt{\frac{1}{LC_p}-\left(\frac{R}{2L}\right)^2}$. If $\left(\frac{2L}{R}\right)^2$ and $\frac{\omega R}{L}$ can be ignored, eqs. (1) and (2) are simply rewritten as

Series resonant type:

$$V_{yx}=\left(\frac{V_s}{2}-V_{ON}\right)\left[1-e^{-t/\tau}\cos\omega' t\right] \quad (3)$$

Parallel resonant type:

$$V_{yx}=-(V_s-V_{ON})e^{-t/\tau}\cos\omega' t-V_{ON} \quad (4)$$

where, $\omega'=\sqrt{\frac{1}{LC_p}}$. The peak values of two equations occur at $\omega'=\pi$ and can be obtained as follows:

Series resonant type:

$$V_{yx,pk}=\left(\frac{V_s}{2}-V_{ON}\right)\left(1+e^{-\frac{\pi R}{2}\sqrt{\frac{C_p}{L}}}\right) \quad (5)$$

Parallel resonant type:

$$V_{yx,pk}=-(V_s-V_{ON})^{-\frac{\pi R}{2}\sqrt{\frac{C_p}{L}}}-V_{ON} \quad (6)$$

It says that increase of the parasitic resistance causes the recovery efficiency to be degraded. Naturally, it is necessary to reduce the parasitic resistance by designing the circuit board optimally as well as choosing switching devices with small on-resistance and low on-drop voltage to minimize the hard-switching stress and improve the recovery performance. However, since it is impossible to get rid of the parasitic components completely, EMI and switching stress caused by the surge current are inevitable. It shows the limitations of simple LC resonant method. On the other hand, reduction of the inductor value produces the similar results and, thus, using too small value of L is not desirable in the aspect of driving loss and EMI.

3. Mode Analysis

Fig. 3 is the PDP driver circuit to adopt the CIM method. This circuit is similar to series resonant type circuit except that the energy storage capacitors are connected in series between V_s and ground. However, the operation is different from simple LC resonant method.

Fig. 4 is the key waveforms of the proposed method, divided by eight modes, and their operational mode diagrams are as shown in Fig. 5. It is assumed that before start of mode 1, the switches, Y_g and X_s are on and L_1=L_2=L. In addition, recovery capacitors of C_1, C_2, C_3, and C_4 are charged to the half of the sustain voltage. Because the operation of the two half cycle is symmetric, mode analysis is performed about the first half cycle.

Mode 1 ($t_0 \le t < t_1$)

Referring to Fig. 6, once the switch Y_r of the Y electrode is turned on, there forms a current path including capacitor C_2, switch Y_r, inductor L_1, and switch Y_g in sequence. On the other hand, when the switch X_f of the X electrode is turned on, there forms a current path including switch X_s, inductor L_2, switch X_f, and capacitor C_4 in sequence.

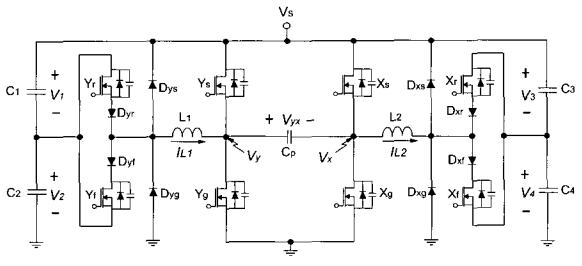


Fig. 3. PDP driver circuit to adopt the new method.

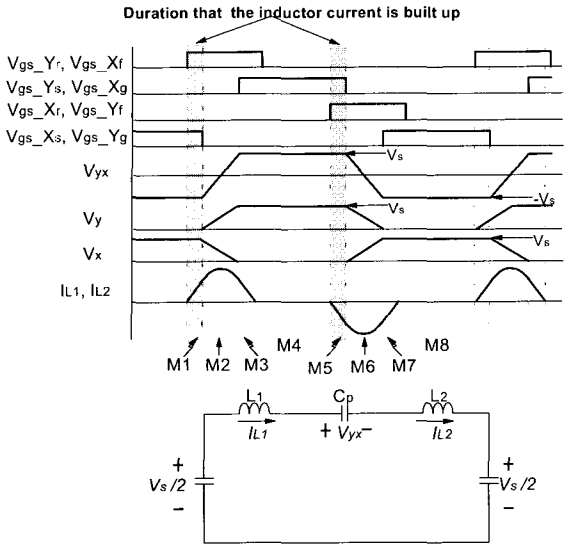
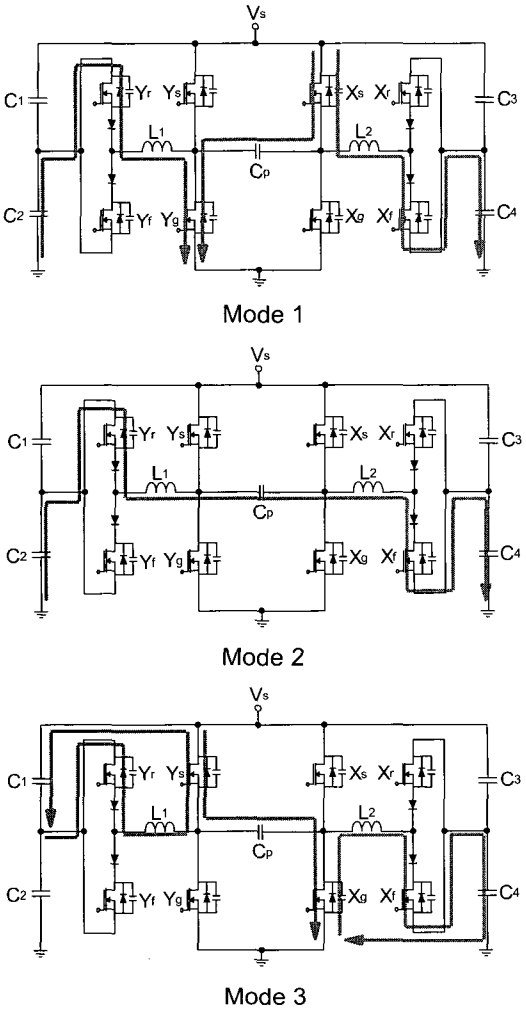


Fig. 4. Key waveforms of the proposed method and equivalent circuit during mode 2.



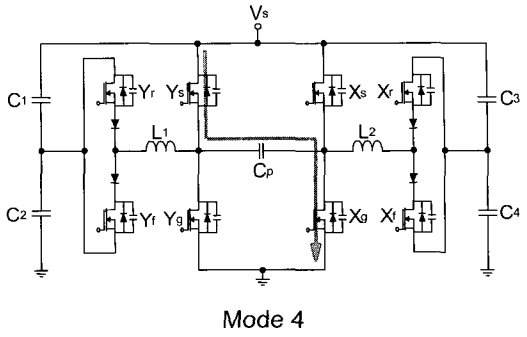


Fig. 5. Operational mode diagrams.

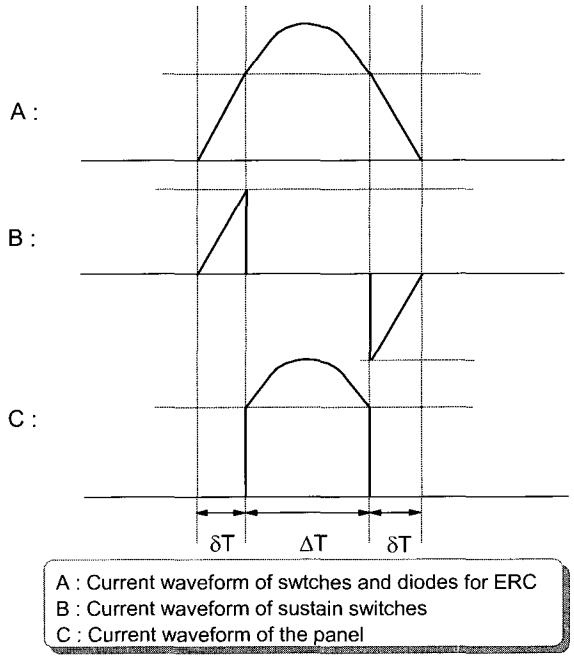


Fig. 6. Current waveforms of energy recovery and sustain circuits.

Accordingly, currents I_{L1} and I_{L2} flowing to the L_1 and L_2 linearly increase with slope of $V_s/2L$ to store the magnetic energy in the inductors. The currents are expressed as:

$$I_{L1} = I_{L2} = \frac{V_s}{2L}(t - t_0) \tag{7}$$

Mode 2 ($t_1 \le t < t2$)

When X_s and Y_g are turned off, the currents built up during mode 1 flow through capacitor C_2, switch Y_r, panel capacitance C_p, inductor L_2, switch X_f, and capacitor C_4 in sequence. A resonant current caused by the panel capacitance flows and the terminal voltage V_{yx} of the panel

capacitor is inverted in polarity from $-V_s$ to V_s. That is, the voltage V_y at the Y electrode rises from ground to the sustain voltage V_s and the voltage V_x at the X electrode falls from the sustain voltage V_s to ground. In this mode, the equivalent circuit is Fig. 4. From this circuit I_{L1}, I_{L2}, and V_{yx} are written as:

$$I_{L1} = I_{L2} = I_{L1}(t_1)\cos\omega_c(t-t_1) + \frac{V_s}{Z}\sin\omega_c(t-t_1) \quad (8)$$

$$V_{yx} = -V_s\cos\omega_c(t-t_1) + ZI_{L1}(t_1)\sin\omega_c(t-t_1) \quad (9)$$

where, $Z = \sqrt{\frac{2L}{C_p}}$ and $\omega_c = \frac{1}{\sqrt{2LC_p}}$.

Mode 3 ($t2 \le t < t3$)

After inverting the polarity of the panel capacitance, the body diodes of Y_s and X_g are turned on. Accordingly, the current I_{L1} starts to flow through capacitor C_1, switch Y_r, diode D_{yr}, inductor L_1, and body diode of Y_s. Similarly, I_{L2} flows through inductor L_2, diode D_{xf}, switch X_f, capacitor C_4, and body diode of X_g. Afterwards, when Y_s and X_g are turned on to hold the panel electrode voltage as the sustain voltage and ground, zero-voltage-switching is accomplished, which removes the switching loss and surge current. During this mode, I_{L1} and I_{L2} are ramped down to zero with the slope of $-V_s/2L$. This can be expressed as:

$$I_{L1} = I_{L2} = I_{L1}(t_2) - \frac{V_s}{2L}(t-t_2) \quad (10)$$

Mode 4 ($t_3 \le t < t_4$)

After L_1 and L_2 are completely reset, Y_r and X_f are turned off. Switching losses do not occurs since switch currents do not remain. During mode 4, the voltage V_y at Y electrode and the voltage V_x at X electrode are maintained at the sustain voltage and ground.

It is noted that during mode 2, the recovery capacitor delivers sufficient energy to the inductor so that regardless of the circuit loss, the voltages at sustaining and scanning electrodes can go up or down to the sustain voltage and ground completely with the aid of this delivered energy. Moreover, the remaining energy of inductors can be used for zero-voltage-switching of switches after inverting the panel polarity.

4. Design Considerations

4.1 Relationship of transition time ΔT, inductor L, and build-up time δT

The transition time ΔT is defined as the time during which the panel electrode voltage is changed between the sustain voltage and ground. the build-up time δT is the time during which the inductor current is built up prior to the inversion of the panel polarity. It is depicted in Fig. 6. By replacing t-t_1 with ΔT in eq. (9), the transition time can be found as:

$$\Delta T = \sqrt{2LC_p}\left[\cos^{-1}\left(-\frac{V_s}{\sqrt{V_s^2 + (ZV_s\delta T/2L)^2}} - \Theta\right)\right] \quad (11)$$

where, $\Theta = \tan^{-1}\left(\frac{Z\delta T}{2L}\right)$. The transition time becomes reduced as the build-up time becomes increased with a fixed value of L. It provides another design factor besides the inductor value.

4.2 Power losses

Circuit efficiency is the one of the most important factor to determine whether newly developed method is usable or not. Until now, many PDP driving circuits has been developed, but they are suffered from low efficiency compared with series and parallel resonant types. Based on the mode analysis and Fig. 6, the power dissipated in diodes and switches averaged over a switching period T_s can be written as follows:

$$P_{ER,SW} = \frac{4}{T_s}\left[2\int_0^{\delta T}\left(\frac{V_s}{2L}t\right)^2 R_{ds,ER}dt + \int_0^{\Delta T}\left(\frac{V_s\delta T}{2L}\cos\omega_c t + \frac{V_s}{Z}\sin\omega_c t\right)^2 R_{ds,ER}dt\right] \quad (12)$$

$$P_{ER,Diode} = \frac{4}{T_s}\left[2\int_0^{\delta T}\left(\frac{V_s}{2L}t\right)V_{ON}dt + \int_0^{\Delta T}\left(\frac{V_s\delta T}{2L}\cos\omega_c t + \frac{V_s}{Z}\sin\omega_c t\right)V_{ON}dt\right] \quad (13)$$

$$P_{SUS,SW} = \frac{4}{T_s}\left[2\int_0^{\delta T}\left(\frac{V_s}{2L}t\right)V_{ON}dt + \int_0^{\Delta T}\left(\frac{V_s}{2L}t\right)^2 V_{ON}dt\right] \quad (14)$$

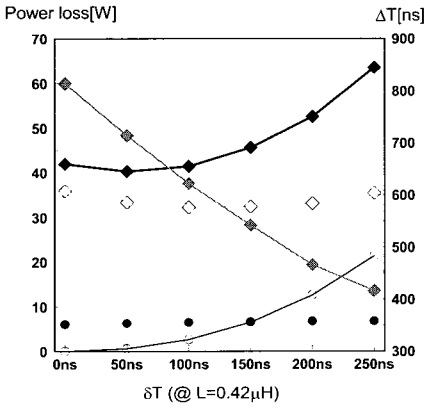
where, $R_{ds,ER}$ and $R_{ds,sus}$ are on-resistances of energy recovery and sustain MOSFETs, respectively. In addition, since the clamping currents through D_{ys}, D_{yg}, D_{xs}, and D_{xg} cannot be ignored, the power loss caused by this current expressed as eq. (15) should be considered.

$$P_{clamp} = \frac{4}{T_s}\left[\int_{\Delta T+\delta T}^{T_S/2}\left(i_{clamp}(t)V_{ON} + i_{clamp}(t)^2 R_{ds,sus}\right)dt\right] \quad (15)$$

where, C_{oss} is the output capacitance of the energy recovery switches and

$$i_{clamp}(t) = -\frac{V_{ON}}{R_{ds,sus}} + \left(\frac{V_s}{2}\sqrt{\frac{C_{oss}}{L}} + \frac{V_{ON}}{R_{ds,sus}}\right)e^{-\frac{R_{ds,sus}}{L}t} \quad (16)$$

Since the power dissipation caused by a large amount of surge current of sustain switches can be removed by using this method, most of the circuit losses are conduction loss. Different from simple LC resonant methods, it has some circulating current due to the current built up before inverting the panel polarity and this current may contribute to degrade the circuit efficiency. Using eqs. (12)-(16), the power losses under the build-up time and inductor value variations can be calculated with parameters used in prototype PDP driver, which is shown in Fig. 7.



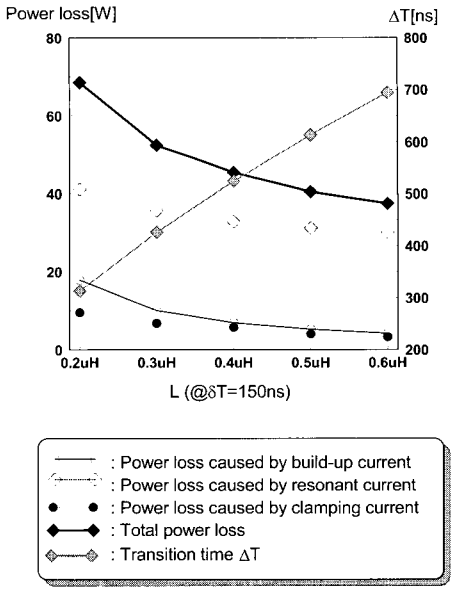


Fig. 7. Calculated power losses under δT and L variations without panel discharge at V_s=165V.

The power loss goes up as the build-up times and inductor values are varied so that the circulating current increases. Therefore, it is not desirable to choose an excessively large build-up time or small inductor value.

5. Design

To validate the proposed method, a prototype PDP driver circuit has been designed for 42" PDP panels with following specifications:

- Sustain voltage : V_s = 165V
- Switching frequency : fs= 200kHz
- Transition time : $\Delta T \geq$ 600ns
- Panel capacitance : C_p = about 80nF

Fig. 8 is the interaction plot that shows the currents supplied by the sustain power supply with δT and L variations when the panel discharge is removed to observe the circuit loss itself. The power loss is measured under five test image patterns such as full white, full red, full green, full blue, and nine white square images. The full white image pattern has the largest discharge current about 150A in 42 inch panel, but its sustain pulse number is smallest among other patterns.

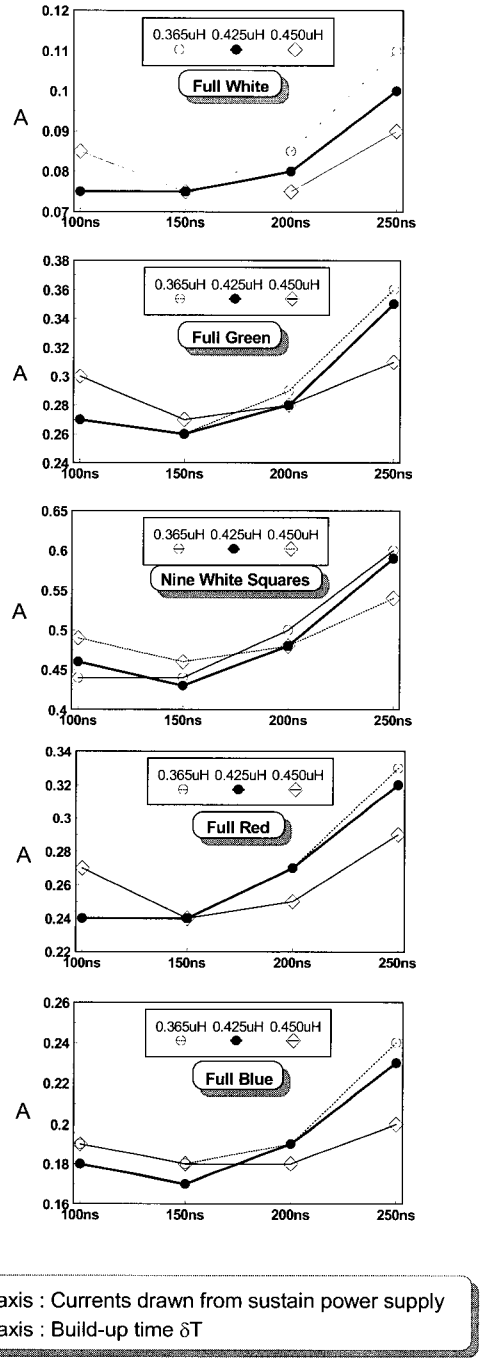


Fig. 8. Currents drawn from the sustain power supply under δT and L variations at V_s=165V.

Meanwhile, the nine white square pattern has the smallest discharge current, but many pulses are applied to the panel to obtain a peak brightness. The interaction plot shows that when L and δT are selected as 0.42μH and 150ns, respectively, the circuit power loss can be minimized. Using the selected values, the transition time can be obtained as 500ns from eq. (11). Table 1 is the key components for prototype PDP driver.

Table 1. Key components for prototype driver.

Y_s, Y_g, X_s, X_g	2SK2995 × 4
Y_r, Y_f, X_r, X_f	2SK2995 × 2
D_{yr}, D_{yf}, D_{xr}, D_{xf}	SF20LC30 × 4
Clamping diodes	SF20LC30 × 2
C_{yer1}, C_{yer2}, C_{xer1}, C_{xer2}	12μF
L_1, L_2	0.42μH

6. Experimental Results

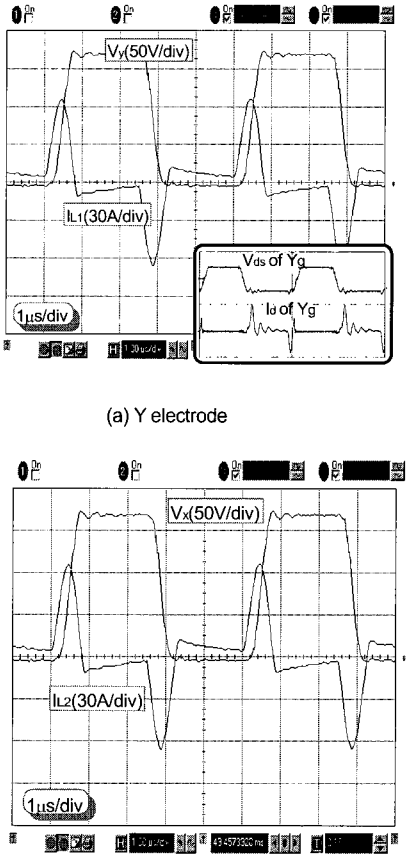
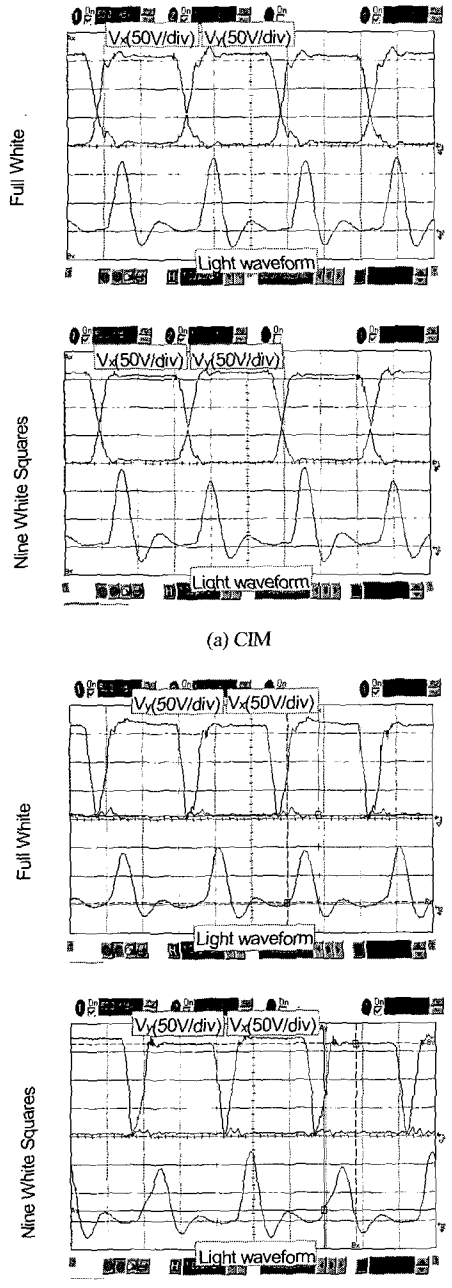


Fig. 9. Sustain voltage and inductor current waveforms at L= 0.42μH, δT= 150ns, and V_s=165V.

Fig. 9 shows the sustain voltage and inductor current waveforms. Before the panel polarity is inverted, the inductor currents are built up to about 35A and they are recovered to the capacitors after changing the panel polarity. The measured waveforms in box shows soft switching can be accomplished. The clamping currents caused by parasitic capacitance of energy recovery switches are also shown in this figure.

Fig. 10 is the voltage waveforms of the panel electrodes accompanied by light waveforms when panel discharge for emitting light happens. As can be seen in this figure, the start voltage of the panel discharge is higher than series resonant type and more stable light waveform can be obtained especially at nine white square image pattern.

Fig. 11 is the power loss comparison plot. It shows that the power loss is similar to that of series resonant type energy recovery circuit. It is desirable characteristic since this type has been known to be very effective method. The EMI test result is as shown in Fig. 12. The newly developed method shows a lower EMI level due to the reduction of surge current when the sustain switches are turned on. This characteristic will help PDP engineers to handle EMI.



(a) CIM

(b) Series resonant method

Fig. 10. Sustain voltage and light waveforms with panel discharge at Vs=165V.

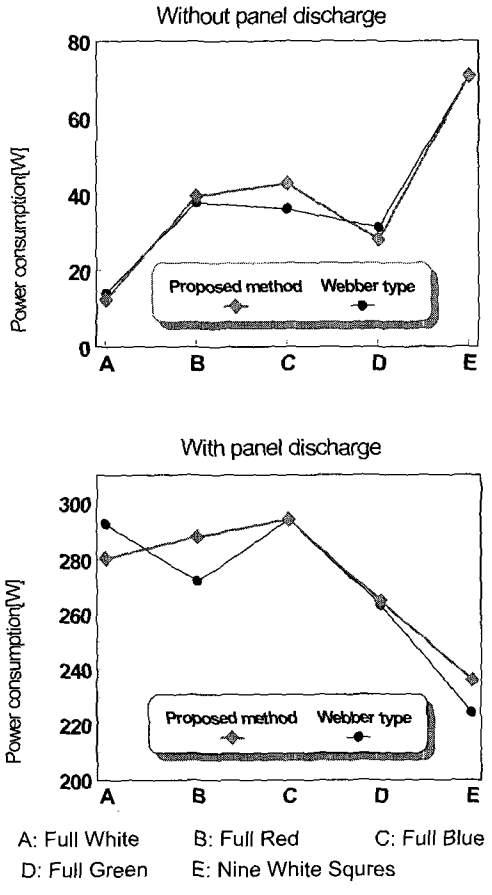
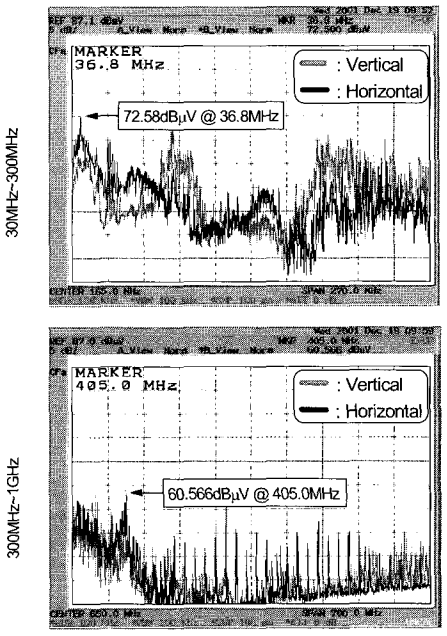
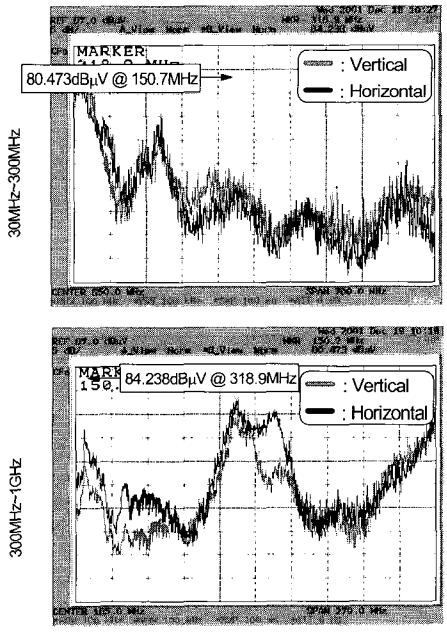


Fig. 11. Power consumption of PDP set with and without panel discharge at V_s=165V.



(a) CIM



(b) Series resonant method

Fig. 12. EMI comparisons between two methods.

7. Conclusions

In this paper, new concept of energy recovery using current injection method(CIM) is proposed and verified with 42 inch PDP panel. Experimental results show that with the help of the build-up inductor current just prior to invert the panel polarity, zero-voltage-switching of switches can be achieved regardless of the parasitic resistance and it reduces the EMI caused by the surge current. Prototype driver circuit produces stable light and sustain voltage waveforms while it has a desirable characteristic that power loss does not fall behind that of series resonant method. This concept can be applied to parallel resonant driver and address recovery circuit as well as series resonant driver.

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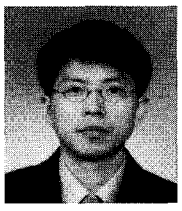

Jun-Young Lee was born in Seoul, Korea, on October 3, 1970, He was received the B.S. degree in Electrical Engineering from Korea University, Seoul, Korea, in 1993. M. S. and PH. D degree in Electrical Engineering from Korea Advanced Institute of Science and Technology (KAIST), Taejon, Korea, in 1996 and 2001 respectively. He was currently working for Samsung SDI as a manager. His research interests are in the areas on power electronics which include AC/DC PFC converter topology design, modeling and soft switching techniques and PDP drive system.

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