STI 채널 모서리에서 발생하는 MOSFET의 험프 특성

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The MOSFET Hump Characteristics Occurring at STI Channel Edge

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Abstract

An STI(Shallow Trench Isolation) by using a CMP(Chemical Mechanical Polishing) process has been one of the key issues in the device isolation[1]. In this paper we fabricated N, P-MOSFET to analyze hump characteristics in various rounding oxidation thickness(ex : Skip, 500, 800, 1000Å). As a result we found that hump occurred at STI channel edge region by field oxide recess, and boron segregation(early turn on due to boron segregation at channel edge).

Therefore we improved that hump occurrence by increased oxidation thickness, and control field oxide recess(≤ 20nm), wet oxidation etch time(19HF, 30sec), STI nitride wet cleaning time(99HF, 60sec+P 90min) and gate pre-oxidation cleaning time (U10min+19HF, 60sec) to prevent hump occurring at STI channel edge.

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I. Introduction

With device scaling down to sub-quarter micron (0.25um) class, the STI technology becomes a key method to realize high density DRAM[2][3]. Recently, STI technology have paid much attention on the surface roughness during CMP(Chemical Mechanical Polishing) or etchback process to planarization and void-free gap filling in the narrow space. Also the electrical characteristics of the nMOSFETs with STI structure strongly depend on the corner shape of trench isolation and trench gap filling dielectric materials[4]. When the gate is biased, the field lines from the overlapping region are focused by the edge geometry of the channel. Thus, at the edges of the channel, an inversion layer is formed at lower voltages than at the center region. As a result, less voltage bias overall must be applied to the gate to invert the channel across its full width. Also, a corner parasitic MOSFET in parallel with the main device is produced. The parasitic device turns on at voltages lower than channel center region, resulting in a hump in the drain current vs gate voltage curve[5]. Thus, the parasitic device increases the subthreshold leakage current of the active device. Sharp corners and gate oxide thinning lead to high electric field at the corners and produce hump characteristics in I-V curve, higher off-current, reverse narrow channel effect[6-9].

In this paper we find that threshold voltage shift increased drastically with increasing field oxide recess and decreasing oxidation thickness which exposes the top trench corners. The Vt of this edge device also depends on the geometric factors, such as the gate wrap-around, corner radius, sidewall corner angle, and wet cleaning time etc. In order to eliminate the hump effect, we carried out the experiment on the various oxidation thickness.

II. Experimental

Buffer oxide and Si_3N_4 layer were deposited and etched the field area for active area definition. Trench etching was performed(in depth=3000Å) after thin Si3N4 layer was etched. Slight oxidation of trench sidewall was formed(1050℃, 100Å) to eliminate the defect which might be occurred during the trench etching step. Filling the trench gap with HDP(High Density Plasma) oxide, and densification at high temperature, then CMP was carried out for planarization. Si_3N_4 and pad oxide were removed by 99HF 60 +Phorporic acid 75′ and U10′+19HF 45 , respectively. Next, oxidation was performed by with the following conditions; 1)skip, 2)500Å, 3)800Å and 4)1000Å to analyze the hump

<Table 1> The process of transistor

	NMOS	PMOS
Channel I/I	B, 20KeV, 2.0E12/cm^2	BF2, 40KeV, 6.5E12/cm^2
Gate Oxide	70nm	
Gate	Poly/Wsix/CAP HLD/Nit structure	
LDD sidewall	Si_3N_4(65nm)	
Blanket I/I	P, 2.0E13/cm^2	
P-type Halo I/I	B,4.0E12cm^2*300	-
Deep S/D I/I	As, 3.0E15/cm^2	BF2, 2.5E15/cm^2
RTA Anneal	950℃, 60sec	

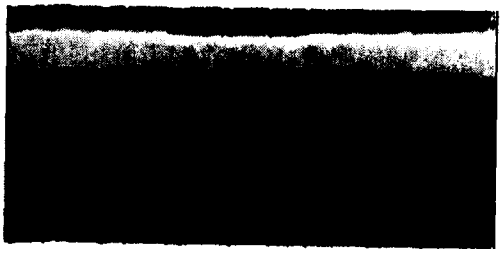
effect. Finally NMOS, PMOS transistor were formed. The fabricated transistor has 7.0nm thin gate oxide. The gate electrode was patterned by KrF lithography. Then 650Å Si3N4 sidewall spacer was formed. Table1 shows the detailed process of transistor fabrication.

III. Results and Discussions

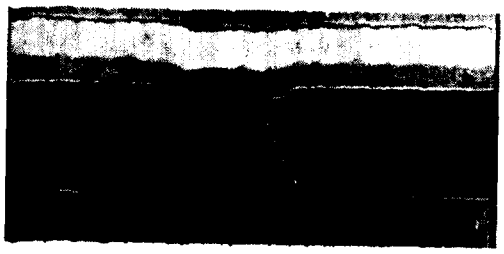
Fig1 shows the STI top corner profile of rounding oxidation after HDP oxide CMP process. Round oxidation was performed by dry oxidation process at 1100℃ high temperature. Dry oxidation effectively rounds off the STI bottom, sidewall and top corner (dry oxidation slower than wet oxidation). As shown in Fig1, active area is flat and edge junction edge with field shows negative steep slope when the round oxidation is skipped. When rounding oxidation is performed steep slope at top corner disappears and increases the rounding effect. But bird's beak encroachment occurred at central region. Fig2 represented the dimension of STI section((a) active area in silicon surface, (b) active width from surface 300Å, (c) STI depth, (d) remain oxide thickness from top to bottom). In this fig2 we can observed that from (a) to (b) does not dramatically difference. But (c) and (d) values are increased by increasing rounding oxidation thickness, and STI oxidation pre-cleaning, gate oxidation pre-cleaning time. So we must control the rounding oxidation thickness, etch time and pre-cleaning time to get optimal oxide recess.

(a) Rox=Skip

(b) Rox=500Å

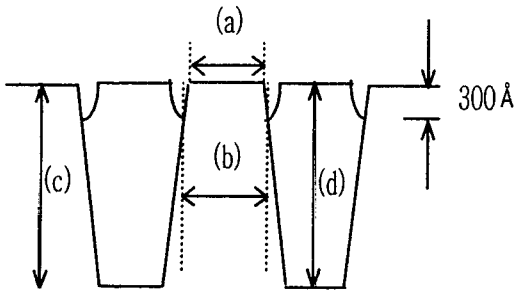


(c) Rox=800Å



(d) Rox=1000Å

<Figure 1> STI top corner profile with various rounding oxidation(SEM image)

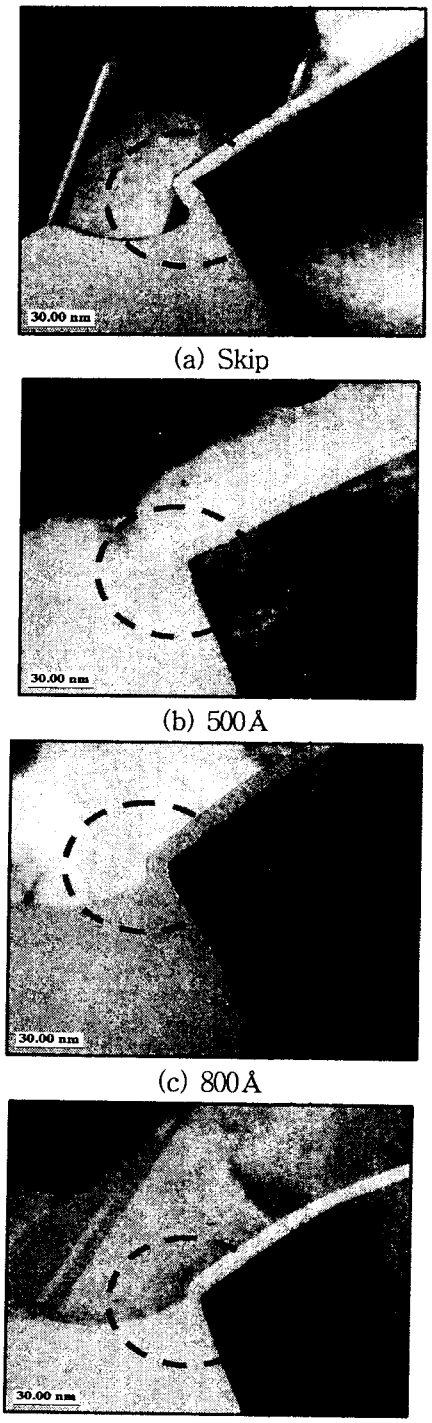


<Figure 2> Cross section of STI

<Table 2> Dimension values of STI rounding oxidation

Items	skip	500Å	800Å	1000Å
(a)	1800Å	1850Å	1750Å	1650Å
(b)	1900Å	2000Å	1900Å	1800Å
(c)	3050Å	2950Å	3000Å	3000Å
(d)	2950Å	3000Å	3100Å	3250Å

Fig 3 shows TEM cross section with various oxidation process. When rounding oxidation is skipped, profile is very sharp at STI top corner. When oxidation thickness is increased, steep top corner profile is disappeared. In this experimental we evaluated following that ; 1)hump effect of subthreshold Id-Vg, with channel widths variation, gate oxide Qbd of STI, and junction leakage to confirm top corner rounding profile. Fig4 shows the characteristics of MOS transistor subthreshold curve. In this figure we can observed hump effect by applied back-bias to substrate(Vbb=0~-2V). That is, hump phenomena does not observed when substrate bias is zero. But hump occurred only rounding oxidation skip structure except for rounding oxidation performed.



(a) Skip

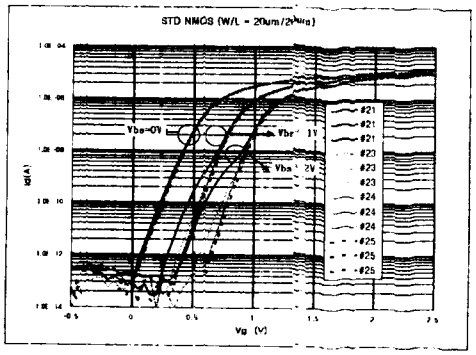
(b) 500Å

(c) 800Å

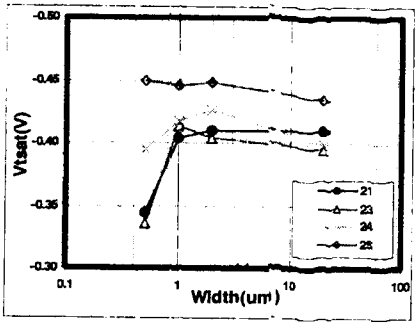
(d) 1000Å

<Figure 3> STI top corner profile with various rounding oxidation(TEM image)

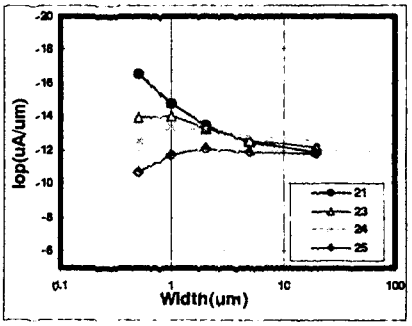
These hump effect implied that electric field concentration exist in channel edge from source to drain direction (parasitic transistor exist in parallel with one transistor in which has different Vth co-existence two-transistor). With increasing substrate bias, hump was occurred due to increased depletion region width in surface and threshold voltage. Hump was occurred when the gate electric field affect on channel top edge profile. When rounding oxidation was performed, we can observed hump effect was disappeared with applied substrate bias(especially, rounding oxidation thickness =800,1000Å).



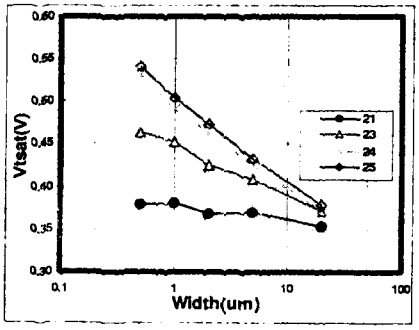
<Figure 4> Subthreshold characteristics with various rounding oxidation(Vbb=0~-2V)



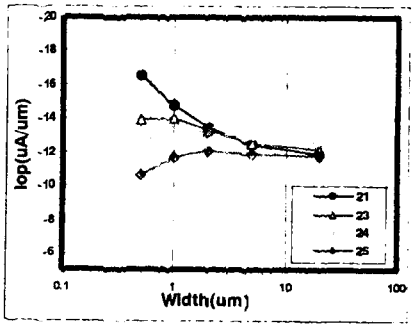
(a) Vtsat(PMOS)



(b) Iop(PMOS)



(c) Vtsat(NMOS)

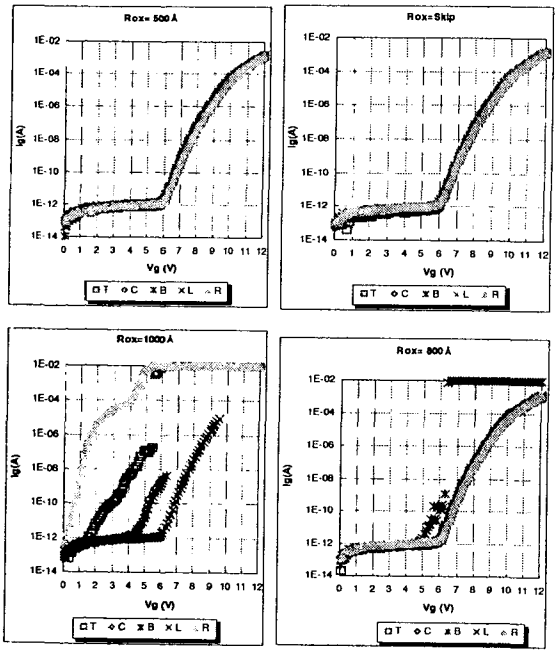


(d) Iop(NMOS)

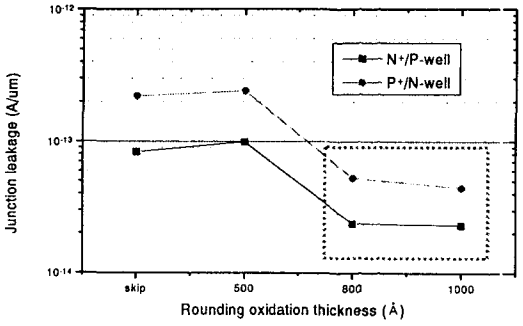
<Figure 5> Narrow width effect with various rounding oxidation(where,21:skip, 23:500Å, 23:800Å, 23:1000Å)

Fig 5 shows the variation of Vt and operation current with various channel widths. When skip the rounding oxidation INWE (Inverse narrow width effect) occurred due to gate electric field concentration. Meanwhile, Vtsat increased with increasing oxide thickness

and INWE occurred due to electric field relaxation effect by STI top corner rounding. These results advantageous on small-device Vt margin for narrow width effect but has decreased the device operation current. So we must decide rounding oxidation thickness to get optimal device spec. Fig6 shows Obd of gate oxide in various rounding oxidation. The Characteristics of gate oxide Qbd is good when rounding was skipped or rounding oxidation 500Å was carried out. But Qbd characteristics is not good 800Å and 1000Å. These reasons comes from follow that 1) mini bird' s beak was not removed completely at active area edge during post whole cleaning process, 2) due to profile of active and field. If field oxide higher than active silicon, Qbd characteristics is not good. So we could observed that field oxide higher than active height in fig1, 3)degradation was occurred by stress effect during rounding oxidation. So we could solved above mentioned items 1), 2) by control field oxide recess quantity. And item 3) solved by increasing rounding oxidation temperature to relaxation stress.



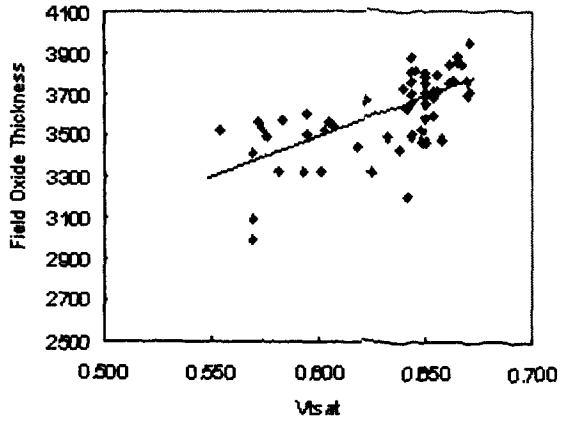
<Figure 6> Qbd of gate oxide with various rounding oxidation



<Figure 7> The characteristics of junction leakage with various rounding oxidation

Fig 7 represented the junction leakage of P+/N-well and N+/P-well with various oxidation thickness. When rounding oxidation was skip or 500Å was showed the same result. When rounding oxidation 800Å or 1000 Å, decreased leakage level about 1/3 than skip or 500Å due to thermal budget during rounding oxidation. As a result we found that optimal rounding oxidation dramatically improved the junction leakage, STI top corner profile, INWE and hump characteristics.

Fig 8 represented the threshold voltage of field oxide recess on wafer. Threshold voltage changed by field oxide recess. Threshold voltage low when field oxide was over recess. In this figure we found that threshold voltage depends on field oxide recess quantity. Thus it is very important field oxide recess control to get optimal threshold voltage.



<Figure 8> Threshold voltage with various rounding oxidation

4. Conclusions

In this paper we fabricated N, P-MOSFET to analyze hump characteristics in various rounding oxidation thickness (Skip, 500, 800, 1000Å). As a result we found that hump occurred at STI channel edge region by field oxide recess. We improved that hump occurrence by increased oxidation thickness, and control field oxide recess(≤20nm), wet oxidation etch time(19HF, 30sec), STI nitride wet cleaning time(99HF, 60sec + P 90min) and gate pre-oxidation cleaning time (U10min +19HF, 60sec) to prevent hump occurring at STI channel edge.

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