Fabrication of Field-Emitter Arrays using the Mold Method for FED Applications

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The typical mold method for FED (field emission display) fabrication is used to form a gate electrode, a gate oxide layer, and emitter tip after fabrication of a mold shape using wet-etching of Si substrate. However, in this study, new mold method using a side wall space structure was developed to make sharp emitter tips with the gate electrode. In new method, gate oxide layer and gate electrode layer were deposited on a Si wafer by LPCVD (low pressure chemical vapor deposition), and then BPSG (Boro phospher silicate glass) thin film was deposited. After then, the BPSG thin film was flowed into the mold at high temperature in order to form a sharp mold structure. TiN was deposited as an emitter tip on it. The unfinished device was bonded to a glass substrate by anodic bonding techniques. The Si wafer was etched from backside by KOH-deionized water solution. Finally, the sharp field emitter array with gate electrode on the glass substrate was formed.

Keywords : Mold, Field emitter array, BPSG, Anodic bonding

1. INTRODUCTION

Field emitter arrays (FEAs) are extensively studied for electron sources in vacuum microelectronic devices and field emission display[1-7]. In a field emitter device, the effiency of electron emission is largely affected by the device structure, material and shape of the emitter tip. Until now, there are two kinds of field emitter device, one is the diode type which is consist of cathode and anode, the other one is the triode type which is consist of cathode, gate and anode. In the triode structure, because the field for electron emission is applied to the gate near the cathode, it can be operated at even low voltage and emitting current is easy to control, so that is much developing. As an emitter material, metal, silicon, diamond, diamond like carbon and carbon material are widely used. In order to fabricate field emitter device, there are two methods. One is to develop new materials, the other is to modify the method presently used. In a new material developing division, the research is focus on carbon thin films. Fabricating sharp emitter tip is a key factor to improve properties of materials. The gate difficult made on the mold method by the conventional mold method. For example, even though the emitter tip can be fabricated, the end of tip can not be matched with the gate height[8,9]. Since the end of tip is higher than the gate eletrode, the electric field from the gate can not effectively drive[10]. The conventional mold method fabricated technique of combining anistropic Si wet etching. Other problem might be produced; the gate has to be made on the glass plate. In this study, we fabricated sharp emitter array to overcome the problems using the new mold method. We used the BPSG film to make sharp shaped tip. According to the feature of mold method, the gate oxide layer can be deposited with sharp shape, so the sharp emitter arrays could be fabricated by the mold method[11-15]. We fabricated the field emitter array of triode typed gate electrode prior to form the gate

electrode matched to height of the tip. The semiconductor processing was also used during tip formation.

2. EXPERIMENTAL

2.1 Fabrication method for transfer mold method

In this work, the sharp and uniformed field emitter array was fabricated by the new mold method using glass substrate instead of silicon substrate and semiconductor process was appied during tip fabrication. In order to expose tip and bond silicon substrate to glass substrate, the KOH solution was used, which can dissolve silicon substrate. The fabrication method of the field emitter tip is shown in Fig. 1. Firstly, the thick oxide layer was deposited with 300nm on the silicon substrates (5 inch n-type, respectively 5-8cm) by LPCVD method. 300nm thick poly-silicon as the gate eletrode material was deposited on the substrate. On the gate oxide layer, 500 nm thick TEOS oxide films were deposited. After that, the tip masks were patterned with optical stepper. And then, the oxide layer was etched step by step to form 1μm hole diameter[Fig. 1(a)]. On the structure, side wall space structure consist of multiple layers was formed by deposition and etching three times using the RIE(reative ion etaching) method [Fig. 1(b)]. However, a sharp shaped tip couldn't be obtained by this method. Secondly, the BPSG thin film was deposited on the gate oxide layer and then the oxide layer was formed with slope shape by the flow method at 950°C in order that the electrode material can be filled up well[Fig. (a')]. By the RIE method, after deposition and etching twice, the sharp shaped tip was formed[Fig. 1(b')]. The next processes are deposition and etching processes. n a plasma CVD reactor, the oxide layer was deposited by SiH_4, N_2O gas with 200nm thick. After that, in the reactor, etching was done by Ar gas in thickness of 100nm, by the repeated deposition and etching. As the edge of cross section became dull, the cross section of oxide layer had slope shape[Fig. 1(c)]. The following process is to adjust the height of gate electrode and field emitter tip. A supplementary deposition process was done by LPCVD method to add proper thick dieletric film[Fig. 1(d)]. On the designed mold, TiN as a field emitter tip was formed with 200nm thick by the deposition and then on the emitter tip, oxide layer was deposited with 1000nm thick, to protect the emitter tip when the silicon substrate was eroding in KOH solution [Fig. 1(e)]. The following process was to bond a pyrex glass to the oxide film by an anodic bonding technique [Fig. 1(f)]. In the bonded glass and silicon substrate (625μm thick), the 80% of silicon substrate was polished

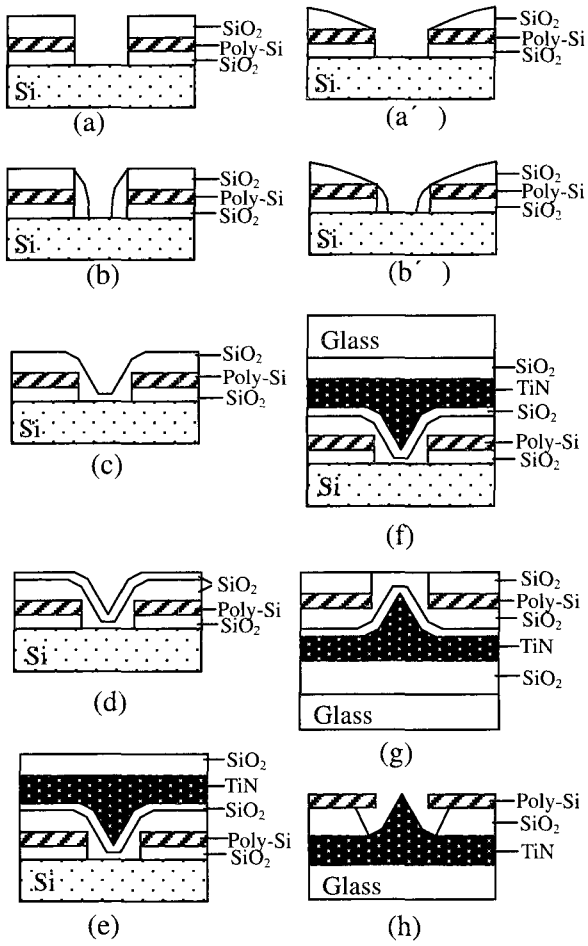

Fig. 1. Transfer Mold Process (a) etching after mask patterning[TEOS oxide deposition], (a') slope shape by the flow method[BPSG oxide deposition], side wall space strucrure by RIE (b) TEOS, (b') BPSG, (c) slope shape of the cross section, (d) oxide layer deposition by LPCVD, (e) oxide layer deposition after TiN deposition, (f) pyrex glass bond by anodic bonding, (g) Si substrate remove, (h) final process.

out. And then the remain of silicon substrate was eroded by KOH solution at 80°C for 2 hr[Fig. 1(g)]. As the last process, according to partially eroding oxide layer with HF solution, we exposed sharper emitter tips[Fig. 1(h)].

2.2 Technique of bonding a glass to a silicon substrate

In order to fabricate field emitter arrays with mold shape, the most important process is to bond a pyrex glass to the silicon substrate. In this work, we used the anodic bonding method for bonding a pyrex glass to the silicon substrate. The anodic mechanism of a silicon substrate and glass using a pyrex glass is similar to that of silicon and silicon using a general glass[9,16]. Fig. 2 shows the schematic diagram of the anodic bonding system which consists of heater, temperature controller

and DC voltage supplier. The temperature can be increased to 500°C and DC voltage can be increased to 3kV. The anode of voltage supplier is connected to the silicon layer and the cathode is connected to the pyrex glass layer.

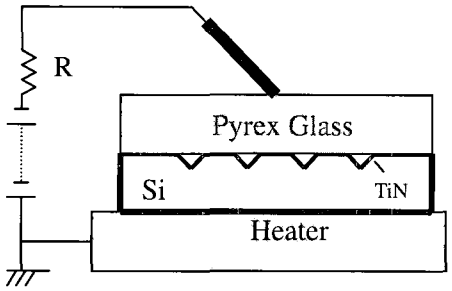

Fig. 2. The Schematic of Si-glass anodic bonding.

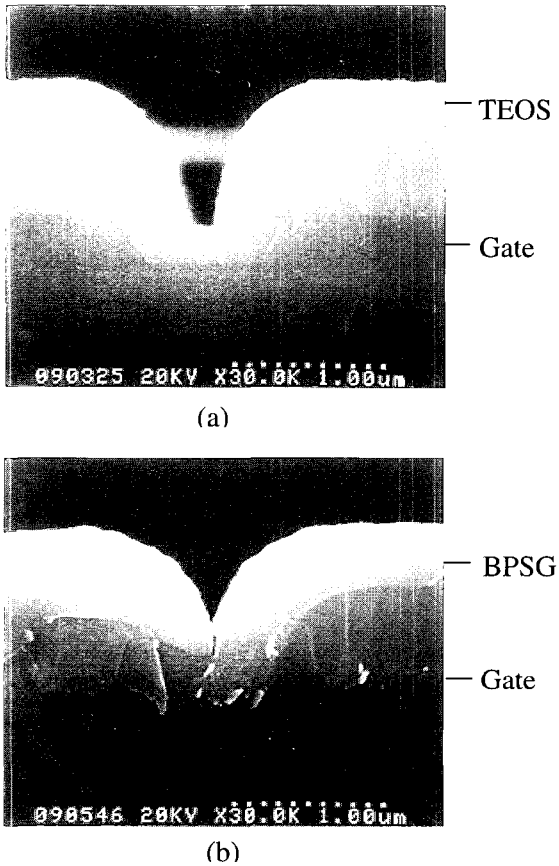

Fig. 3. SEM photographs of after mold formation by (a) TEOS, (b) BPSG

3. RESULTS AND DISCUSSION

The gate difficult made on the mold method by the conventional mold method. Even though the emitter tip can be fabricated, the end of tip can not be matched with the gate height[8,9]. Since the end of tip is higher than the gate eletrode, the electric field from the gate can not effectively drive[10]. The conventional mold method fabricated technique of combining anistropic Si wet etching. Other problem might be produced; the gate has to be made on the glass plate. In this study, we fabricated sharp emitter array to overcome the problems using the new mold method. As shown in Fig. 3, SEM images show that the final emitter tip shapes formed by etching and deposition repeatedly which were deposited on the mold types with TEOS and BPSG thin film as an oxide layer by means of the LPCVD method. First, using TEOS layer, as a result of repeated etching and deposition[Fig. 3(a)], the tip shape is formed to rectangular instead of sharp one and we could know that the end of tip was below the gate electrode. Even though oxide layers and gate electrode was deposited as different thicknesses instead of constant ratio, we got the same results. In order to fabricate a sharp shaped tip using above method, the side wall should have smooth slope, not rectangular one. In this work, we could finally obtain the sharp shape of tips with depositing BPSG layer instead of TEOS layer as an oxide layer in order to solve above problem. First of all, the BPSG thin film was annealed at a high temperature of 950°C and the oxide layer was formed to slant shape from rectangular one with approximate 45° slope[Fig. 1(b)]. The important result is that the gate oxide layer was formed to slant shape by annealing at high temperature after deposition of BPSG thin film and in fabrication of sharp shaped tips, the sides of hole had sharp shapes by etching the sides of wall. Therefore, the end of tip was made in the center of gate with deposition of the oxide layer. According to deposition thickness of BPSG thin film and variances of slope value of slant angle when annealed at high temperature, the height of tip and thickness of insulator layer are determined by the slope of angle and shape of slant. Before the gated emitter

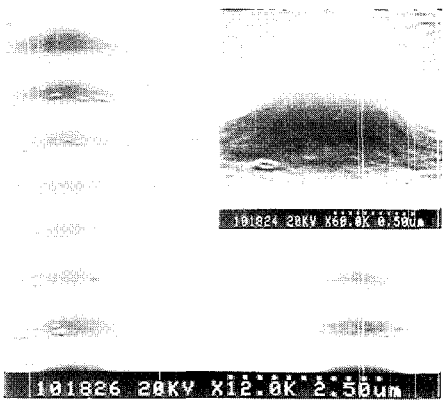

Fig. 4. SEM photographs of the emitter arrays before gate formation.

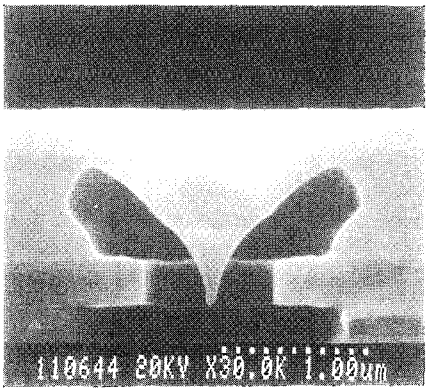

Fig. 5. SEM photographs of the TiN FEA cross section view of a single tip array.

fabricated, the distance between two tips is 5μm and the field emitter array are uniformly formed as shown in Fig. 4. Fig. 5 shows the cross section structure of TiN field emitter array which was fabricated by the mold method based on SEM photographs. The tips has a height of 1.07μm, and a tip-radius is about 358Å. The end of tip has sharp and stable structure. The surface of tip is rough. Next, in order to fabricate the field emitter array, one of important techniques is to bond glass to silicon substrate. In this work, we analysed the anodic bonding conditions based on bonding temperature, driving voltage, bonding time, material formed on the silicon substrate i.e. polysilicon, oxide layer and the thickness of TiN. The bonding rate was low due to the insufficient heat below 200°C in bonding temperature and above 400°C, the bonding rate was also low because the bonding areas were decreased as increasing of heat deformation by the difference of heat expansion coefficients between a glass and a silicon substrate. The change of thickness didn't affect to the current density streamed on the surface. Having similar current densities, bonding pressures became similar without being affected by oxidative layer, polysilicon and thickness of TiN. In other words, having similar current densities, the residual stress was more affecting factor in bonding glass and silicon deposited several materials. These results imply that the bonding is constantly deformed to parallel direction under same bonding pressure. In the bonding process, we knew that the most important factor which can affect to the ratio of bonding areas is the bonding temperature followed by bonding time, bonding pressure and DC voltage. And the best condition was 300°C bonding temperature, 500V bonding direct voltage (DC) and 10min bonding time.

4. CONCULSION

In the summary, we fabricated the field emitter arrays on the glass substrate, which was different from conventional method. After gate electrode and gate oxide layer were formed on a silicon substrate, BPSG thin film was deposited on it by LPCVD method. And then, by heating the substrate at high temperature, the gate oxide layer was formed to slant shape. By several deposition and etching processes, the mold for an emitter tip had sharp shape. After that, TiN was deposited as a tip material. While a pyrex glass was bonded to the silicon substrate by an anodic bonding technique, an oxide layer was deposited in order to protect tip material. Consequently, the silicon substrate was completely removed to expose a sharp tip. Finally, the sharp field emitter arrays that had gate electrodes were fabricated. It is easy to deposit a layer having a low work function by the new mold method. Also, the deposition layer can be formed thickly, and field emitter arrays that have good uniformity can be formed. It might be possible to make large-area panels by a bonding technique. It seems that this study needs more evaluation of the measurement of the emission.

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