Emission Characteristics of 0.7″ Monochrome MOSFET-Controlled Field Emission Displays in a High Vacuum Chamber

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Abstract

MCFEDs (MOSFET-Contoolled Field Emission Displays) were fabricated to evaluate the validity of MCFEA for display application. The electrical properties of FEAs (Field Emitter Arrays), HVMOSFETs (High-Voltage MOSFETs), and MCFEAs (MOSFET-Controlled Field Emitter Arrays) were measured. The extraction gate voltage of the FEAs to obtain the anode current of 10 nA/tip was around 71 V. The breakdown voltages of the HVMOSFETs were above 81 V for all the samples. The I-V characteristics of the MCFEAs showed that the emission currents of the FEAs were well controlled depending on the control gate voltages of the HVMOSFETs. To avoid the harmful effects during the packaging process, the performance of the MCFEDs was evaluated in a high vacuum chamber. The emission images of the MCFEDs were controlled through very-through operation. From the comparison with a conventional FED, it was proven that the poor uniformity of FED could be improved through the integration with HVMOSFET.

Keywords : field emission display, MCFED, uniformity.

1. Introduction

Since the development of the first field emission display (FED), was many attempts have been made to overcome its poor uniformity and stability[1, 2]. As one of the approaches, an active device controlled field emitter array (FEA) was proposed by Ting, et al [3]. Integration with various active devices was also expenmented [4-7]. Most of all, the integration with a metal-oxide-semiconductor field effect transistor (MOSFET) were intensively researched because of its well-developed fabrication process [6-9]. The field emitter with a MOSFET has its own advantages, i.e., the good stability due to superior current controllability of a MOSFET and the good reliability due to the prevention of disruptively excessive emission currents. In addition, if it is used as a pixel of a FED, cheap driver circuit is applicable because the emission current is controlled by the gate of a MOSFET.

Lee, et al. proposed and fabricated a MOSFET-controlled field emitter array (MCFEA) with a high voltage MOSFET (HVMOSFET) that is composed of two-threshold voltage region to improve the breakdown voltage and the current controllability [7-9]. The fluctuation and the stability of the emission current were remarkably improved. These electrical performances were good enough to use the electron sources in an FED.

In this paper, it is reported that 0.7″ monochrome FEDs with MCFEAs as pixels shows better performances in comparison with a conventional FED.

2. Fabrication

The fabrication sequence of a MCFEA is shown in Fig. 1. The starting material was a boron-doped (100)-oriented silicon wafer with low doping concentration of $5\times10^{14}/cm^3$, which is chosen to increase the junction breakdown voltage. The n^+-well was formed by phosphorus diffusion. A 52 nm-thick nitride film was

Manuscript received August 18, 2001; accepted for publication September 12, 2001.
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Table 1. The process conditions for V_T adjustment implantation and gate oxidation.

Wafer	V_T implantation condition	Gate oxidation condition
A	B^+, 40 keV, 2×10^{12} ions/ cm^2	Dry, 950 °C, 38 min. 30 sec. (250 Å)
B	B^+, 40 keV, 1×10^{12} ions/ cm^2	Dry, 950 °C, 38 min. 30 sec. (250 Å)
C	B^+, 40 keV, 1.5×10^{12} ions/ cm^2	Wet, 1000 °C, 12 min. 30 sec. (1000 Å)
*D	B^+, 40 keV, 1.5×10^{12} ions/ cm^2	Wet, 1000 °C, 12 min. 30 sec. (1000 Å)

* Sample D was implanted after gate oxidation and annealed at the temperature of 1000 °C for 10 min.

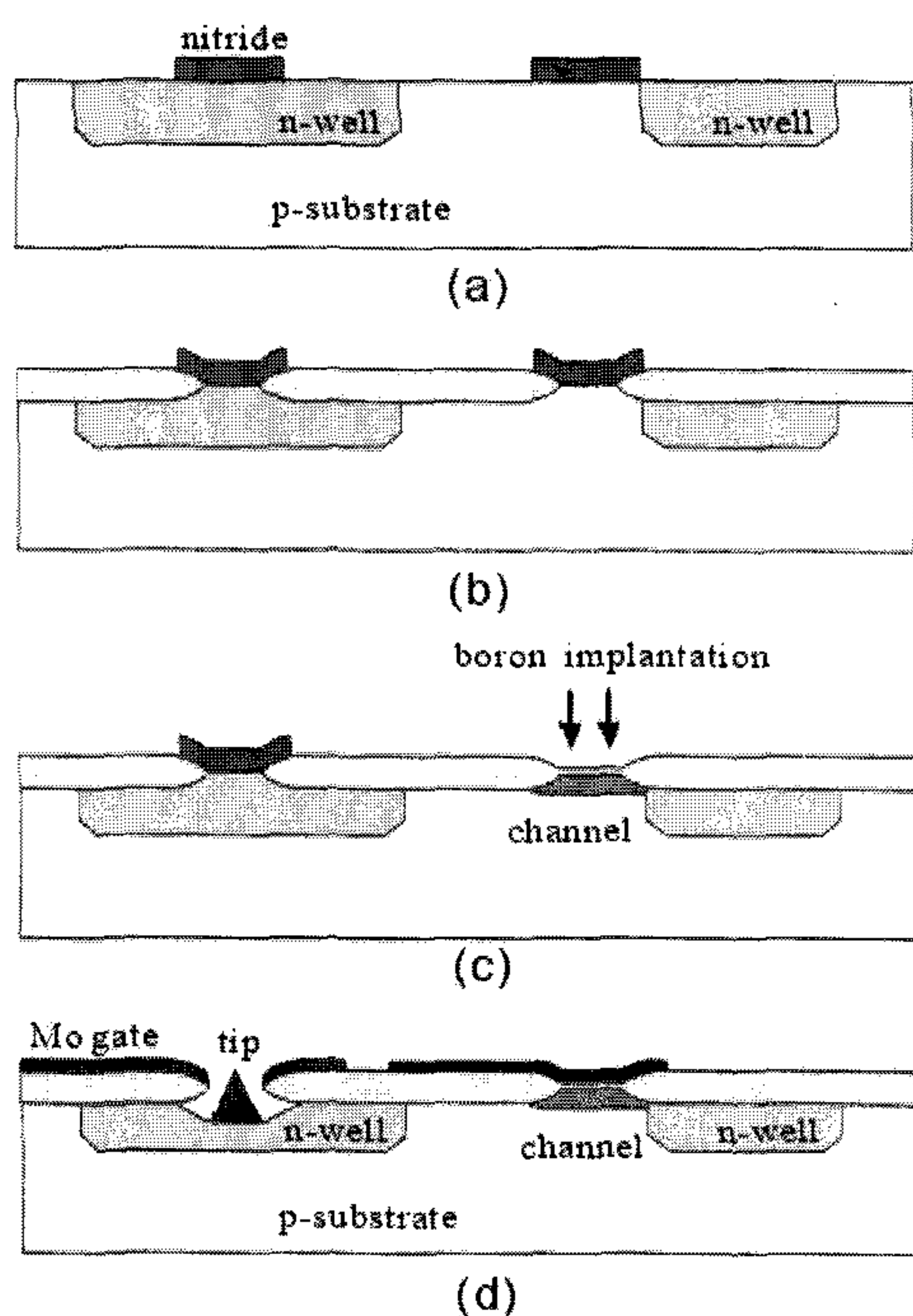
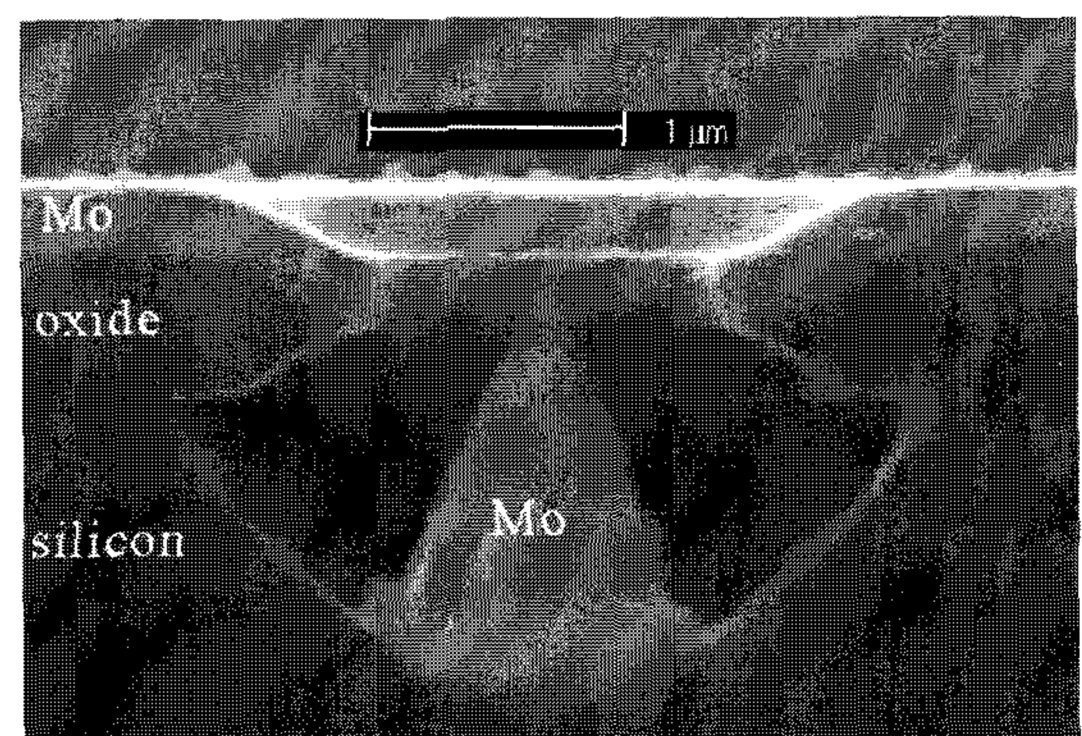
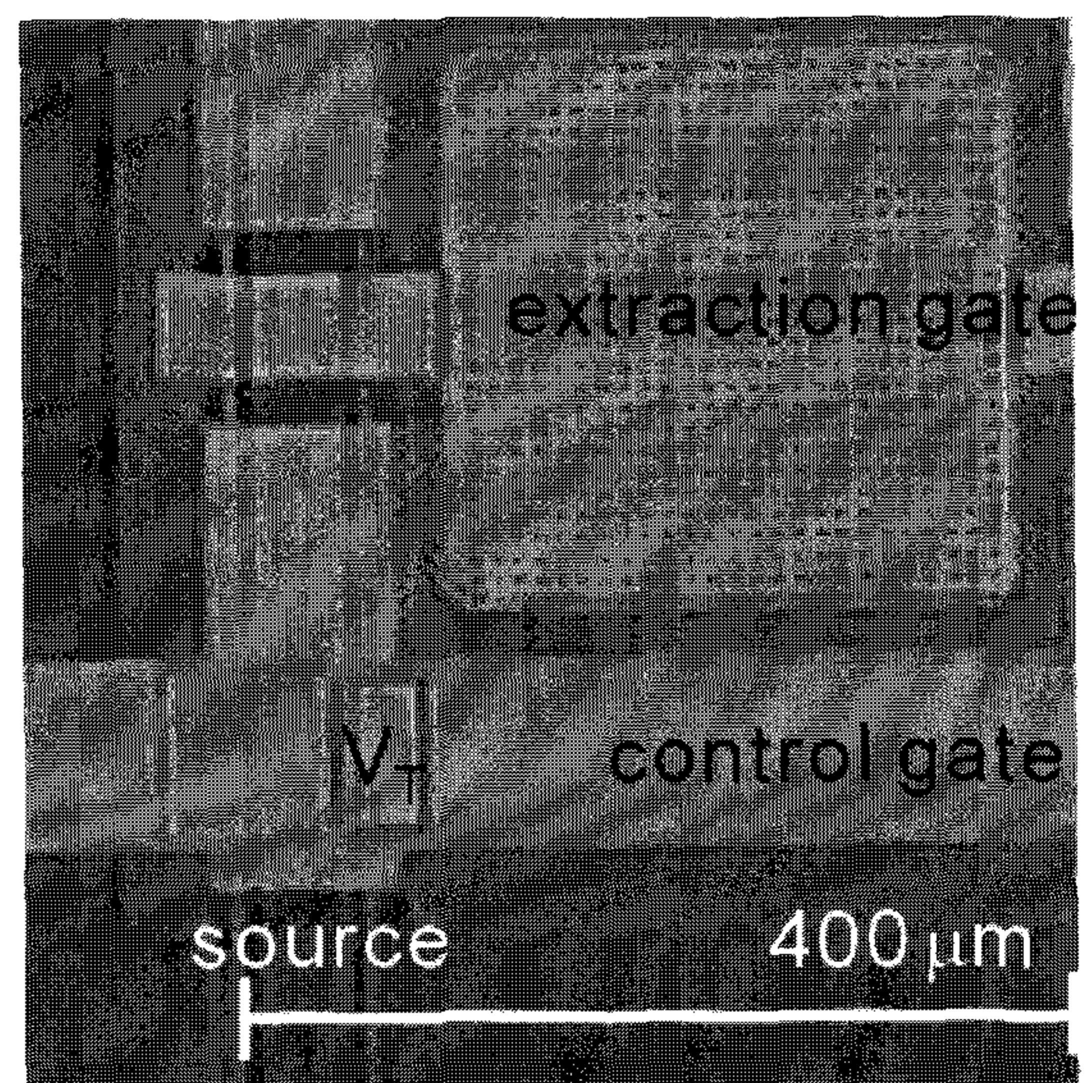


Fig. 1. The process sequence of a MCFEA; (a) well formation, (b) field oxidation, (c) V_T adjustment implantation and gate oxidation, and (d) tip formation.

deposited by low pressure chemical vapor deposition (LPCVD) and patterned into the discs and the active region (Fig. 1 (a)). The wafer was locally oxidized in wet O_2 ambient at 1000 ℃ for 120 min. The thickness of the grown oxide on the n^+-well was 640 nm whereas the thickness on the p-substrate was 570 nm (Fig. 1 (b)). Then, the nitride film was patterned to expose the channel region of the HVMOSFET. Borons were implanted to adjust the threshold voltage of the HVMOSFET. Oxidation was done to grow a gate oxide of MOSFET (Fig. 1 (c)). The process conditions for threshold voltage (V_T) adjustment implantation and gate oxidation for each wafer are summarized in Table 1. The nitride layer was removed by reactive ion etching (RIE) and the exposed silicon was isotropically etched by RIE



(a)



(b)

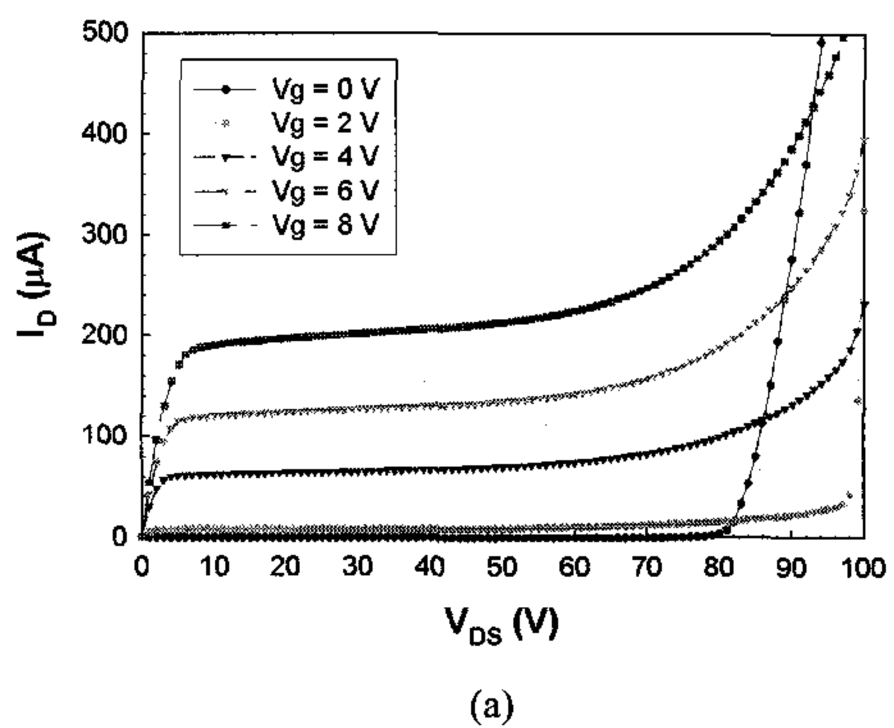
Fig. 2. (a) The cross-sectional view of a fabricated field emitter and (b) the top view of a fabricated MCFEA.

using SF_6 to form gate holes, followed by the conventional Spindt process. The gate metal, the parting layer, and the tip metal were deposited by electron beam evaporator successively. Finally, the parting layer and the overlying structure were lifted-off (Fig. 1 (d)).

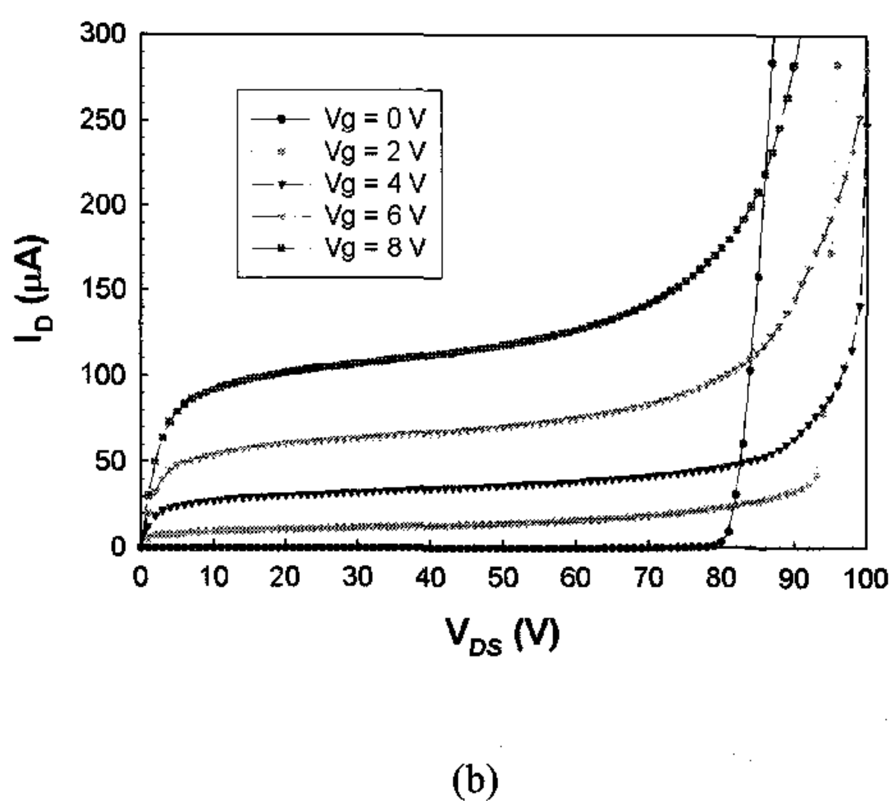
Fig. 2 shows the cross-sectional view of a field emitter and the top view of a fabricated MCFEA pixel. The gate hole diameter of the emitter is 1.25 μm. The cathode of the field emitter acts as the drain of the HVMOSFET. The channel is composed of two regions, the low and high threshold voltage regions. The low threshold region determines the breakdown voltage of the HVMOSFET while the high threshold voltage region determines the threshold voltage of it [9].

3. Results and Discussion

Electrical measurements of HVMOSFETs were performed with a HP 4155B parameter analyzer. Fig. 3. shows the typical drain current (I_D)-drain voltage (V_{DS}) characteristics of the HVMOSFETs with the gate oxide thickness of 250 and 1000 Å. The breakdown voltages were higher than 81 V for both cases. However, considering the flatness of the saturation region in Fig. 3, the HVMOSFET with the thinner gate oxide has better current controllability.



(a)



(b)

Fig. 3. The typical I_D-V_{DS} characteristics of HVMOSFETs with the gate oxide thickness of (a) 250 Å and (b) 1000 Å. The breakdown voltages were higher than 81 V for both cases.

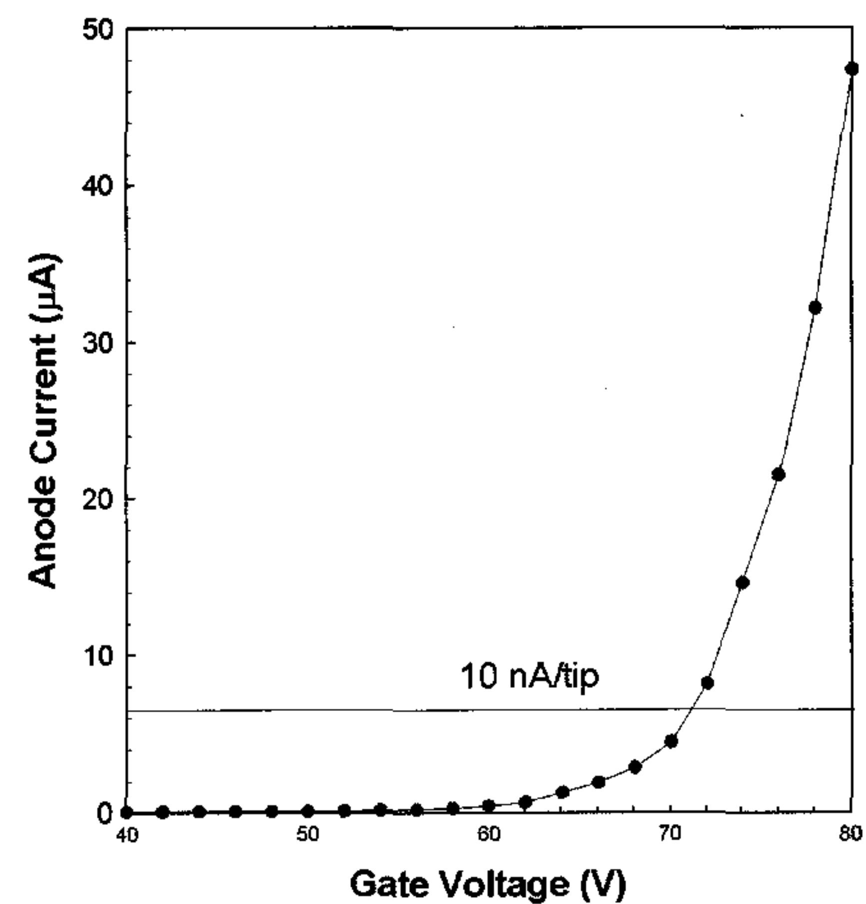
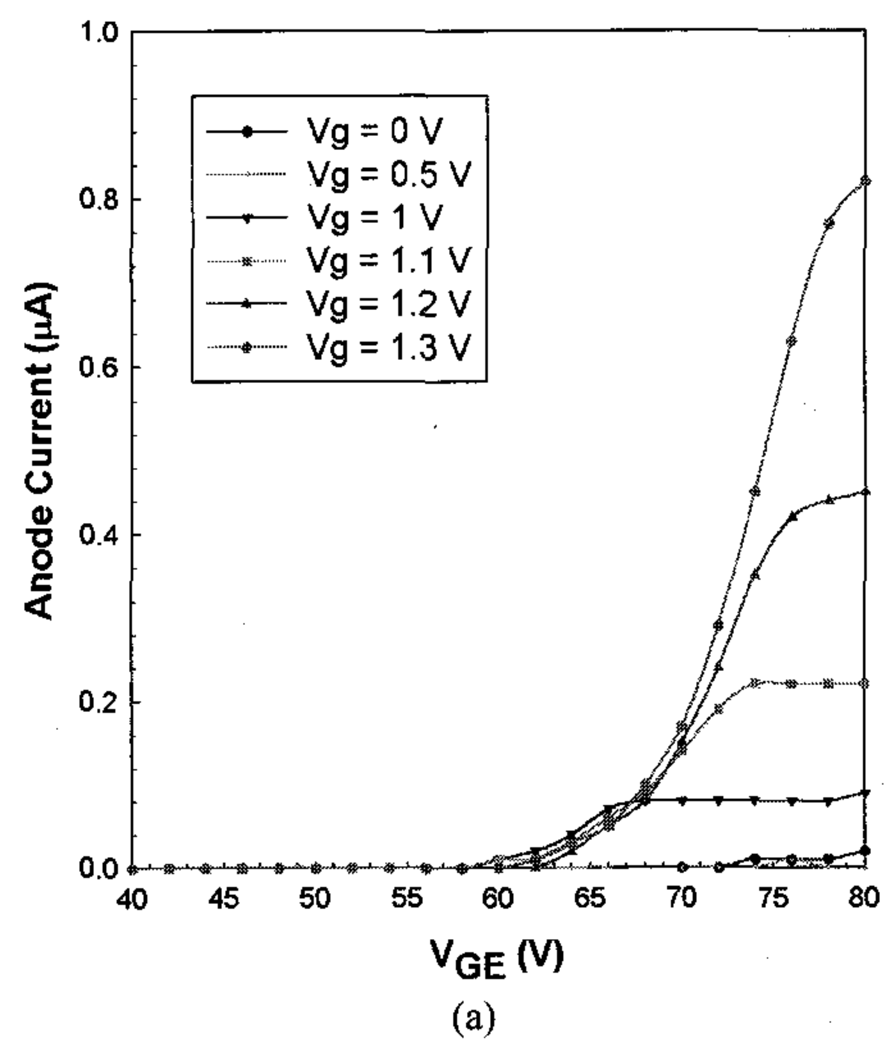
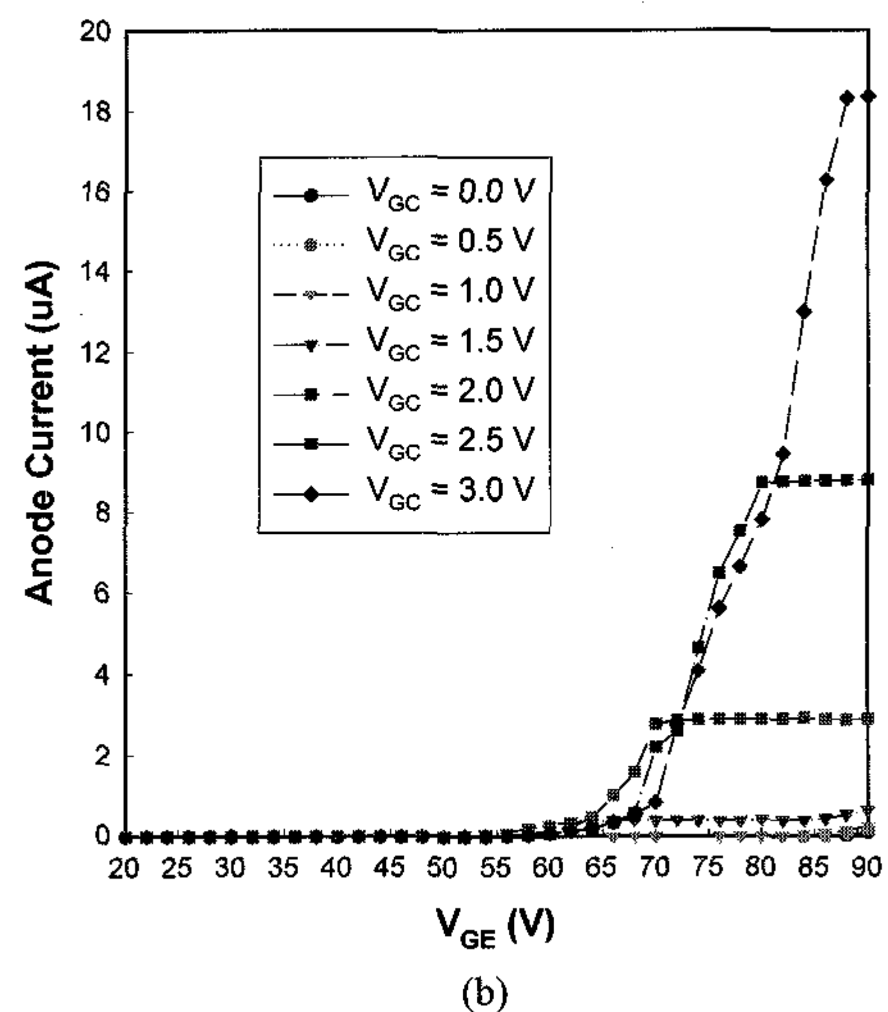


Fig. 4. The I-V characteristics of a FEA with 625 tips. The gate voltage to obtain the anode current of 10 nA/tip was around 71 V.

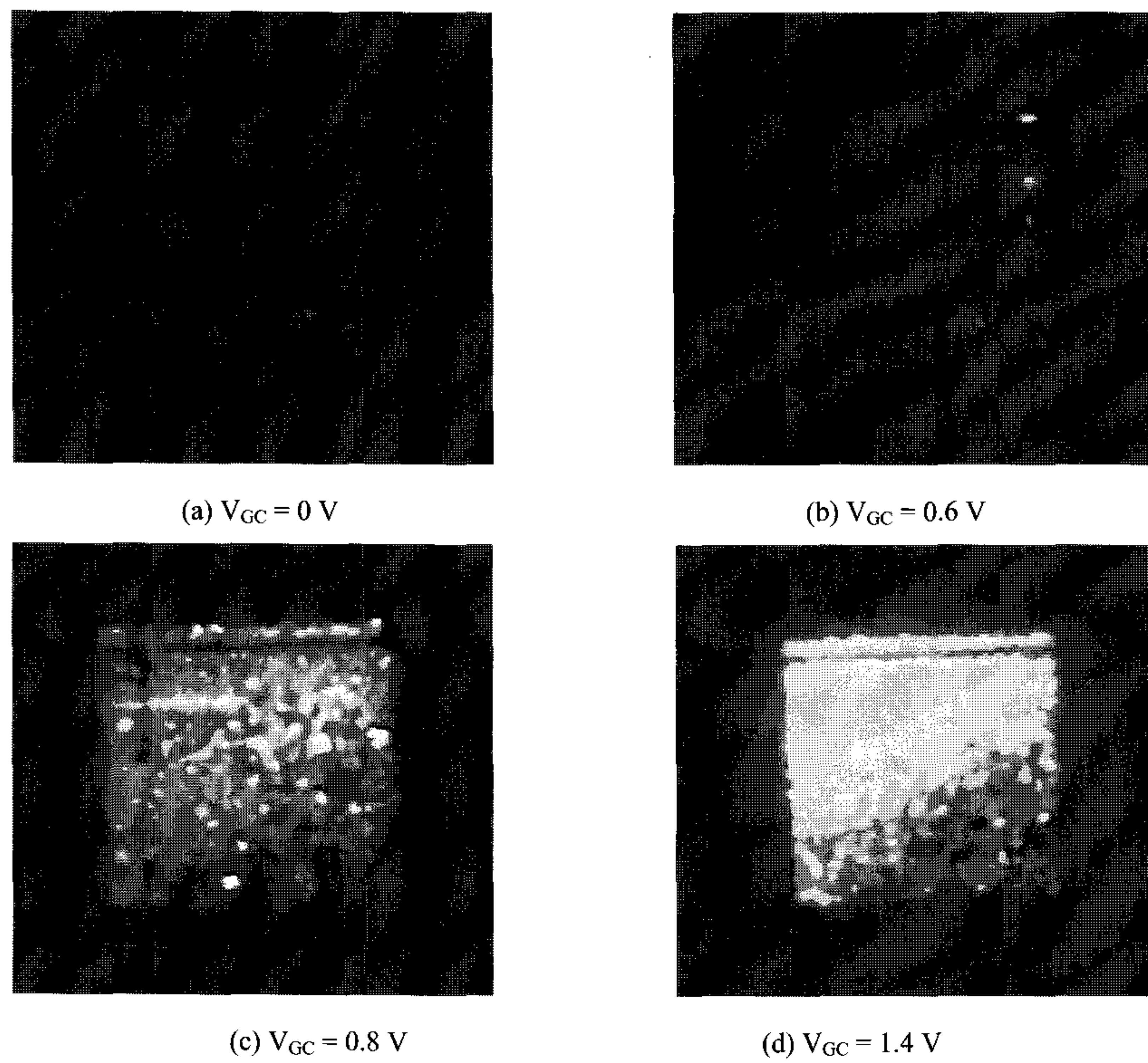


(a)



(b)

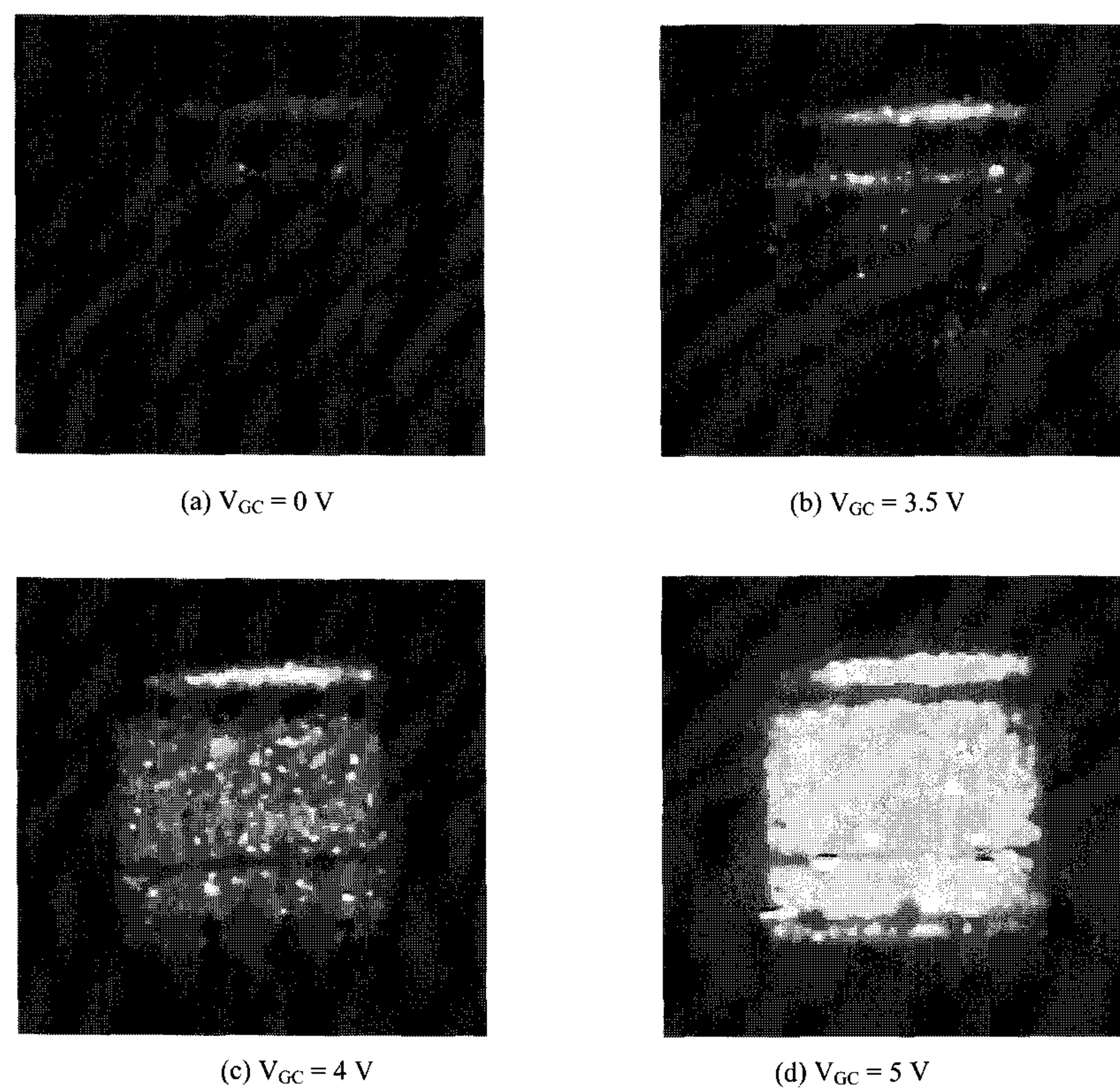
Fig. 5. The I-V characteristics of MCFEAs fabricated in (a) the wafer A and (b) C. The I-V curves of the MCFEAs show the saturations of emission currents.



(a) $V_{GC} = 0$ V (b) $V_{GC} = 0.6$ V

(c) $V_{GC} = 0.8$ V (d) $V_{GC} = 1.4$ V

Fig. 6. The emission images of a MCFED fabricated in the wafer B depending on the control gate voltages under the extraction gate voltages of 80 V and the anode voltage of 400 V.



(a) $V_{GC} = 0$ V (b) $V_{GC} = 3.5$ V

(c) $V_{GC} = 4$ V (d) $V_{GC} = 5$ V

Fig. 7. The emission images of a MCFED fabricated in the wafer D depending on the control gate voltages under the extraction gate voltages of 75 V and the anode voltage of 400 V.

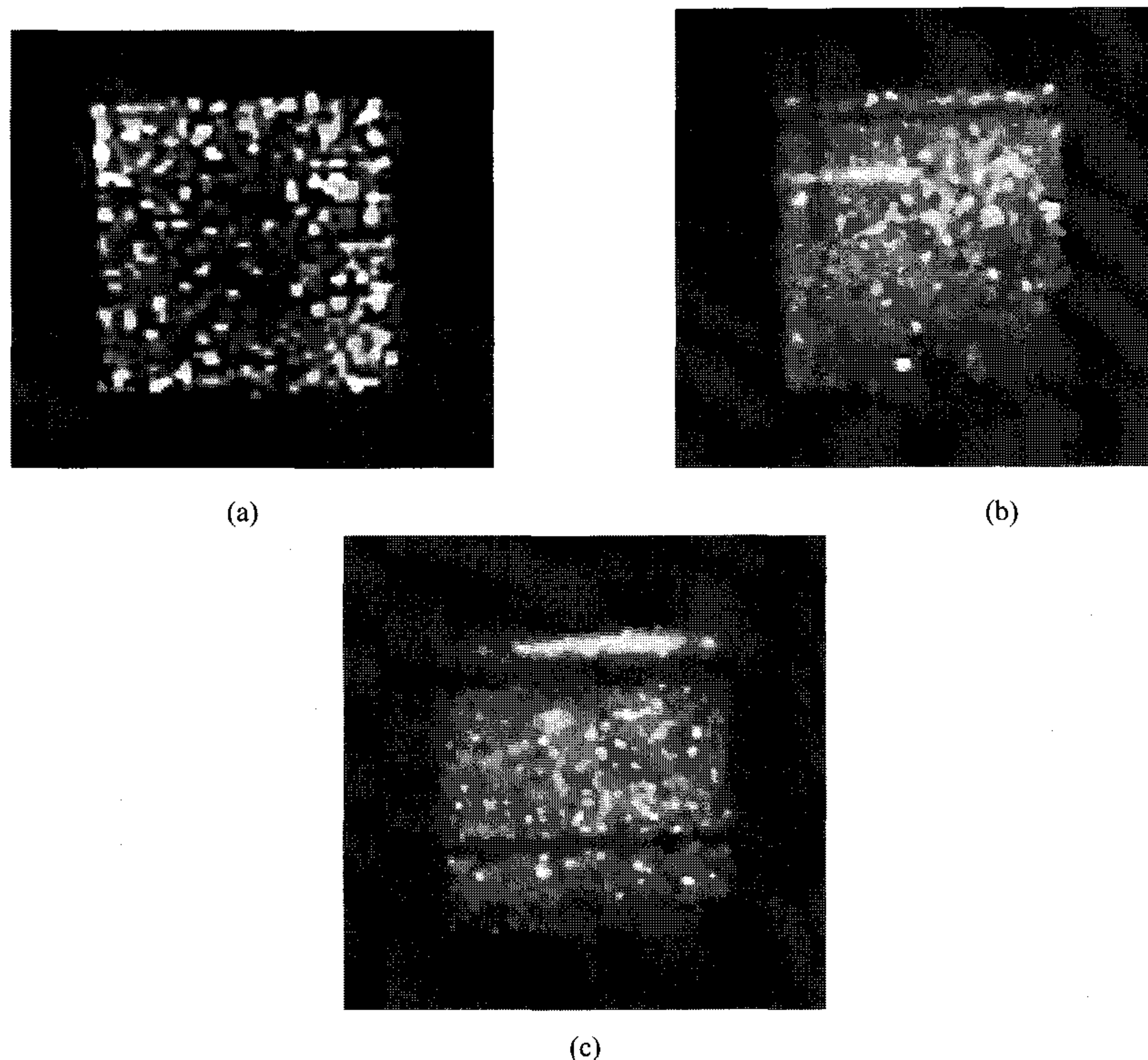


Fig. 8. (a) The emission image of a conventional FED at the gate voltage of 48 V and the anode voltage of 400 V. (b) The emission image of a MCFED fabricated in the wafer B at the extraction gate voltage of 80 V, the control gate voltage of 0.8 V, and the anode voltage of 400 V. (c) The emission image of a MCFED fabricated in the wafer D at the extraction gate voltage of 75 V, the control gate voltage of 4 V, and the anode voltage of 400 V.

Electrical measurements of FEAs and MCFEAs were performed in an ultra high vacuum (UHV) chamber at a pressure of 2.3×10^{-9} Torr. The chamber was baked at 250 °C for 10 hours before the measurements were taken to remove contaminants. The cathode, the source of HVMOSFET in the case of MCFEA, was grounded, the anode was biased at + 400 V, and positive voltages were applied to the gates. The distance between the anode and the gate was maintained at about 1 mm. The I-V characteristics of a FEA and MCFEAs are shown in Figs. 4 and 5, respectively. The gate voltage to obtain the anode current of 10 nA/tip is around 71 V in the FEA. The I-V curves of the MCFEAs show the saturations of emission currents, meaning that the emission current of the FEAs is well controlled by the HVMOSFETs. Considering the off current of about 10 nA in the worst case, the on/off ratio of emission current above 1000 is obtainable using the device with the control gate oxide thickness of 1000 Å at the extraction gate voltage of around 82 V. By increasing the breakdown voltage of the HVMOSFET or decreasing the turn-on voltage of the FEA, the on/off ratio can be improved. However, the off current of 10 nA can make a dim image on the phosphor. This current should be suppressed lower than 100 pA.

To evaluate the uniformity of the display, the MCFEDs fabricated in the wafer B and D were operated in a high vacuum chamber at a pressure of about 5×10^{-7} Torr. The threshold voltages of HVMOSFETs fabricated in wafers B and D weres 0.5 V and 2.8 V, respectively. ITO glass with ZnO:Zn or ZnS:Cu phosphor was prepared as the anode plate. The gap between the cathode and the anode plate was sustained by a 1.8 mm-thick glass spacer.

The emission images of the MCFEDs for control gate voltages were shown in Figs. 6 and 7. As the control-gate voltage was increased, the brightness of the display also proportionally increased. The emission images of Figs. 6(c) and 7(c) are uniform except for the defect area that originated from fabrication process and phosphor preparation. These results show the precise operation of the MCFED. Fig. 6(d) and 7(d) show the images in the partially controlled region in which the emission current level of the FEA is lower than the saturation current level of the HVMOSFET. The bright

images due to high emission currents are shown in the figures. But, there are no arcing or flickering due to the disruptively high current because the control gate of the HVMOSFET limits the maximum emission currents.

Fig. 8 shows the emission image of a conventional FED and MCFEDs operated in a vacuum environment. The conventional FED has the same pixel number and field emitter structure except the gate hole size of 1.1 μm, which is relatively smaller than that in the MCFED. As shown in the figure, the MCFEDs have more uniform images among the pixels than that of the conventional FED. Thus, it was confirmed that the integration with MOSFETs can compensate for the poor uniformity of FEAs. If the process is optimized, a good performance can be achieved.

4. Conclusions

FEAs, HVMOSFETs, and MCFEAs were fabricated and characterized. The gate hole diameter of the FEA was 1.25 μm. The gate voltage to obtain the anode current of 10 nA/tip was around 71 V in the FEAs. The breakdown voltages of the HVMOSFETs were higher than 81 V for all the samples. Considering the flatness of saturation region, the HVMOSFET with a thin gate oxide showed better current controllability. The I-V curves of the MCFEAs show the saturations of emission currents, indicating that the emission currents of the FEAs were well controlled by the HVMOSFETs. MCFEDs were fabricated and their evaluations were carried out in a high vacuum chamber. The brightness of the MCFEDs was controlled by the control-gate voltage of the HVMOSFET. The comparison with a conventional FED confirmed the superiority of the MCFED. But, more works on process optimization are required.

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