Journal of the Korean Ceramic Society
Vol. 38, No. 9, pp. 782~786 2001.

Effects of Ti and TiN Capping Layers on Cobalt-silicided MOS Device Characteristics in Embedded DRAM and Logic

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(Received July 20, 2001; Accepted September 5, 2001)

ABSTRACT

Cobalt silicide has been employed to Embedded DRAM (Dynamic Random Access Memory) and Logic (EDL) as contact material to improve its speed. We have investigated the influences of Ti and TiN capping layers on cobalt-silicided Complementary Metal-Oxide-Semiconductor (CMOS) device characteristics. TiN capping layer is shown to be superior to Ti capping layer with respect to high thermal stability and the current driving capability of pMOSFETs. Secondary Ion Mass Spectrometry (SIMS) showed that the Ti capping layer could not prevent the out-diffusion of boron dopants. The resulting operating current of MOS devices with Ti capping layer was degraded by more than 10%, compared with those with TiN.

Key words : Cobalt silicide, Capping layer, Dopant, Metal-Oxide-Semiconductor Field-Effect transistor (MOSFET)

1. Introduction

Titanium silicide($TiSi_2$) and cobalt silicide($CoSi_2$) have been employed as gate electrode materials in silicon-based Very Large-Scale Integration (VLSI) circuits, as a consequence of their low electrical resistivities and good process compatibilities.[1,2] $TiSi_2$, however, suffered from high electrical resistivity for sub-0.25 micron generations due to the difficulty of phase transition from high resistive C-49 phase to low resistive C-54 phase during the second Rapid Thermal Annealing (RTA) of the two-step RTA process.[3] Meanwhile, since $CoSi_2$ could maintain its low resistivity on much narrower lines, it has been employed as gate electrode material by several companies targeting for their sub-0.25 micron technology generations.[4]

Recently, needs for Embedded DRAM and Logic (EDL) technology have been rapidly increasing in an effort to merge DRAM cell arrays and logic circuits in a single chip for the advantages of lower power consumption and higher performance.[5,6] We have empolyed cobalt silicide as source/drain contact material to maintain high-speed logic devices in the EDL technology.[7] Cobalt silicidation has been conducted under TiN or Ti capping layer to prevent the oxidation of cobalt layer during the silicidation process.[8,9] Especially, epitaxial cobalt silicidation has been studied by inserting titanium,[10] silicon dioxide,[11] or silicon-germanium alloy[12] between cobalt and silicon to retard the reaction between the two materials, resulting in excellent thermal stability of cobalt disilicide upon post annealing. In addition, TiN capping layer is employed to reduce an unfavored reaction of cobalt and silicon with oxygen from air, and Ti capping layer to retard also the reaction between cobalt and silicon, resulting in a high quality polycrystalline cobalt disilicide.[13]

This work presents the effects of Ti and TiN capping layers on cobalt-silicided CMOS device characteristics under a full integration of EDL. The TiN capping layer is shown to be superior to the Ti capping layer with respect to high thermal stability and the current driving capability of pMOSFETs.

2. Expremental

The substrates used in this study were p-type Si (001) wafers with electrical resistivity of 9-12 ohmcm. Phosphorus (P) and boron (B) were ion-implanted to form n and p-well in the substrate after Shallow Trench Isolation (STI). Appropriate n and p-type dopant ion implantations for threshold voltage control of MOSFET devices were conducted in n and p-channel region, respectively. After gate etch process, reoxidation and Lightly Doped Drain (LDD) ion implantation were performed.

Rapid Thermal Annealing (RTA) process was performed to activate the implanted dopants. The samples were dipped in a diluted HF solution prior to cobalt (Co) film deposition to remove native oxide. Co film was sputter deposited without breaking vacuum in a DC magnetron sputtering system.[13] To investigate the effects of capping materials on the full integrated EDL with cobalt silicide in source / drain region, Ti and TiN capping materials were sputter deposited on the Co films, respectively. Subsequent RTA was carried out at 600°C for 60 sec in an N_2 ambient (first RTA). Unreacted metals were then removed in metal etchant solu-

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tions. Additional annealing was performed at 750°C for 30 sec to form low resistivity $CoSi_2$ (second RTA). In the case of DRAM part, a stack capacitor structure based on NO dielectric was used. Subsequently, BPSG layer was deposited and subjected to a reflow process for planarization for 60 min at 850°C. The fabricated samples were analyzed by employing Transmission Electron Microscope (TEM: Philips CM200 with field emission gun) and Focused Ion Beam (FIB: Micrion 2500). Doping profile was measured by employing Secondary Ion Mass Spectrometry (SIMS: Cameca IMS-6F).

3. Results and Discussion

The leakage currents of TiN capped silicided, Ti capped silicided, and non-silicided junctions that experience the full EDL integration with normal DRAM processes for stack cell capacitors are compared in Fig. 1. The junction leakage data are obtained from two types of patterns (area-dominant and edge-dominant patterns), and represented by solid and open symbols, respectively. The leakage currents are measured by applying 4 V of V_{DS} to drain and source at 85°C. The junction leakage level of TiN capped silicided junctions is comparable to that of non-silicided junctions. In the case of Ti capping layers, however, larger leakage currents as well as wider leakage current distributions are observed.

In order to investigate the cause of the leakage current degradation at source/drain regions, TEM cross-sectional micrographs of $CoSi_2$ layers with the two different capping layers are shown in Fig. 2. More protrusions of $CoSi_2$ are observed with Ti capping, compared with TiN capping layer, as can be seen in Fig. 2. It is believed that the protrusion of $CoSi_2$ is attributed to the degradation of leakage currents in the junctions. This implies that the TiN capping layer is superior to the Ti capping layer with respect to high thermal stability that is essential for EDL technologies.

In Figs. 3 and 4, the threshold voltage and the operating current characteristics of nMOSFET and pMOSFET devi-

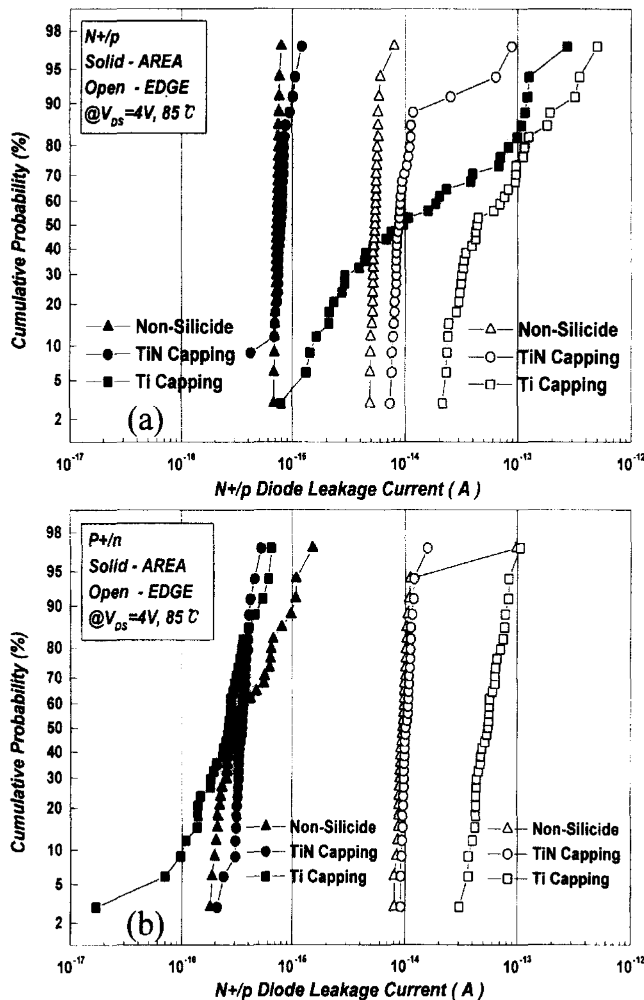

Fig. 1. Cumulative probability of junction leakage currents in (a) N+/p and (b) P+/n junction diodes at 4V and 85°C after the full EDL processes.

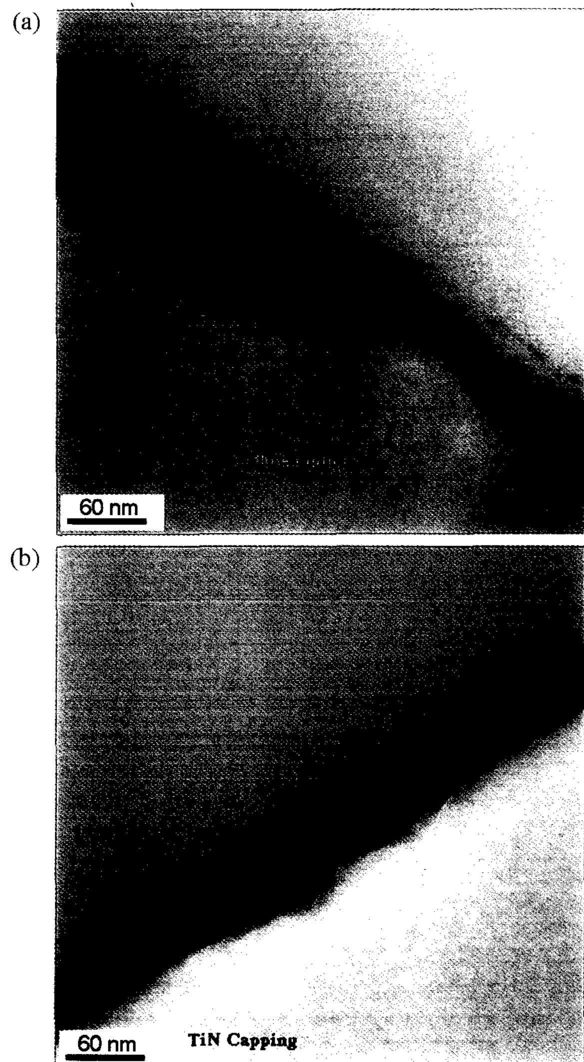

Fig. 2. TEM cross-sectional micrographs of $CoSi_2$ formation with (a) Ti capping layer and (b) TiN capping layer after the full EDL processes.

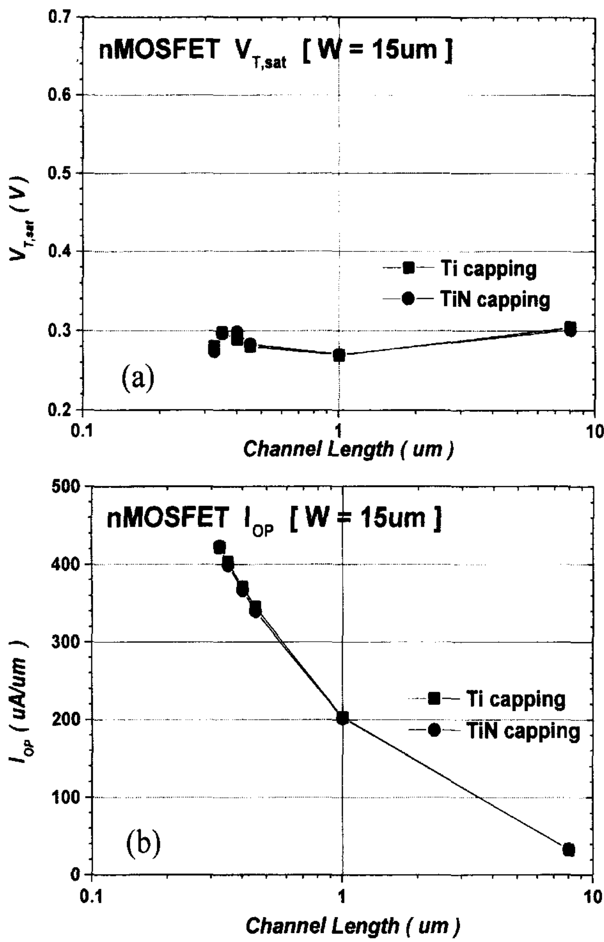

Fig. 3. Gate length dependence of (a) $V_{T,sat}$ and (b) I_{OP} characteristics of nMOSFETs with Ti and TiN capped $CoSi_2$ junctions.

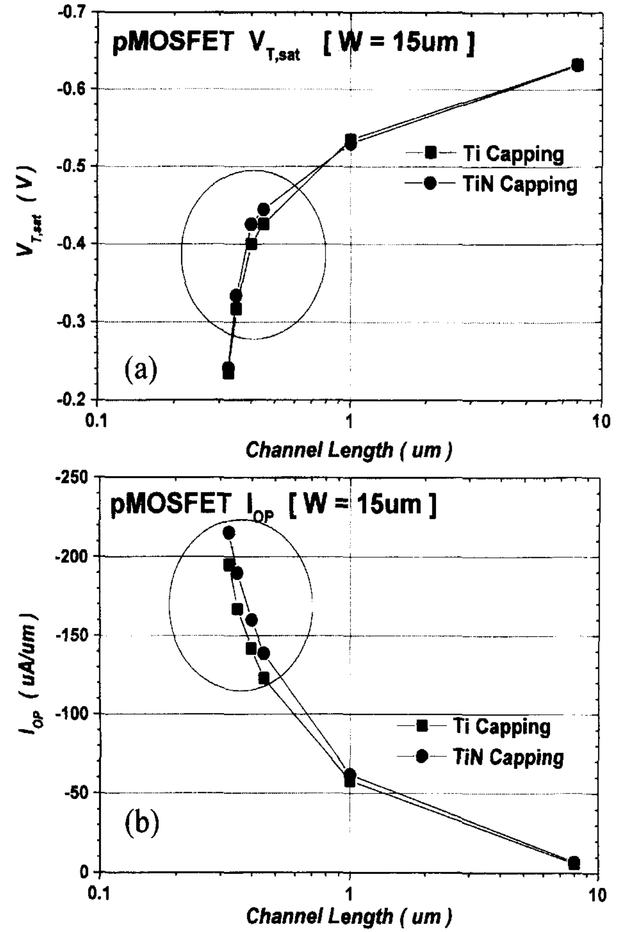

Fig. 4. Gate length dependence of (a) $V_{T,sat}$ and (b) I_{OP} characteristics of pMOSFETs with Ti and TiN capped $CoSi_2$ junctions.

Table 1. Ion Implantation Conditions of the Fabricated pMOSFETs in Fig. 5

SPLIT #	n-(Phosphorus)	p-(BF_2)
1	30 keV, 2.0×10^{13} cm^{-2}	20 keV, 1.0×10^{14} cm^{-2}
2	20 keV, 2.0×10^{13} cm^{-2}	20 keV, 1.5×10^{14} cm^{-2}
3	20 keV, 2.0×10^{13} cm^{-2}	30 keV, 1.0×10^{14} cm^{-2}
4	30 keV, 2.0×10^{13} cm^{-2}	30 keV, 1.5×10^{14} cm^{-2}

ces that have experienced the full EDL integration are shown, respectively. The width of MOSFETs is fixed at 15 μm, and their channel lengths are varied as shown in Fig. 3 and 4. In the case of nMOSFETs, no difference between TiN and Ti capping layers is shown. On the contrary, a remarkable difference between TiN and Ti capping layers is exhibited in pMOSFETs. To try to understand this difference, we have fabricated pMOSFET devices with several splits of implantation process that are shown in Table 1. The threshold voltage and the operating current characteristics of pMOSFETs with the split conditions are shown in Fig. 5. The results show that the operating currents of

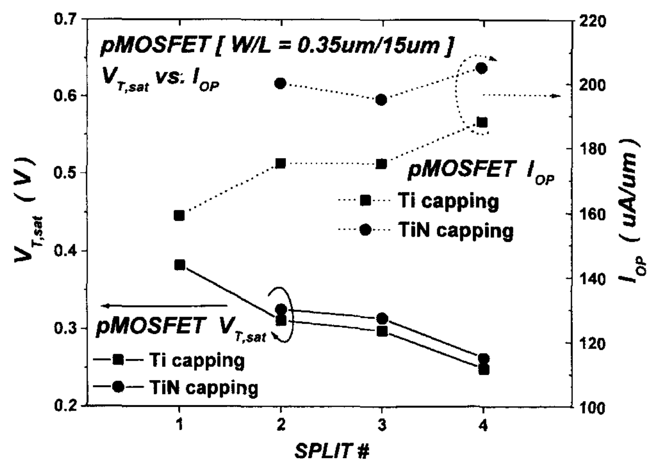

Fig. 5. $V_{T,sat}$ and I_{OP} characteristics on split conditions of pMOSFETs with Ti and TiN capped $CoSi_2$ junctions.

the devices with Ti capping layer are degraded by more than 10% compared with those of the devices with TiN capping layer, irrespective of the split conditions. The effect of degraded pMOSFETs on the propagation delay time (t_{pd}) of

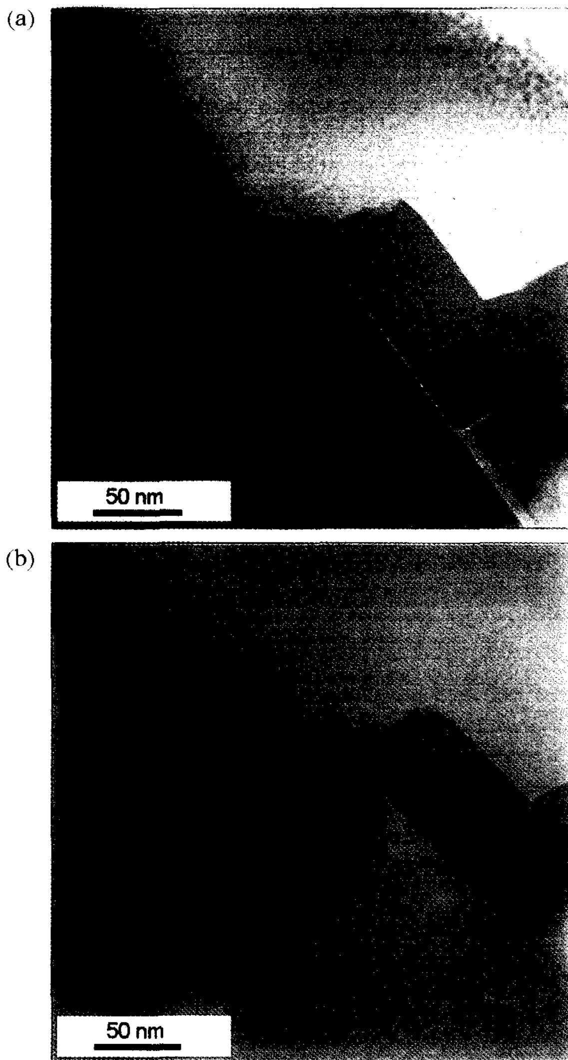

Fig. 6. TEM cross-sectional micrographs of both (a) nMOSFET and (b) pMOSFET devices with Ti capped $CoSi_2$ junctions.

CMOS inverter chain (L_g = 0.35) was investigated. A test pattern with 99 stages of COMS inverter chain connected in series was used to measure the propagation delay time of the COMS inverter. A good t_{pd} value of 71 picosec/stage was obtained at the inverter chain with TiN capping layer, while that of the inverter chain with Ti capping layer was 91 picosec/stage. For reference, the t_{pd} value of non-silicided CMOS inverter chain was 167 picosec/stage.

Fig. 6 shows TEM micrographs of both nMOSFET and pMOSFET devices with Ti capped $CoSi_2$ junctions. Observable differences in $CoSi_2$ thickness between the two devices are not shown, indicating that a stable and uniform formation of the $CoSi_2$ junction has been completed in both cases of the nMOSFET and pMOSFET devices. $CoSi_2$ encroachment below MOSFETs sidewall is also well formed for both devices. The angle of the $CoSi_2$/Si (001) interface under the sidewall spacer indicates that the interface is one of the {111} faces, and some portion of the interface at the source/

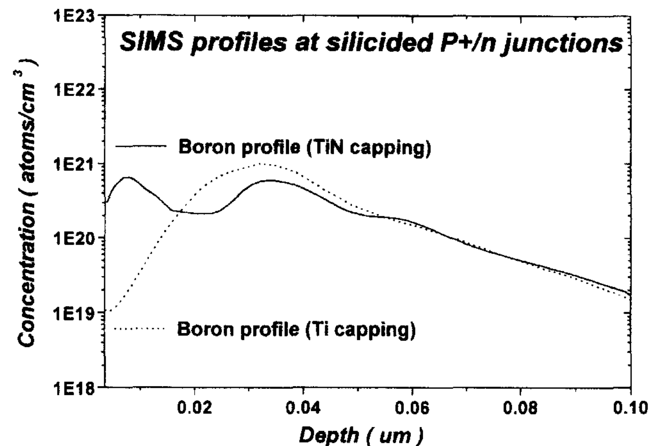

Fig. 7. SIMS depth profiles of boron at Ti and TiN capped $CoSi_2$ junction patterns.

drain region also zigzags along the {111} faces. This is easily understood by considering that the {111} interfaces are energetically more stable than other interfaces due to less dangling bonds.

In order to find out the origin of the pMOSFET operating current degradation when Ti capping layer was applied, we analyzed boron doping profiles in the Si substrate by SIMS. The boron implant dose was 3×10^{15} cm^{-2}, and the implant activation was conducted at 950°C for 30 sec in nitrogen ambient. As shown in Fig. 7, the out-diffusion of boron dopants at the junction interface has taken place. This indicated that Ti capping layer could not prevent the out-diffusion of the implanted boron dopants and degraded the driving capability of pMOSFETs due to a reduced LDD dosage. The interaction between Ti and boron should be studied further to understand this phenomenon.

4. Conclusion

We have investigated the influences of Ti and TiN capping layers on cobalt-silicided CMOS device characteristics. After the full integration of EDL including DRAM processes, the TiN capping layer was shown to be superior to the Ti capping layer with respect to high thermal stability and the current driving capability of pMOSFETs. We have discovered that the Ti capping layer could not prevent the out-diffusion of boron dopants so that the operating currents were degraded by more than 10%, compared with those of the TiN capping layer.

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