Analog Delay Locked Loop with Wide Locking Range

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Abstract— **For wide locking range, an analog delay locked loop (DLL) was designed with the selective phase inversion scheme and the variable number of delay elements. The number of delay elements was determined adaptively depending on the clock cycle time. During the analog fine locking stage, a self-initializing 3-state phase detector was used to avoid the initial state problem associated with the conventional 3-state phase detector. With these schemes, the locking range of analog DLL was increased by four times compared to the conventional scheme according to the simulation results.**

Index Terms — **Delay locked loop, wide locking range**

I. INTRODUCTION

The locking range of a conventional analog DLL is determined by the controllable delay range of the variable delay line[1]-[2]. The variable delay range, however, is often too limited to get the required locking range. For example, if the required locking range covers from 4ns to 15ns, the delay line should have at least a 500% variable delay range to cover the process, voltage, and temperature drift. The variable delay range of commonly used delay elements cannot be made as wide as required. One approach for a wide locking range is to have a programmable delay element, that is, the variable delay range of a delay element is coarsely programmed depending on the frequency range by some kind of control signal. For this, the information on the clock cycle time should be provided to the DLL to program the variable delay range.

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II. WIDE LOCKING RANGE ANALOG DLL

The analog DLL proposed in this work achieves a wide locking range by using the selective phase inversion scheme and the adaptive determination of the number of delay elements before the fine locking operation begins. Fig. 1 shows the block diagram of the wide locking range analog DLL proposed in this work. The variable delay line consists of 16 delay elements whose delay is controlled by Vctrl. The output of each delay element is connected to an input to the 16:1 multiplexer. The output of the multiplexer is used as the on-chip clock intClk. The locking operation of this DLL consists of three steps, that is, the selective inversion step of the input clock, the determination step of the number of delay cell, and the analog fine locking step of delay.

A. *Coarse locking*

Initially, the delay of each delay element is set to its center-value (the differential delay control voltages, Vctrl and Vctrlb, are initialized to be the same – see Figures 5 and 7) and the output of the first delay element is selected by the multiplexer. If the phase difference between extClk and intClk is larger than π as shown in Fig. 2-(a), the input clock to the delay line is inverted as shown in Fig. 2-(b). With this selective phase inversion, the required delay is reduced to "tD-tCK/2" from "tD". Therefore, the required variable delay range is halved for the same locking range. After this selective phase inversion, the optimum number of delay elements is

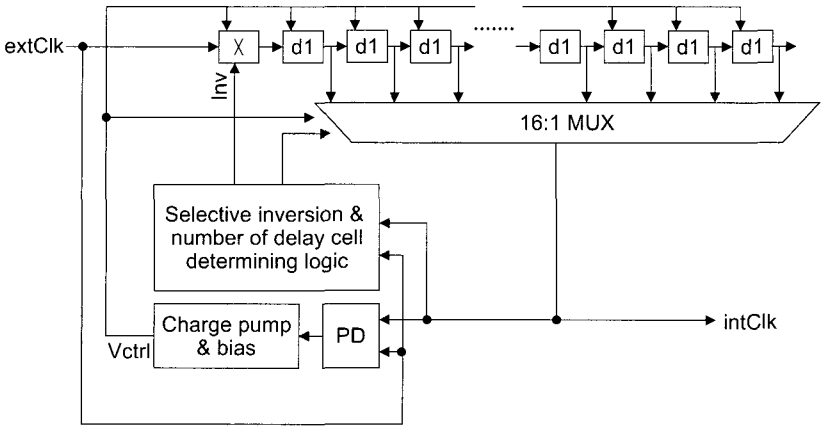

Fig. 1. Block diagram of proposed analog DLL

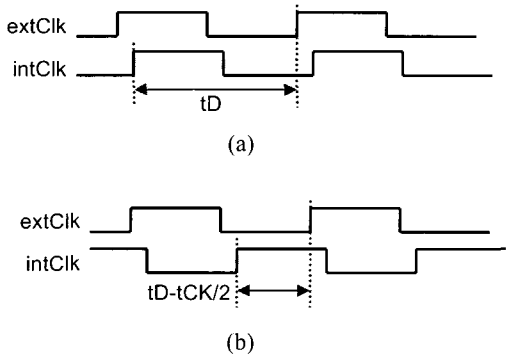

Fig. 2. Effectiveness of the selective phase inversion : (a) Before selective phase inversion (b) After selective phase inversion

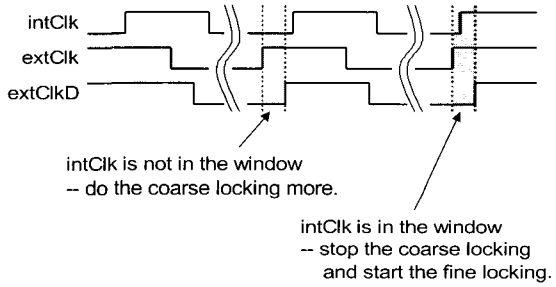

Fig. 3. Determination of the number of delay elements

determined by increasing the number of delay elements until the rising edge of intClk lies in the window formed by the rising edges of extClk and extClkD (delayed clock of extClk) as shown in Fig. 3. The size of this window should be larger than the delay of one delay element in order not to fail to find the optimum number of delay elements.

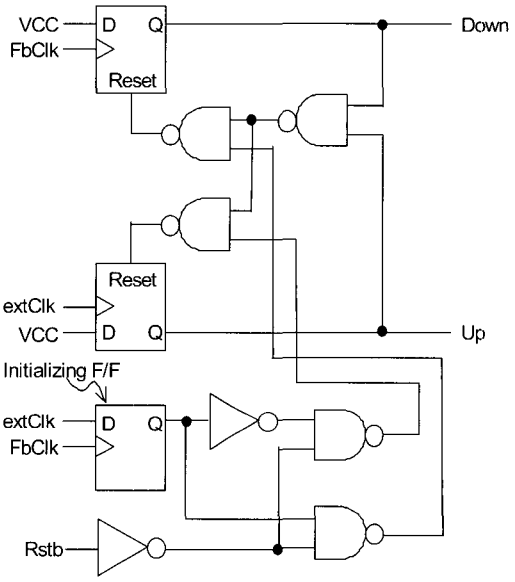

Fig. 4. Self-initializing 3-state phase detector

B. *Analog fine locking*

After these two steps of coarse locking, the analog fine locking step is performed as the final step to reduce the phase error to zero. This step is the same as that in the conventional analog DLL. During this analog finelocking step, the phase error is detected by a 3-state phase detector(PD) whose output pulse width is proportional to the amount of phase error. However, the 3-state PD can change the delay to a wrong direction depending on the initial state. The initial state is determined by the instant when the PD is enabled. If the rising edge of intClk (extClk) is seen right after the PD is enabled, the initial state of PD is Down (Up) regardless of the phase relationship between intClk and extClk.

Thus, the delay can be controlled to a wrong direction if the initial state of PD is different from the phase relationship between intClk and extClk. The self-initializing PD shown in Fig. 4 can alleviate this problem by employing another F/F (flip-flop) which determines the initial state depending on the phase relationship between intClk and extClk. Since the initial state of the PD is determined by initializing F/F depending on the phase relationship between intClk and extClk, the possibility of losing lock due to the wrong initial state can be eliminated.

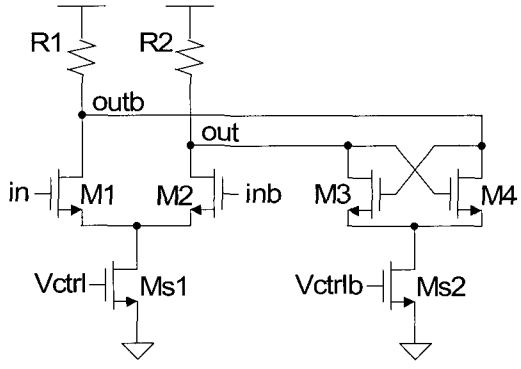

Fig. 5. Delay element with constant voltage swing

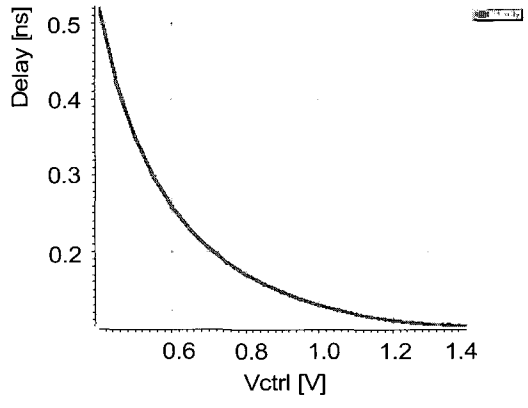

Fig. 6. Delay characteristic of the delay element in Figure 5

C. *Delay element*

The delay element, d1, is basically a differential pair whose delay is controlled by the negative resistance formed by M3 and M4 as shown in Fig. 5. The voltage swing of the output is constant because the currents through Ms1 and Ms2 are controlled to be constant. The delay characteristic of the delay element is shown in Fig. 6. The circuit in Fig. 7 generates the differential control signals, Vctrl and Vctrlb, from the outputs of differential charge pump circuit. This circuit ensures the sum of I1 and I2 to be Ibias, thus the voltage swing of the delay element is constant regardless of its delay. Since the delay is controlled by the differential control signals (the delay is determined by the difference between the differential control voltages, Vctrl and Vctrlb), the common-mode noise immunity can be improved.

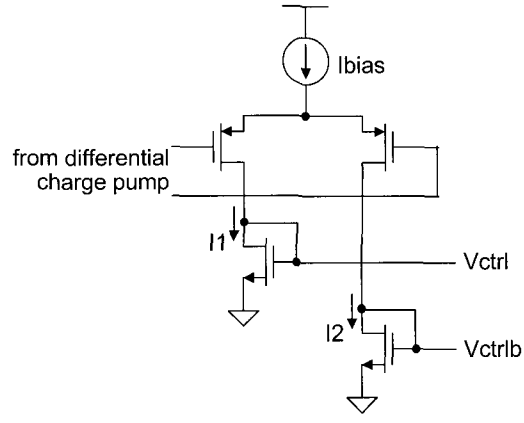

Fig. 7. Buffer circuit generating the differential control signal, Vctrl and Vctrlb, from the output of differential charge pump.

III. Simulation results

The proposed analog DLL has been simulated with a 0.25μm CMOS process. The simulated locking operation is shown in Fig. 8. First, the clock is inverted because the phase difference is larger than π, and then the number of delay elements increases till the rising edge of intClk lies between extClk and extClkD. Then the phase difference between extClk and intClk is reduced to about 160ps and the analog fine locking starts to reduce the phase difference to zero. The simulated locking range of the proposed DLL is 2ns~16ns (62.5MHz~500MHz) while it is only 4ns~8ns (125MHz~250MHz) for a conventional DLL with the same variable delay line. The lower limit of the locking range of the proposed DLL is determined by the transistor capability of a given process not by the DLL itself.

IV. Conclusion

An analog DLL has been proposed which has four times wider locking range than a conventional one. The wide locking range can be achieved by the selective phase inversion scheme and the adaptive determination

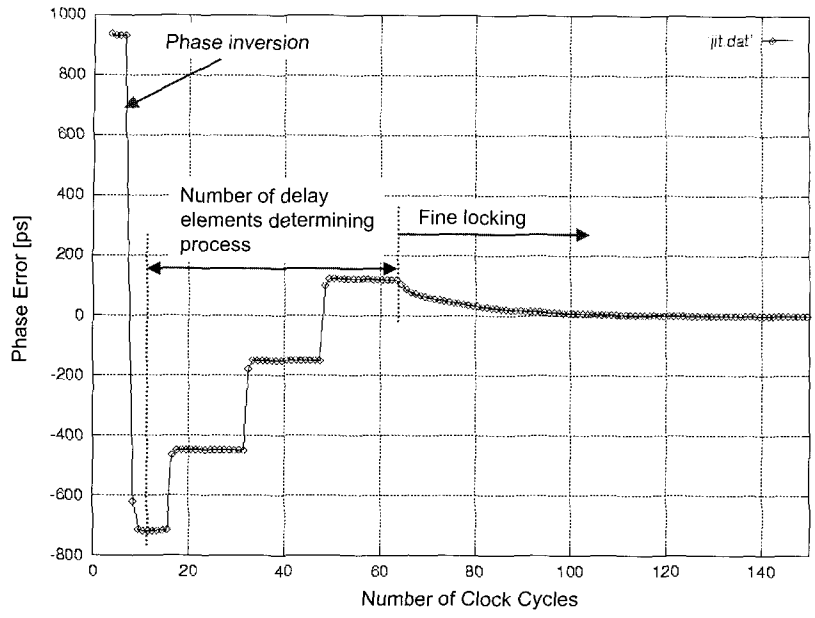

Fig. 8. Simulated locking operation of the proposed DLL

of the optimum number of delay elements. During the analog fine locking, a self-initializing 3-state phase detector is used in order to avoid the initial state problem of conventional 3-state phase detector.

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