

# Circuit Techniques for Low-Power Data Drivers of TFT-LCDs

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**Abstract**— A stepwise driving method was used for reducing the AC power consumption in a TFT-LCD. The AC power takes the largest portion of the total power consumption of a TFT-LCD. Experimental results confirmed that the AC power saving efficiency reached up to 75% when a 5-stepwise driving with each step time of 2 $\mu$  sec was applied to a 14.1 inch-diagonal XGA TFT-LCD. The second largest component of power consumption called the DC power comes from the quiescent currents in Op-amps. A simple and efficient architecture was proposed in this work to reduce this DC power consumption: Half of the Op-amps have the 5V-supplies, and the rest half have the 10V-supplies, and two Op-amps are shared by adjacent two channels. Measurements of test circuits showed that this simple method could reduce over 40% of the DC power consumption..

**Index Terms** — Low-power, Stepwise charging, TFT-LCD, Data driver

## I. INTRODUCTION

As a TFT-LCD gets more and more attractive as a display device for portable appliances, extensive researches are being carried out on low-power driving methods and circuit techniques [1-4]. Because the largest power consumption source is the AC power stemming from driving data lines as presented in Table 1 [5], previous publications [1-4] have focused on new AC driving methods. Those previous methods, however,

have some shortcomings: The vcom modulation method [1] is incompatible with the dot inversion method which is essential for high-quality images. The multi-field driving method [2] increases the circuit complexity, and reveals a problem with moving pictures. The charge recycling method [3] has no noticeable problem, but the AC power saving efficiency is no better than 50%. An advanced charge recycling method, called the triple charge sharing [4], of which the AC power saving efficiency is nearly 66% was proposed by the authors. This work has been intended to further increase the AC power saving efficiency.

It should be also noted in Table 1 that the DC power due to the quiescent currents of Op-amp circuits is the second largest source of the power consumption in data drivers. Accordingly, several circuit techniques of Op-amp have been reported [4,6-7] for reducing the quiescent current, among which the authors' Op-amp [4] has the lowest quiescent current. This work also presents a very simple and efficient circuit technique for further reducing the DC power of data drivers based on the authors' previous Op-amp [4].

## II. A CIRCUIT TECHNIQUE FOR AC POWER SAVING

### A. Theory of Stepwise Charging [8]

If a conventional buffer drives capacitance as shown in Fig.1, the power consumption can be calculated by equation (1).

$$P = I_{DD,AVG} V_{DD} = f C_L V_{DD}^2 \quad (1)$$

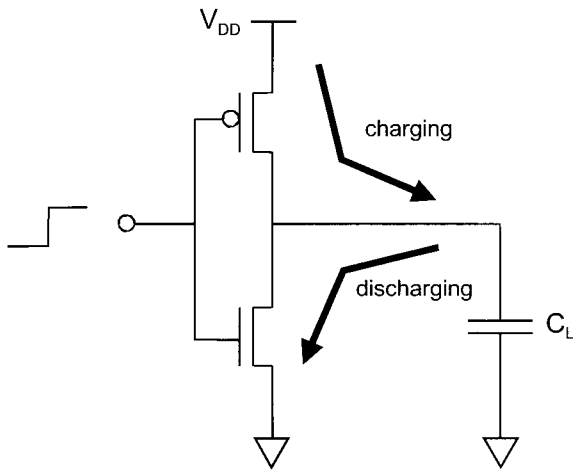
where  $I_{DD,AVG}$  is an average current supplied by  $V_{DD}$ ,  $V_{DD}$  is the supply voltage of buffer,  $f$  is the driving

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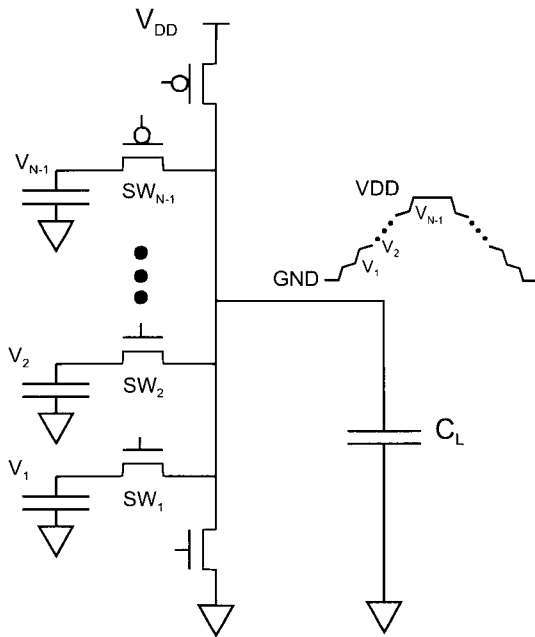
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**Table 1.** Power Consumption Breakdown of Conventional Data Driver for TFT-LCDS.

Image	Black		Black-White Vertical Stripe	
	Line/Dot	Column	Line/Dot	Column
Analog Quiescent Power (VDDa=10V)	145mW	145mW	145mW	145mW
Drive Digital Power (VDDd=2.5V)	5mW	5mW	15mW	15mW
Interface Bus Power	14mW	14mW	21mW	21mW
Panel AC Power	275mW	0.52mW	139mW	0.34mW
Total	439mW	164mW	320mW	181mW



**Fig.1.** Conventional Buffer Circuits for Driving Capacitance



**Fig.2.** Stepwise Charging Circuits for Driving Capacitance

frequency, and  $C_L$  is the load capacitance.

On the other hand, the N-stepwise charging and discharging method shown in Fig.2 can reduce the power consumption to  $1/N$  [8]. Sequential closures of switch  $SW_1$  to  $SW_{N-1}$  charge the load capacitance to  $V_1$ ,  $V_2$ , and  $V_{N-1}$ , assuming the tank capacitances are hundreds of times larger than the load capacitance. When the  $V_{DD}$  supply starts charging the load capacitance, the initial voltage of the load capacitance is  $V_{N-1}$ . So, the  $V_{DD}$  supply has only to charge the load capacitance from  $V_{N-1}$  to  $V_{DD}$  instead from ground to  $V_{DD}$ . Therefore, the current from the  $V_{DD}$  supply to the load capacitance is reduced to  $1/N$  of that of a conventional buffer, which means that the power from the  $V_{DD}$  supply is decreased to  $1/N$ . It should be noted that the charges supplied by the tank capacitors return to each tank capacitor during the stepwise discharging. Thus, each tank capacitor can play a role of an energy-recovery power supply. This power reduction can be explained in equation (2).

$$P = I_{DD,AVG} V_{DD} = F C_L \frac{V_{DD}}{N} V_{DD} = \frac{1}{N} f C_L V_{DD}^2 \quad (2)$$

However, in a practical sense, the power saving is somewhat lower than that given by equation (2). This is due to the power dissipation at the resistance on the data line interconnects and the on-resistance of MOSFET switches used in the stepwise driver circuit. Due to the voltage drop on the resistance components, the final voltage of the tank capacitor  $V_{N-1}$  converges to a value slightly lower [10] than the predicted value. Thus, the current from the  $V_{DD}$  supply to charge the load capacitance has to be increased, causing the degradation of power saving. This phenomenon will be discussed in

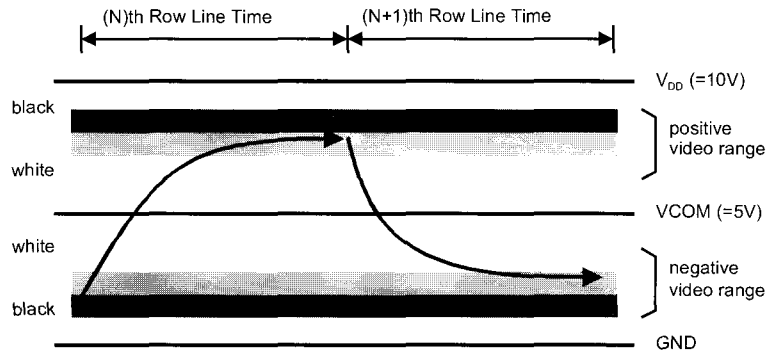


Fig. 3. Data Driving Waveform of Dot Inversion Method in TFT-LCDs

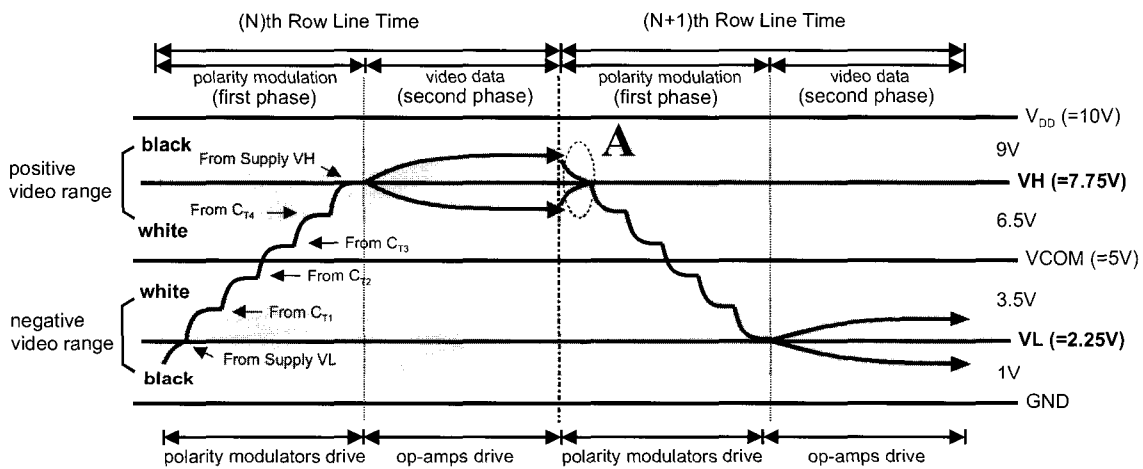


Fig. 4. Proposed Data Driving Waveform using Stepwise Charging Method in TFT-LCDs

detail in section II.C and section IV.

**B. Stepwise Data Driving Method for TFT-LCDs**

Among various inversion methods of TFT-LCDs, the dot inversion method which changes the signal polarity every row line time (1H) as shown in Fig.3 provides the best image quality. Data lines of a TFT-LCD have parasitic capacitance ranging from tens to hundreds of pico farads depending on the panel size. Thus each time they are charged and discharged, which results in a quite high power consumption. This is often referred to as AC power consumption.

In order to reduce the AC power consumption in TFT-LCDs, the stepwise driving method was employed in this work. However, the stepwise data driving for a full video range is practically impossible, because the video data are different from pixel to pixel and change from row to

row. Therefore, the stepwise data driving method is applied as follows in this work.

One row line time (1H) is divided into two phases, and during the first phase of a row line time polarities of even- or odd-numbered data lines are modulated to the positive or negative video range in a stepwise manner between two fixed voltage levels,  $V_L$  and  $V_H$ , as shown in Fig.4. In this case,  $V_L$  is the median voltage level of the negative video range, and  $V_H$  is that of the positive video range. Fig.5 shows the circuits and related control signals for a 5-step stepwise charging method. When the polarities are modulated from  $V_L$  to  $V_H$  level, the switch SWA is closed and the switches SW0 to SW5 are closed sequentially for stepwise charging. Since the voltage of data lines is the same as that of tank capacitor  $C_{T4}$  when  $V_H$  begins to drive data lines, the power supplied by  $V_H$  is reduced to a fifth of the power consumed when  $V_H$

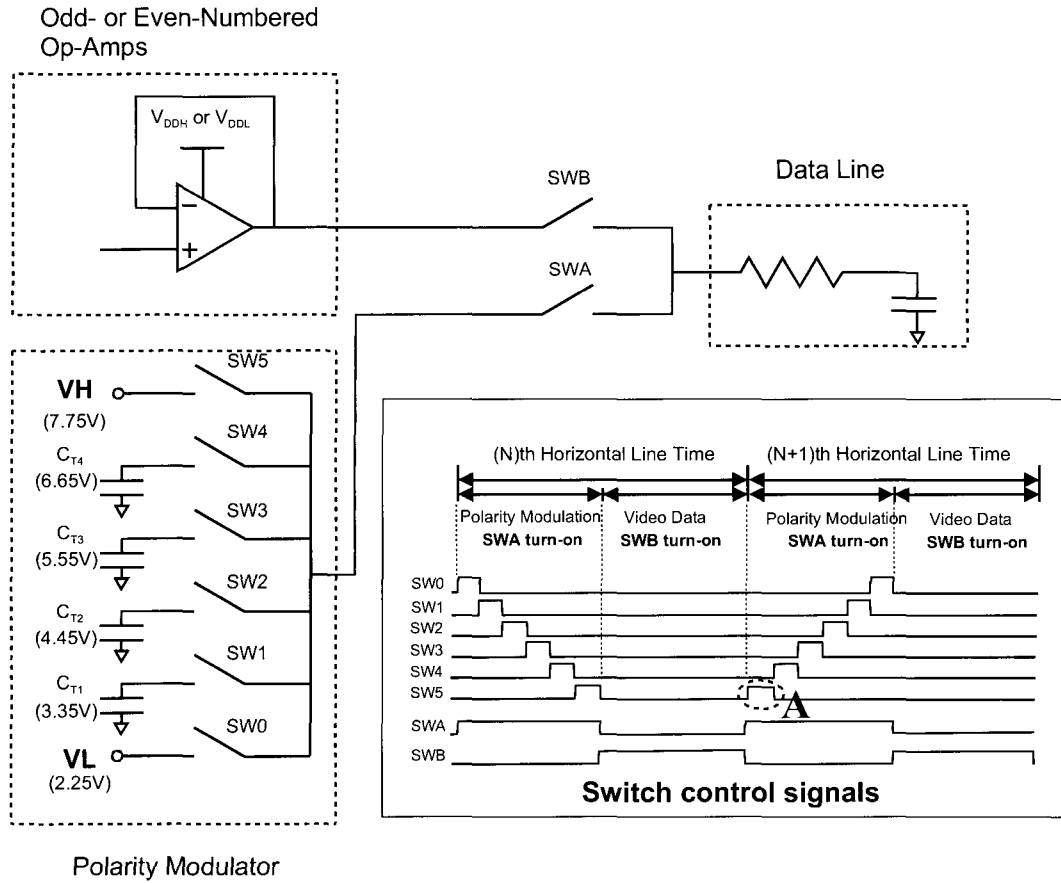


Fig. 5. Schematic Diagram of Data Driver Circuits for Stepwise Polarity Modulation with Control Signals

fully charges the data lines from  $V_L$  to  $V_H$  level. After the polarity modulation to  $V_H$  level, the actual video voltages of pixels are driven by Op-amps according to their own video data during the second phase of a row line time as shown in Fig.4 and Fig.5. Consequently, the Op-amps have only to charge the data lines from  $V_H$  to each pixel's own video data voltage unlike the conventional case in which the full video voltage range has to be charged by the Op-amps. In order to drive an actual video data to each pixel, the switch SWB is closed so that the Op-amp drives the data line in Fig.5.

At the beginning of the next row line time the voltages of the data lines are set to  $V_H$  level by closing the switch SW5 as marked by A in Fig.4 and Fig.5. This makes the voltage of the data lines one step-voltage higher than that of tank capacitor  $C_{T4}$  irrespective of the video data of the current row line time. Thus, during the downward polarity modulation of the next row line time the charges return from the data lines to the tank capacitors irrespective of the video data of the current row line time,

and the power supplied by the tank capacitors is recovered during the downward polarity modulation.

The theoretical power saving efficiency can be easily calculated when the stepwise charging method is applied to drive TFT-LCDs. For convenience of comparison, the conventional driving circuit is presented in Fig.6 where the full video range swing is carried out by the authors' Op-amps[4]. The AC power consumption of the conventional driving,  $P_{CONV}$  is expressed as follows:

$$P_{CONV} = I_{DD,AVG} V_{DD} = N_{DATA} C_L V_{SWING} \frac{f_{ROW}}{2} V_{DD} \tag{3}$$

where  $I_{DD,AVG}$  is the average current supplied by a power supply  $V_{DD}$ ,  $N_{DATA}$  is the number of data lines,  $C_L$  is the capacitance of a data line,  $V_{SWING}$  is the voltage change of  $C_L$  and  $f_{ROW}$  is the row line frequency.

On the other hand, the power consumption of the stepwise driving method,  $P_{STEPWISE}$ , breaks down into

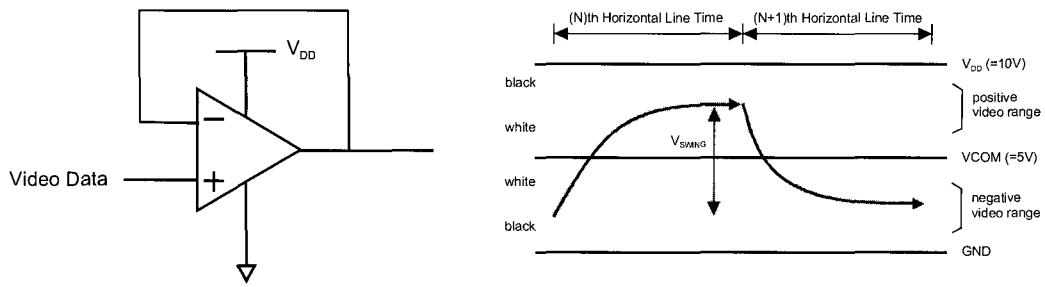


Fig. 6. Schematic Diagram of Buffer Circuits for Conventional TFT-LCD Data Drivers with Driving Waveform

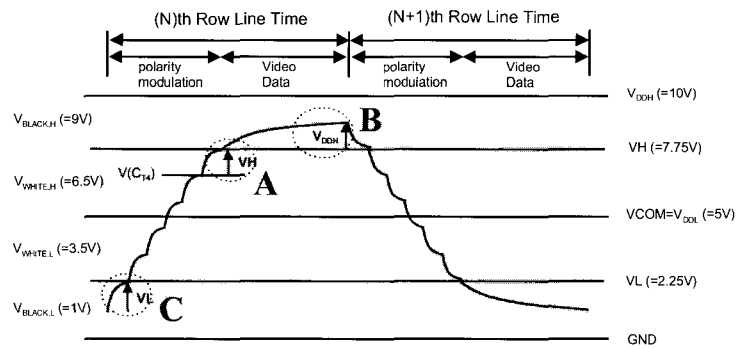


Fig. 7. Stepwise Driving Waveform for Black Image Display with Effective Power Supplies

four parts as expressed in equation (4). The power supplies  $VH$  and  $VL$  supply currents for stepwise polarity modulation, and the power supplies  $VDDH$  and  $VDDL$  supply currents through Op-amps for writing the actual video voltage. As will be covered in section III, in the proposed driving scheme half of the data lines are driven by a high-voltage power supply  $VDDH$  for the positive video range, and the rest half of the data lines are driven by a low-voltage power supply,  $VDDL$ , for the negative video range.

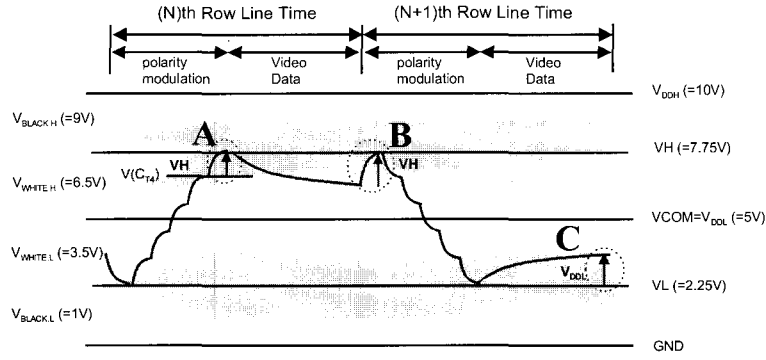
$$\begin{aligned}
 P_{STEPWISE} &= P_{VH} + P_{VL} + P_{VDDH} + P_{VDDL} \\
 &= I_{VH,AVG} VH + I_{VL,AVG} VL \\
 &\quad + I_{VDDH,AVG} VDDH + I_{VDDL,AVG} VDDL
 \end{aligned} \tag{4}$$

where  $P_{VH}$ ,  $P_{VL}$ ,  $P_{VDDH}$ , and  $P_{VDDL}$  are the power consumption supplied by  $VH$ ,  $VL$ ,  $VDDH$  and  $VDDL$  respectively.

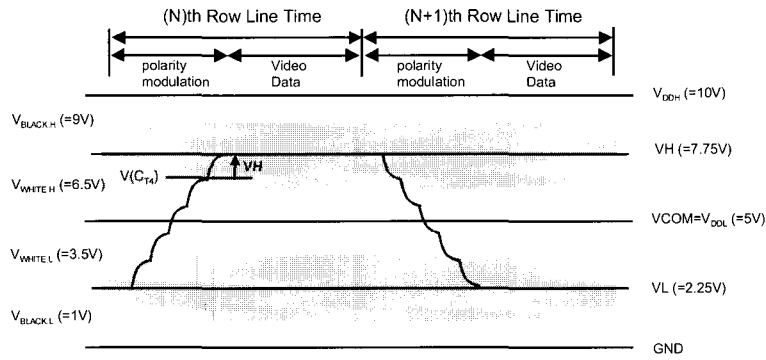
Referring to Fig.7, Fig.8 and Fig.9, the power consumption for black, white and median gray display is analyzed. In Fig. 7 which shows the case of black display, the power consumption by  $VH$ ,  $VL$ , and  $VDDH$  occurs every second row line time as marked by A, B and C respectively. A represents the power supplied by  $VH$

during the polarity modulation. After the polarity modulation, Op-amps ( $VDDH$ ) charge the data lines to  $V_{BLACK,H}$  as marked by B. After the black display in the negative video range the power supply  $VL$  charges the data lines to  $VL$  for polarity modulation, as marked by C in Fig.7. Therefore, equation (4) is reduced to equation (5) for the power consumption for black display.

$$\begin{aligned}
 P_{STEPWISE, BLACK} &= P_{VH} + P_{VL} + P_{VDDH} \\
 &= I_{VH,AVG} VH + I_{VL,AVG} VL \\
 &\quad + I_{VDDH,AVG} VDDH \\
 &= N_{DATA} C_L (VH - V(C_{T4})) \frac{f_{ROW}}{2} VH \\
 &\quad + N_{DATA} C_L (VL - V_{BLACK,L}) \frac{f_{ROW}}{2} VL \\
 &\quad + N_{DATA} C_L (V_{BLACK,H} - VH) \frac{f_{ROW}}{2} VDDH \\
 &= N_{DATA} C_L \frac{VH - VL}{N} \frac{f_{ROW}}{2} VH \\
 &\quad + N_{DATA} C_L (VL - V_{BLACK,L}) \frac{f_{ROW}}{2} VL \\
 &\quad + N_{DATA} C_L (V_{BLACK,H} - VH) \frac{f_{ROW}}{2} VDDH
 \end{aligned} \tag{5}$$



**Fig. 8.** Stepwise Driving Waveform for White Image Display with Effective Power Supplies



**Fig. 9.** Stepwise Driving Waveform for Median Gray Image Display with Effective Power Supplies

where  $N$  is the number of steps for polarity modulation,  $V_{BLACK,L}$  and  $V_{BLACK,H}$  are the voltage levels of black in the negative and positive voltage range respectively, and  $V(C_{T4})$  is the voltage of tank capacitor  $C_{T4}$ .

For white display, the power is supplied by  $V_H$  and  $V_{DDL}$  as marked by **A**, **B** and **C** in Fig.8. **A** and **B** represent the power supplied by  $V_H$ . In case of white display, the polarity modulation to  $V_H$  overcharges data lines, so after the polarity modulation the data lines are discharged to  $V_{WHITE,H}$  and the power supply  $V_H$  recharges the data lines to  $V_H$  level just before the downward polarity modulation, as marked by **B** in Fig.8. The downward polarity modulation to  $V_L$  overdischarges the data lines, so the Op-amps ( $V_{DDL}$ ) charge the data lines to  $V_{WHITE,L}$  for white display, as marked by **C** in Fig.8. These overcharge and over-discharge deteriorate the power saving efficiency for white display. Experimental results in section IV will show that the power saving efficiency for black, white and median gray display. Equation (6) expresses the power

consumption for white display.

$$\begin{aligned}
 P_{STEPWISE,WHITE} &= P_{VH} + P_{VDDL} \\
 &= I_{VH,AVG} V_H + I_{VDDL,AVG} V_{DDL} \\
 &= N_{DATA} C_L (V_H - V(C_{T4})) \frac{f_{ROW}}{2} V_H \\
 &\quad + N_{DATA} C_L (V_H - V_{WHITE,H}) \frac{f_{ROW}}{2} V_H \\
 &\quad + N_{DATA} C_L (V_{WHITE,L} - V_L) \frac{f_{ROW}}{2} V_{DDL} \\
 &= N_{DATA} C_L \frac{V_H - V_L}{N} \frac{f_{ROW}}{2} V_H \\
 &\quad + N_{DATA} C_L (V_H - V_{WHITE,H}) \frac{f_{ROW}}{2} V_H \\
 &\quad + N_{DATA} C_L (V_{WHITE,L} - V_L) \frac{f_{ROW}}{2} V_{DDL}
 \end{aligned} \tag{6}$$

where  $V_{WHITE,L}$  and  $V_{WHITE,H}$  are the voltage levels of white in the negative and positive voltage range respectively

Since  $VH$  and  $VL$  correspond to the median gray display in the positive and negative video range respectively, no Op-amp operation is necessary as shown in Fig.9. That is, for the median gray display the power is supplied only by  $VH$ . Of course, this is a very ideal case. In reality,  $V_{DDH}$ ,  $V_{DDL}$  or  $VL$  also supplies power, if the gray scales of a display image deviate from  $VH$  or  $VL$ . This ideal power consumption for the median gray display is obtained by equation (7).

$$\begin{aligned}
 P_{STEPWISE,MEDIAN} &= P_{VH} = I_{VH,AVG} VH \\
 &= N_{DATA} C_L (VH - V(C_{T4})) \frac{f_{ROW}}{2} VH \quad (7) \\
 &= N_{DATA} C_L \frac{VH - VL}{N} \frac{f_{ROW}}{2} VH
 \end{aligned}$$

The power saving efficiency of the stepwise driving method can be achieved using equation (3), (5), (6) and (7). Dividing equation (7) by (3), the power consumption ratio for median display is obtained. Those for white or black display are also obtained similarly. Here, for convenience, only the power saving efficiency for the median gray display is calculated. For black or white display, the experimental results will be given in section IV.

$$\begin{aligned}
 \frac{P_{STEPWISE,MEDIAN}}{P_{CONV}} &= \frac{N_{DATA} C_L \frac{VH - VL}{N} \frac{f_{LINE}}{2} VH}{N_{DATA} C_L V_{SWING} \frac{f_{ROW}}{2} V_{DD}} \quad (8) \\
 &= \frac{VH}{N V_{DD}}
 \end{aligned}$$

where  $V_{SWING}$  of the conventional driving method is equal to  $VH - VL$  for the median gray display. Assuming that the number of step is 5,  $V_{DD}$  is 10V, and  $VH$  is 7.75V as shown in Fig.5, the power consumption ratio is theoretically 0.155, that is, the power saving efficiency is 84.5%.

### C. Practical Consideration on the Stepwise Driving Method

The power saving efficiency of 84.5% is practically unattainable, because of the following two constraints. In designing the driving scheme in Fig.4, the second phase time for video data writing from  $VH$  level to any voltage

in the video range should be assigned first, and the rest of a row line time is utilized for the polarity modulation. So, the step time may not be long enough for the stepwise polarity modulation due to the parasitic resistance and capacitance of the data lines and the switches. The lack of step time leads to the incomplete stepwise charging of the data lines to each voltage level of tank capacitors. That is, if the switch SW0 is closed for insufficient step time in Fig.5, the data lines are not completely charged to 2.25V due to the parasitic resistance and capacitance, and this incomplete charging is repeated until switch the SW4 is closed, leading to accumulated mis-charging. Therefore, when the switch SW5 is about to be closed for  $VH$  to charge the data lines, the voltage of the data lines do not reach that of  $C_{T4}$ . This means that  $VH$  has to supply a more current to charge the data lines to  $VH$  level compared to the theoretical case in which the data lines are completely charged to the voltage of  $C_{T4}$  before  $VH$  drives the data lines. It is clearly understood in equation (5), (6) and (7) that the power supplied by  $VH$  is directly related to the voltage of tank capacitor  $C_{T4}$ .

Another constraint is the voltage drop of the tank capacitor voltage. Because power is dissipated in the resistance of switches and data lines when the tank capacitors drive data lines, energy loss of the tank capacitors occurs, which leads to the voltage drops of the tank capacitor voltage. In addition to the incomplete charging of the data lines due to insufficient step time, this voltage drop due to energy loss of the tank capacitors further deteriorates the power saving efficiency. More specifically, in the stepwise charging the power supplied by  $VH$  is increased, because the voltage of the tank capacitor  $C_{T4}$  drops due to energy loss, so the voltage of the data lines to be driven by  $VH$  are also lower when  $VH$  is about to drive the data lines. In spite of the energy loss, the proposed driving scheme uses no charge refreshing operation or circuits. Instead, as explained in section II.B,  $VH$  plays a role of recharging the tank capacitors by charging the data lines to  $VH$  level at the beginning of stepwise discharging.

## III. A CIRCUIT TECHNIQUE FOR DC POWER SAVING

The authors previously proposed an Op-amp circuit

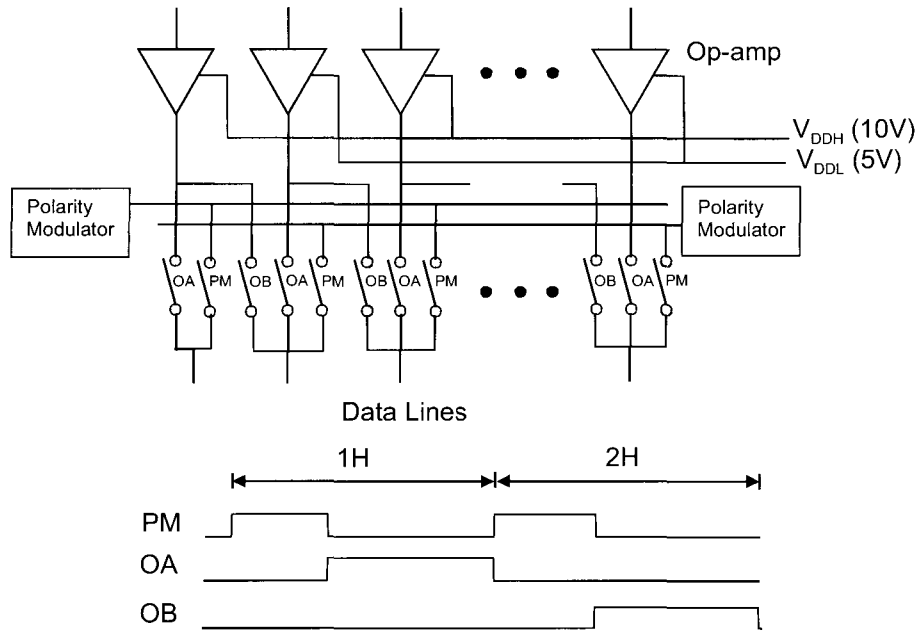


Fig. 10. Schematic Diagram of Output Stages of Proposed Data Driver for DC Power Saving with Control Signals

[4] with a low-quiescent current of  $5\mu\text{A} \sim 7\mu\text{A}$  at 5V-supply which is the lowest among the reported results [4, 6-7]. Because a quiescent current of the proposed Op-Amp increases with the supply voltage, the DC power can be further reduced if a lower supply voltage is used.

We noted that half of the channels in a data driver circuit drive video data of a negative polarity in dot inversion method and the Op-amps driving negative video data can have a lower supply voltage. Typically the Op-amps in a data driver of TFT-LCDs have a supply voltage of 10V or higher. For negative video data, however, a supply voltage of 5V or only a little higher is enough. To realize this idea the conventional data driver circuit was slightly modified in this work. Op-amps of odd (or even)-numbered channels have a 10V-supply, and those of even (or odd)-numbered channels have a 5V-supply. Because adjacent two data lines have opposite polarities, and the signal polarity of a data line changes every row line time in dot inversion, two Op-amps can be shared by adjacent two data lines. That is, when a data line is driven to positive video data, it is driven by an Op-amp with a 10V-supply, and the adjacent line is driven to negative video by one with a 5V-supply. In the next row line time, two Op-amps driving two adjacent data lines are exchanged.

In addition to output switches for the polarity modulation (switch A and B in Fig.5), another switch is

necessary for this Op-amp sharing. As a result, three transistors are used at each channel as output switches as shown in Fig.10, where the related control signals are also presented. The signal PM closes the output switch for the polarity modulation, and OA and OB choose an Op-Amp with a 10V- and a 5V-supply respectively. Op-amps with a 10V- and a 5V-supply use exactly the same circuits except for their supply voltages.

## IV. EXPERIMENTS

### A. Test Circuits and Conditions

We have fabricated test circuits and measured the power consumption. The block diagram of the test circuits is presented in Fig.11. The test circuits consist of 4 channels of Op-amps, two stepwise polarity modulators and output switches shown in Fig.5, control circuits, an integrated resistor string and external tank capacitors. The Op-amps of odd-numbered channels have a high-voltage supply  $V_{DDH}$  and those of even-numbered channels have a low-voltage supply  $V_{DDL}$ . In the dot inversion method, directions of the polarity modulation of odd- and even-numbered data lines are opposite, thus two polarity modulators are necessary. The control circuits generate control signals for switches



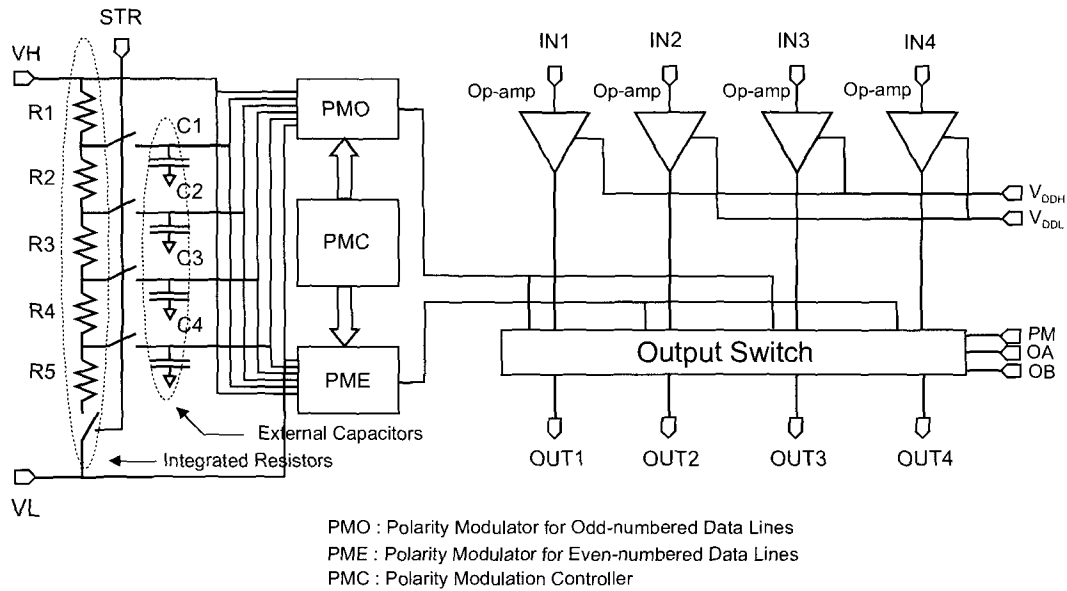


Fig. 11. Schematic Diagram of Fabricated Test Circuits

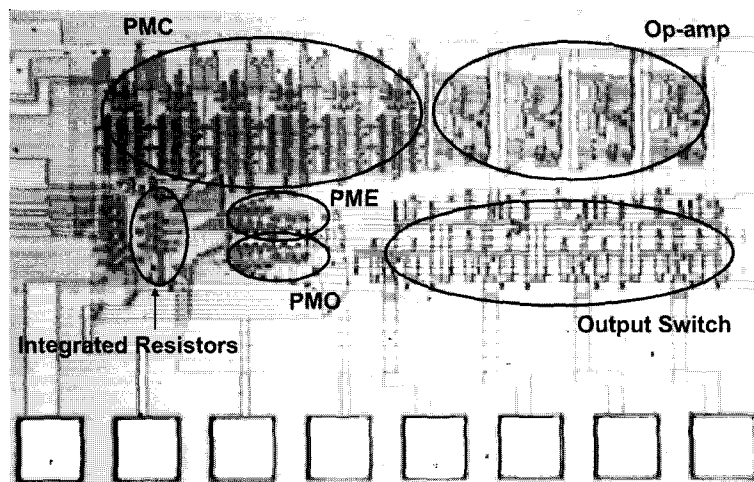


Fig. 12. Microphotograph of Fabricated Test Circuits

of the polarity modulators. A resistor string is not an essential part, but used only for convenience of the experiment. As a matter of fact, the tank capacitors can have their own voltages between  $VH$  and  $VL$  even without a resistor string, because the tank capacitors can be charged by  $VH$  and  $VL$  through data lines. That is, during the stepwise discharging, charges of the data lines flow into the tank capacitors. In the experiment the voltages of tank capacitors are initialized by a control signal  $STR$  just after the driver is turned-on. To prevent unnecessary static currents from flowing through the integrated resistor string, a switch controlled by  $STR$  is

inserted between the integrated resistors and  $VL$ , and closed only at the initial stage. Fig. 12 shows a microphotograph of the fabricated test chip.  $PMO$  and  $PME$  are polarity modulators for the odd- and even-numbered data lines respectively.

To evaluate the AC power saving efficiency, we measured the power consumption of both the stepwise and the conventional driving method using the test circuits shown in Fig.11. To measure the power consumption of the conventional driving method, the polarity modulators and the control circuits should be idle, and only the Op-amps drive data lines in the full

**Table 2.** Measurement Condition of Fabricated Test Circuits

Panel Size (inch)		14.1
Resolution		XGA
Frame Frequency (Hz)		60
Line Time ( $\mu$ sec)		22
Data Line	Resistance ( $k\Omega$ )	5, 7.5, 10
	Capacitance (pF)	66, 99, 132

**Table 3.** Applied Voltages for Measurement

$V_{DDH}$	5V	$V_{BLACK,H}$	5V
$V_{DDL} (=V_{COM})$	2.5V	$V_{BLACK,L}$	0V
$V_H$	4.5V	$V_{WHITE,H}$	4V
$V_L$	0.5V	$V_{WHITE,L}$	1V

video range with a high-voltage supply,  $V_{DDH}$ . The AC power for stepwise driving which is supplied by  $V_H$ ,  $V_L$ ,  $V_{DDH}$  and  $V_{DDL}$  is obtained and compared with that for conventional driving which is supplied only by  $V_{DDH}$ .

Measurements of the power consumption were carried out under the following conditions: The stepwise driving method is applied to a 14.1-inch diagonal TFT-LCD with XGA resolution. Typically the resistance of a data line has a value between  $5k\Omega$  and  $10k\Omega$ , and the capacitance has a value between  $50pF$  and  $100pF$ . An RC network modeling a data line was established by using a T3 model. The frame frequency was assumed to be 60Hz, leading to a row line time of about  $22\mu$  sec. These measurement conditions are summarized in Table 2. As mentioned above, the test circuits have been fabricated in a standard CMOS process, so the voltage range of Fig.4 is inapplicable. The applied voltages for the experiment are listed in Table 3. Although the power saving efficiency is dependent upon the voltage range as easily found from equation (5) to (7), the feasibility of the stepwise driving method and the power saving efficiency can be evaluated. Although the total power consumption of the stepwise driving method generally includes the power consumed by the related switches and the control circuits [9], the power consumed by the related switches and the control circuits was not considered for simplicity in this experiment. It is because

the total gate capacitance of the switches and the control circuits for the stepwise driving method was less than  $1pF$ , while the capacitance of the data lines was over hundreds of pico-farads.

### B. Results and Discussions

Fig.13 shows the output waveforms of the stepwise data driver circuits observed at the far end of a data line. The control signal PMS triggers the start of the stepwise polarity modulation, and the signal PM controls the output switches for the polarity modulation or video data writing. When a typical a-Si TFT model with an effective mobility of  $0.8cm^2/Vsec$  was used, HSPICE simulations revealed that it takes at least  $10\mu$ sec to charge a pixel electrode from  $V_H$  to a video voltage  $V_{BLACK,H}$ . Another  $2\mu$ sec is also necessary to set the voltage of data lines to  $V_H$  or  $V_L$  before the stepwise polarity modulation starts as described in section II. Consequently,  $10\mu$ sec of a row line time of  $22\mu$ sec is available for the stepwise polarity modulation. The number of step and step time have been chosen to be 5 and  $2\mu$ sec respectively through HSPICE simulations.

Fig.14, Fig.15 and Fig.16 show the measured power saving efficiencies of the median gray, black and white display images respectively, where it is easily found that the power saving efficiency of the stepwise driving method in a TFT-LCD is highly dependent upon a

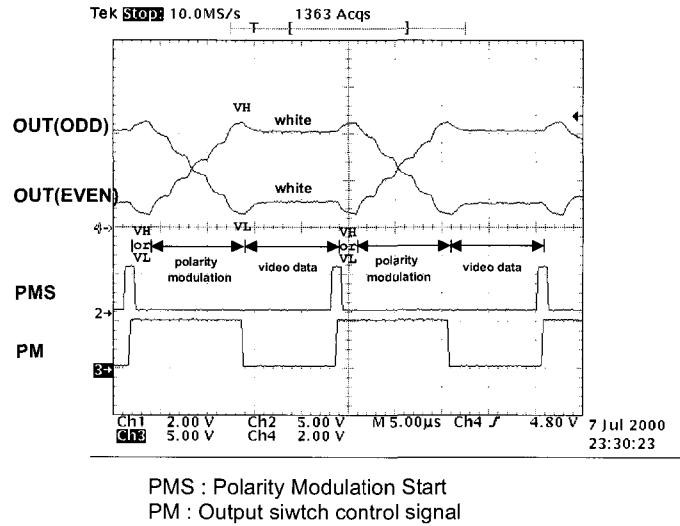


Fig. 13. Measured Driving Waveforms for White Image Display with Control Signals

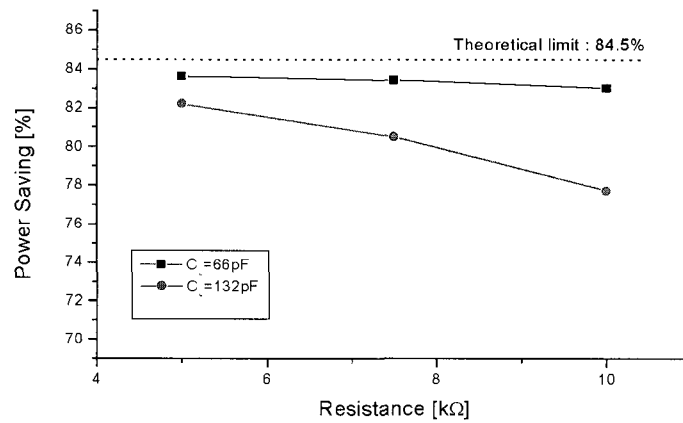


Fig.14. Measured Power Saving Efficiency of Median Gray Display with Load Condition

display image. While this driving scheme works well in case of median or dark gray images, the power saving efficiency is poor for white or bright gray images. It is because the polarity modulation between the two fixed voltages means unnecessary overcharging data lines when white or bright gray images are displayed. Therefore, further researches are required for reducing the power consumption for white or bright gray images. But, this stepwise driving is still meaningful, because the voltage levels of most display images can be assumed to stay near the median gray level on the average.

In Fig.14, Fig.15 and Fig.16, the dotted lines indicate the theoretical power saving efficiencies obtained using equation (3) to (7). In the experiment, however, two practical constraints, the insufficient step time and

charge loss of tank capacitors, combine to make lower the power saving efficiency. For example, from equation (8) it is found that the theoretical power saving efficiency of the median gray display is 84.5% when the number of step is 5,  $V_{DD}$  is 10V and  $VH$  is 7.75V. However, the measurement results reveal that the actual power saving efficiency falls to about 78%. The plots in Fig. 14 to Fig.16 reflect the combined effect of the above-mentioned two constraints.

As explained in section II, the voltage drop of the tank capacitor  $C_{T4}$  has a great influence on the power saving efficiency, so it is meaningful to check the voltage drop of the tank capacitor  $C_{T4}$ . Because the applicable voltage range of the fabricated test circuits is limited to 5V, the voltage drop of the tank capacitor  $C_{T4}$  in a practical

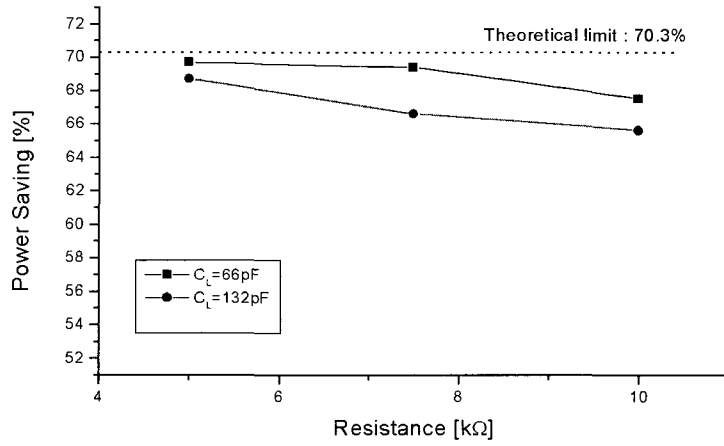


Fig. 15. Measured Power Saving Efficiency of Black Display with Load Condition

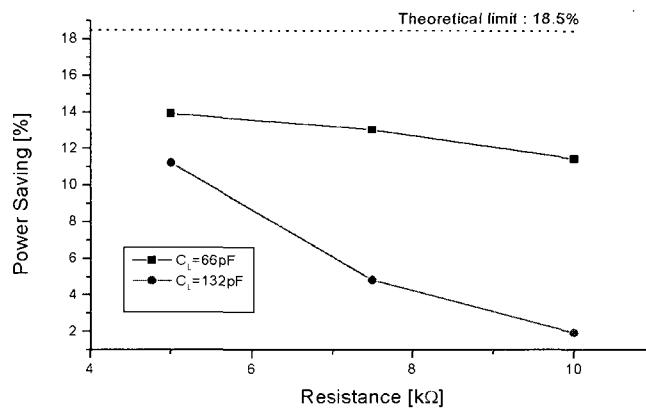


Fig. 16. Measured Power Saving Efficiency of White Display with Load Condition

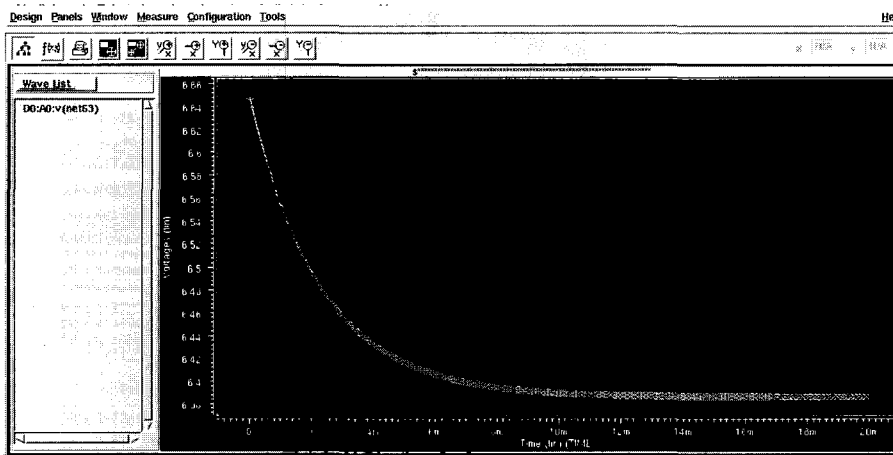


Fig. 17. Simulated Voltage Waveform of Tank Capacitor C<sub>T4</sub>

voltage range of Fig.4 is checked through HSPICE simulation. Fig.17 shows that the voltage of the tank capacitor C<sub>T4</sub> converges to about 6.38V from the initially charged 6.65V when the resistance and capacitance of a

data line are 10kΩ and 132pF respectively. The convergence voltage of the tank capacitors has been calculated by L."J." Svensson *et al.* [10]. Fig. 18 plots the voltage drop of the tank capacitor C<sub>T4</sub> with the

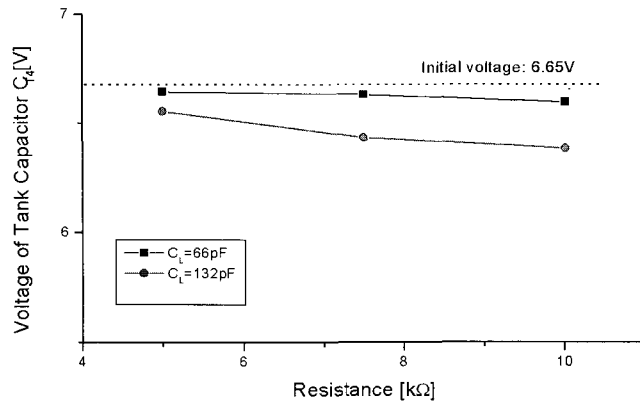


Fig. 18. Simulated Voltage Converge of Tank Capacitor  $C_{T4}$  with Resistance and Capacitance of a Data Line

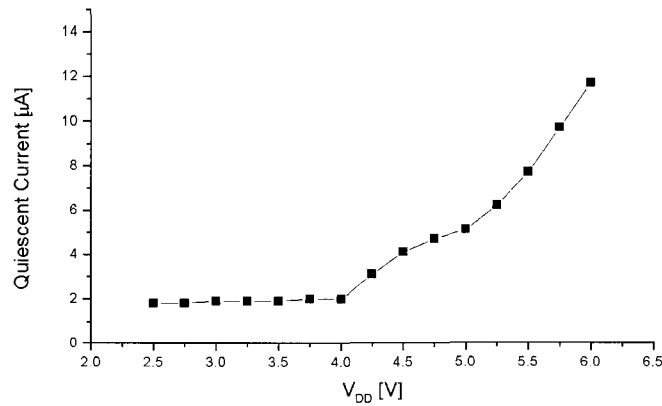


Fig. 19. Measured Quiescent Current of the Authors' Op-amp with Supply Voltage

resistance and capacitance of a data line. The plots explain the dependency of the power saving efficiency on the load condition.

**C. DC Power Saving**

The total DC power consumption of a conventional TFT-LCD,  $P_{DC,CONV}$ , can be easily calculated by using equation (9).

$$P_{DC,CONV} = N_{DATA} I_Q V_{DD} \tag{9}$$

where  $I_Q$  is a quiescent current of an Op-amp supplied by  $V_{DD}$ .

As explained in section III, half of the channels of Op-amps have a low voltage supply  $V_{DDL}$ . Therefore, the total DC power consumption using the proposed scheme,  $P_{DC,PROP}$ , can be obtained by using equation (10).

$$P_{DC,PROP} = \frac{N_{DATA}}{2} I_{QL} V_{DDL} + \frac{N_{DATA}}{2} I_{QH} V_{DDH} \tag{10}$$

where  $I_{QL}$  and  $I_{QH}$  are the quiescent currents supplied by  $V_{DDL}$  and  $V_{DDH}$  respectively.

As a result, the DC power saving efficiency can be obtained by dividing the equation (10) by the equation (9), resulting in the equation (11).  $I_Q$  and  $V_{DD}$  in equation (9) are the same as  $I_{QH}$  and  $V_{DDH}$  in equation (10) respectively.

$$\frac{P_{DC,PROP}}{P_{DC,CONV}} = \frac{I_{QL}V_{DDL} + I_{QH}V_{DDH}}{2I_{QH}V_{DDH}} \tag{11}$$

Fig. 19 plots quiescent currents with the supply voltage of the author's Op-amp[4] which was measured by using HP 4142B when the input voltage is half of

each supply voltage. If  $V_{DDH}$  is 5V and  $V_{DDL}$  is 2.5V, the quiescent current is 5.1 $\mu$ A and 1.8 $\mu$ A respectively. From equation (11), the DC power saving efficiency is 41.2%.

## V. CONCLUSIONS

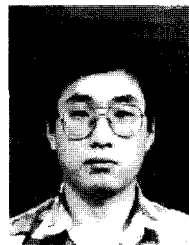
Since the largest power consumption source called the AC power in a TFT-LCD comes from driving data lines, the stepwise charging method was applied for reducing the AC power. Experimental results reveal that the AC power saving efficiency is over 75% for a 14.1 inch-diagonal XGA TFT-LCD when the number of step is 5 and each step time is 2 $\mu$  sec. Test chip was fabricated by using a 0.6 $\mu$  m standard CMOS process. Another major power consumption source is the DC power due to quiescent currents in Op-amps. Thus, we have also proposed a simple and efficient architecture of driver circuits for reducing the DC power. That is, two neighboring channels share two Op-amps, and one of the two Op-amps has a lower supply voltage. Experimental results showed that over 40% of the DC power in data drivers was reduced by using this method.

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