3-레벨 플라잉 커패시터 인버터를 위한 일반화된 Undeland 스너버 회로

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A Generalized Undeland Snubber for Flying Capacitor 3-level Inverter

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요 약

본 논문은 플라잉 커패시터 3-레벨 인버터 및 컨버터를 위한 스너버 회로를 제안하였다. 제안한 스너버회로는 Undeland 스너버를 기본 스너버로 사용하여 구성한 것으로서, 2-레벨 인버터에서 사용되어온 Undeland 스너버의 장점을 그대로 지니고 있다. 3-레벨 인버터 및 컨버터를 위해 제안한 스너버 회로와 기존의 RCD/RLD 스너버를 비교하면 1)사용소자의 수가 감소하며, 2) 낮은 과전압에 의한 스위칭 소자의 전압 스트레스가 감소하며, 3) 스너버 회로에서의 전력손실이 감소하여 전체 시스템에서의 효율이 개선된다. 본 논문에서는 제안한 스너버를 3-레벨 플라잉 커패시터 인버터에 적용하여 스너버 특성을 컴퓨터 시뮬레이션으로 분석하였으며 실험을 통해 제안한 스너버의 효용성을 입증하였다. 제안한 플라잉 커패시터 3-레벨 인버터 및 컨버터를 위한 스너버 회로를 구성하는 방법은 멀티레벨 인버터 및 컨버터에도 그대로 적용할 수 있다.

ABSTRACT

This paper proposes a snubber circuit for flying capacitor 3-level inverter and converter. The proposed snubber circuit makes use of Undeland snubber as basic snubber unit. It has such an advantage of Undeland snubber used in the two-level inverter. Compared with conventional RLD/RCD snubber for 3-level inverter and converter, the proposed snubber keeps such good features as fewer number of components, reduction of voltage stress of main switching devices due to low overvoltage, and improved efficiency of system due to low snubber loss. In this paper, the proposed snubber is applied to multilevel flying capacitor inverter and its feature is demonstrated by computer simulation and experimental result.

키워드: Multilevel inverter, Flying capacitor multilevel inverter, Snubber

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I. Introduction

The power converter, especially AC/DC PWM converter, DC/AC PWM inverter have been extending their range of use in industry because they provide reduced energy consumption, better system efficiency, improved quality of product, good maintenances and so on. In particular, the inverters and converters in such application areas as Static reactive compensator, active filter, high voltage DC transmission, FACTS and high voltage motor drive should be able to handle high voltage and large power. For this reason, two-level high-voltage and large-power inverters and converters have ever been designed with series connection of switching power devices such as BJT, GTO and IGBTs because the series connection allows reaching much higher voltages than the blocking voltages of the semiconductor devices. But the series connection of switching power devices have big problems, namely, non-equal distribution of applied device voltage across series-connected devices that may make the applied voltage of individual devices much higher than blocking voltage of the devices during transient and steady-state switching operation of devices.

As alternatives to effectively solve the above mentioned problem, several circuit topologiesof multilevel inverter and converter have been researched and utilized. In 1981 and 1991, diode-clamped multilevel inverter schemes were first proposed[1-2,7-8]. Succeedingly, in 1992, second flying capacitor multilevel inverters[3-4] and in 1996, third cascaded multilevel inverter were proposed[5-6]. These multilevel inverters can extend rated inverter voltage and power by increasing the number of voltage levels. They can also increase equivalent switching frequency without the increase of actual switching frequency, thus reducing ripple component of inverter output voltage and EMI effects.

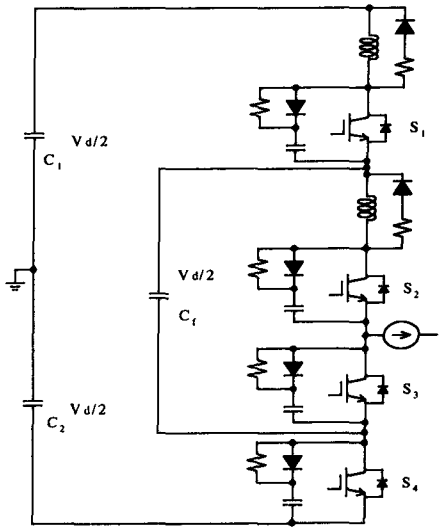


Fig. 1 Flying capacitor three-level inverter with conventional RCD/RLD snubber.

Among the above-mentioned multilevel inverter schemes, the flying capacitor multilevel inverter have good characteristics in terms of blocking voltage distribution among main switches, dv/dt and total harmonics distortion[7]. Thus in this paper we are to research for the snubber circuit of the flying capacitor multilevel inverter and converter. As shown in Fig. 1, conventional RCD/RLD snubber can be easily applied as the snubber of the flying capacitor multilevel inverter. But this kind of snubbers need separate snubber circuit unit for each main switching devices which are composed of turn-off capacitors, turn-on inductors, resistors and diodes. Thus the total number of snubber components become considerably high and complex, thus resulting in highly costly multilevel inverter and converter. And since the large amount of snubber energy is fully dissipated in snubber resistor, system power loss can be very high, which causes system efficiency to become very low. Furthermore, during turn-off process, the overvoltage of main switching devices can be very high, usually about 1.8 times higher than DC link voltage because there is only one small turn-off

capacitor for each switching devices to absorb the stored inductor energy.

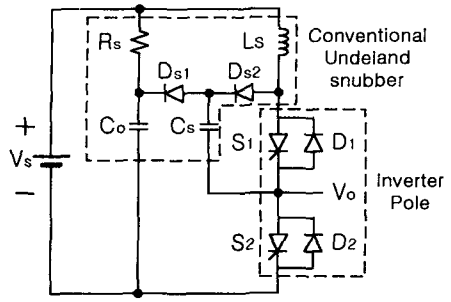


Fig. 2 Conventional Undeland snubber circuit.

To overcome the above-mentioned disadvantage of RCD/RLD snubber for flying capacitor multilevel inverter and converter, a new snubber topology suitable for flying capacitor multilevel inverter and converter are proposed. The proposed snubber utilizes Undeland snubber as basic snubber unit and can be regarded as a generalized Undeland snubber for flying capacitor multilevel structure converter. Its good features include fewer number of component, improved efficiency due to low loss snubber, capability of clamping overvoltage across switching main device. This paper also explains in detail how to construct a snubber circuit for multilevel inverter and converter.

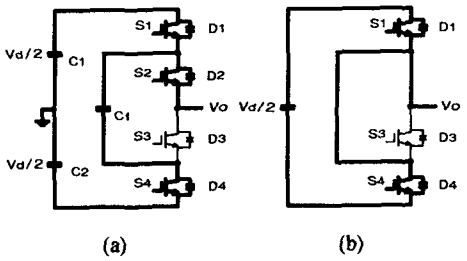
II. Principle of operation of Proposed snubber for Flying Capacitor Multilevel Inverter

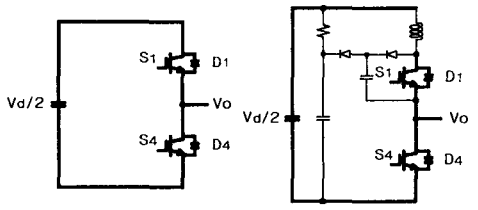
A. Review of Undeland Snubber as Basic Snubber Unit

Fig. 2 shows one inverter pole with the conventional Undeland snubber. In this paper, the Undeland snubber is to be utilized as basic snubber unit for multilevel inverter and converter [9]. As shown in Fig. 2, the snubber circuit consists of fewer components, which includes turn-off capacitor CS for dv/dt limitation, turn-on inductor LS for di/dt limitation, capacitor CO for overvoltage clamping and snubber energy recovery normally about ten times larger than CS, resistor RS for resetting snubber inductor and capacitor, and diodes. Such a simple circuit topology of Undeland snubber make itself good candidate for multilevel inverter and converter which essentially include a number of main switching device. In addition since the resistor R_S is not directly involved in snubbing action unlike RCD and RLD snubber, mechanical arrangements of components and cooling are much easier and simpler. In particular, Thanks to capability of clamping overvoltage at turn-off and no unbalance problem of overvoltage, the Undeland snubber can beselected as the best basic snubber unit for flying capacitor multilevel inverter and converter.

B. Snubber Derivation for Flying Capacitor Multilevel Inverter

A flying capacitor m-level multilevel inverter typically consists of m-2 flying capacitors on the DC bus side and produces m-levels of the phase voltage. For convenience, in this paper we will mainly consider the flying capacitor three-level inverter. Of course, all the concept handled here can equally apply to flying capacitor multilevel inverter of other levels. Fig. 3(a) shows one pole of three-level inverter in which the DC bus consists of DC link capacitor C1 and C2, and flying capacitor C_f. For a DC bus voltage V_d, the voltage across





(c) (d)

Fig. 3 Derivation of the proposed snubber for 3-level flying capacitor inverter. (a) Operating part of circuit (thick line), during level changes between Vd/2 and 0, (b) Redrawn circuit of (a), (c) Equivalent two-level inverter, (d) Equivalent circuit with Undeland snubber unit.

Table 1 Switching states and output voltage levels

switching state	S_1	S_2	S_3	S_4	output voltage Level
P	ON	ON	OFF	OFF	$V_d/2$
Zp	ON	OFF	ON	OFF	0
Zn	OFF	ON	OFF	ON	0
N	OFF	OFF	ON	ON	$-V_d/2$

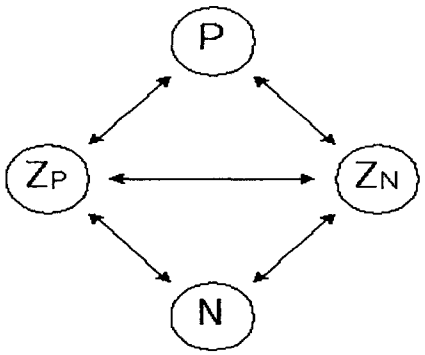


Fig. 4 Possible switching state transitions of flying capacitor three-level inverter pole.

the flying capacitor is Vd/2 and each device stress will be limited to Vd/2 through the flying capacitor. Table 1 lists the switching state, the output voltage levels and their corresponding switch on/off conditions. The voltage levels are Vd/2(P level), 0(Z level: Zp, Zn) and -Vd/2(N level). Notice that the level changes occur only between adjacent levels as shown in Fig. 4. Speaking in more detail, the level changes between voltage level P and Z is like P→Zp→P→Zn→P···. The level changes between voltage level Z and N are like N→Zp→N →Zn→N···. In case of staying on Z switching state, the level changes occurs alternately between Zp and Zn states. Under any switching sequences, the reason to insert the Z switching states Zp and Zn alternately is to maintain the DC voltage of flying capacitor constant. Among the voltage level changes, we can find that there exists two complementary switch pairs. The complementary switch pair is defined such that turning on one of the pair switches excludes the other from being turned on. In case of three-level inverter, the two complementary pairs are (S1, S4) and (S2, S3)

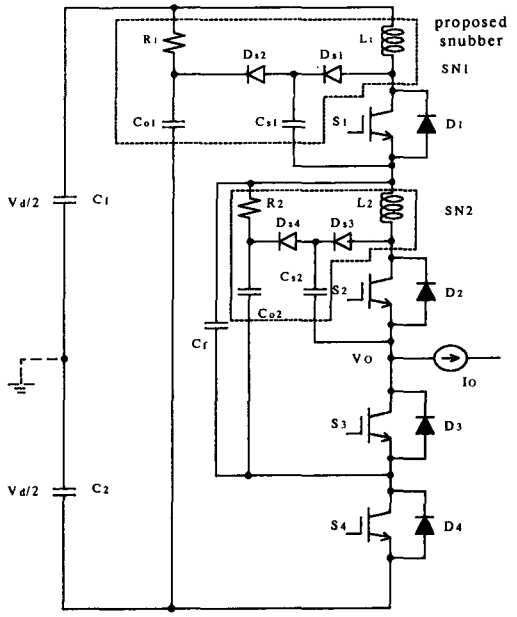


Fig. 5 Flying capacitor Three-level inverter equipped with proposed snubber.

For example, in case of switching state transition between P and Zn, we can find the operating part of circuit during each level change to converge to equivalent two level inverter which is composed of complementary pair switches(S1,S4) and flying

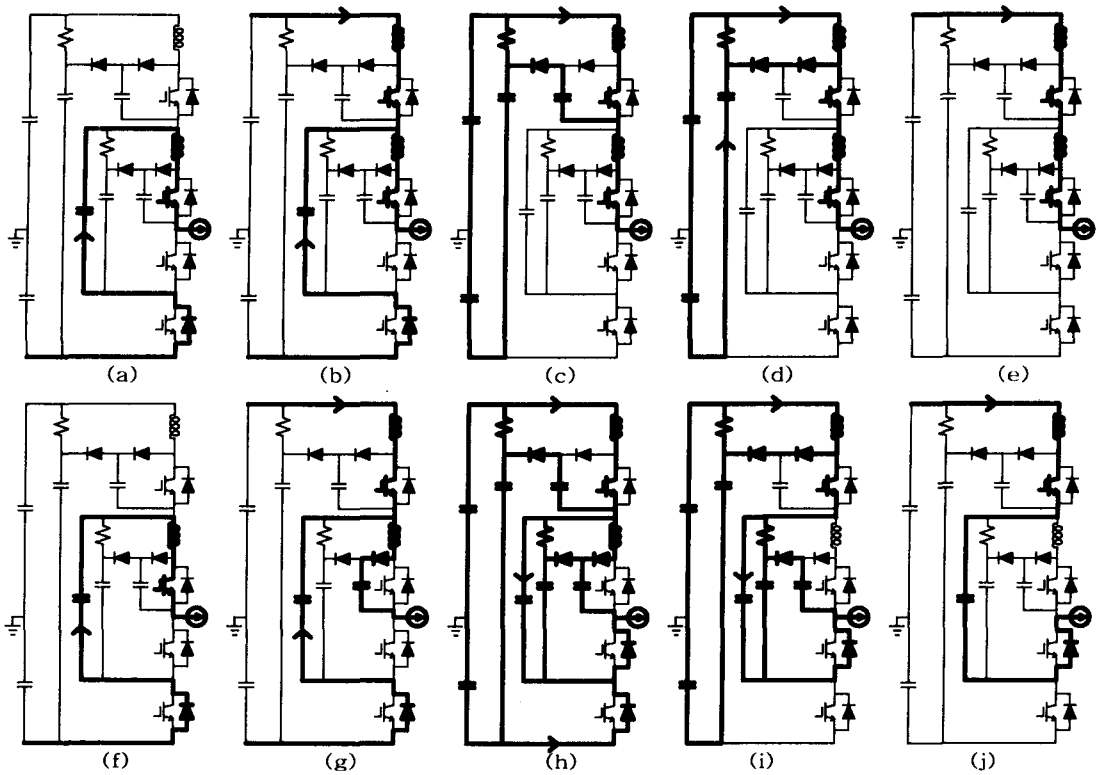


Fig. 6 operation modes of proposed snubber during switching state transitions from Zn to P (mode (a)-(e)), and from Zn to Zp (mode (f)-(j)).

capacitor. During the level changes the operating components of five-level inverter can be drawn with thick line as shown in Fig. 3(a) where S1 and S4 make turn-on and off operation, and S2 is always on and S3 is always off. The thick-lined part of operating circuit can be transformed into Fig. 3(b) and can also be redrawn as Fig. 3(c) since switch S2 remains turned on irrespective of on/off condition of S1 and S4. Fig. 3(c) shows that the operating part of circuit is equivalent to the conventional two-level voltage source inverter. It follows that for the equivalent two-level inverter related to switching devices (S1, S4), the basic snubber unit which has been used in two-level inverter can be applied as shown in Fig. 3(d). In the same way, the equivalent two-level inverter corresponding to the other complementary pair(S2, S3) in three-level inverter can be derived, and the same basic snubber unit can apply to that. So, we can obtain three-level inverter equipped with the proposed snubber circuit as shown in Fig. 5.

When using the same principle, we can get the snubber circuit for other multilevel inverter. Furthermore, a generalized snubber for any multilevel inverter and converter can be achieved. The generalized snubber has the same good features as the basic snubber unit. In this paper since we use the Undeland snubber as the basic snubber unit, the characteristics of the generalized snubber are such as fewer number of component, improved efficiency due to low loss snubber, capability of clamping overvoltage across switching main device and easy arrangements and mounting of snubber circuit. Furthermore thanks to the

snubber structure, the generalized snubber has no unbalance problem of overvoltage unlike RCD/RLD snubber, thus resulting in equal voltage stress to all main switching device.

III. DESCRIPTION OF OPERATION MODES OF PROPOSED SNUBBER

Even if the proposed snubber can apply to any level of flying capacitor multilevel inverter and converter, let me explain here the case of three level converter only for convenience. In case of three level flying capacitor inverter pole, there are several transitions of switching states among switching states P, Zp, Zn, and N as shown in Fig. 4. Only the operation modes of proposed snubber in two transitions of switching states, that is, from Zn to P and from Zn to Zp are described in detail in this section. The operations in the other transitions can be explained in the similar way.

A. switching state transition from Zn to P

At the beginning of this transition, the initial switching state is Zn as shown in Fig. 6(a), so that switches S2 and S4 are on, and S1 and S3 are off. And also the initial voltages of VCS1 and VCS2 are Vd/2 and zero, respectively while the initial voltages of VCO1 and VCO2 are Vd and Vd/2, respectively. The transition to switching state P is initiated by turning on switch S1 and turning off switch S4. By doing so, the inductor iL1 current through L1 as shown in Fig. 6(b) increases linearly from zero to load current iO while the current iD4 though D4 decreases linearly at the same rate. As iL1 (iD4) reaches iO (zero), the capacitor voltage vCS1 starts to discharge through the current path CS1-DS2-R1-L1 like Fig. 6(c). Of course, during the discharging interval, the switch voltage vS4 across S4 increases sinusoidal, thereby making sure snubbing action on turned-off diode D4. When the discharging capacitor voltage vCS1 becomes equal to zero, the snubber diode DS1 is turned on like Fig. 6(d). As the inductor current iL1 approaches the load current iO, the switching state moves to P as shown in Fig. 6(e), thus completing the switching state transition from Zn to P.

B. switching state transition from Zn to Zp

At the beginning of this transition, the initial switching state is Zn as shown in Fig. 6(f), so that switches S2 and S4 are on, and S1 and S3 are off. The transition to switching state Zp is initiated by turning on switches S1 and S3, and turning off switches S2 and S4. By doing so, the inductor iL1 current through L1 as shown in Fig. 6(g) increases linearly from zero to load current iO while the current iD4 though D4 decreases linearly at the same rate. And also the capacitor voltage vCS2 increases linearly by the load current iO. As iL1 reaches iO and vCS2 reaches Vd/2, the operating mode becomes like Fig. 6(h) where two snubbers SN1 and SN2 operate independently. At snubber SN1, the capacitor voltage vCS1 discharges to zero through the current path CS1-DS2-R1-L1 while at snubber SN2, the inductor current iL2 reduces to zero, thereby approaching the operating mode of Fig. 6(i). As the inductor current iL1 approaches the load current iO and the capacitor voltage vCO2 approaches Vd/2, the switching state moves to Zp as shown in Fig. 6(j), thus completing the switching state transition from Zn to Zp.

IV. SIMULATION RESULTS

In order to prove the effectiveness of the proposed snubber circuit, A simulation for 3-level inverter equipped with the proposed snubber circuit is carried out. Only one pole of the 3-level inverter was simulated as shown in Fig. 5 with the output terminal VO connected to the midpoint of input source voltage Vd through series-connected R-L

load. The used simulation tool is PSPICE 8.0 version. The simulation conditions are as follows:

V_d = 400 [V]
L_S = 25 [μH] C_S = 1 [μF]
C_O = 40 [μF] R_S = 5 [Ω]
fs = 780 [Hz]

Since the proposed snubber utilizes Undeland snubber as basic snubber, the snubber circuit parameters are determined according to their conventional design method. Table 2 shows that the proposed snubber requires lower number of snubber circuit elements than that of conventional snubber. The number of snubber diodes of proposed snubberis 2 smaller than that of RCD/RLD snubber. The number of snubber resistors of proposed snubber is 4 smaller than that of RCD/RLD snubber. In addition, in case of snubber capacitor, since two of the snubber capacitors in proposed snubber is used as overvoltage clamping devices, the proposed snubber is regarded as 2 less number of snubber capacitor. Thus the total number of snubber components is 8 less than that of

Table 2 Comparison of the number of devices

	C	L	Diode	R	Total
RCD/RLD	4	2	6	6	18
Proposed	4	2	4	2	12

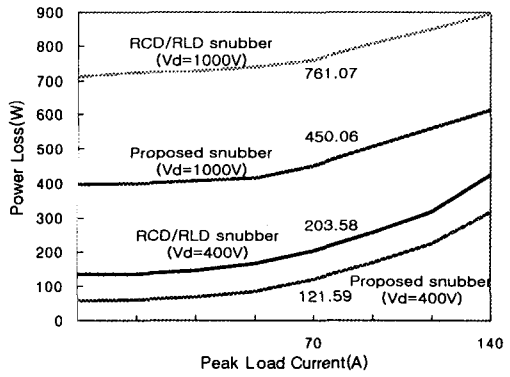


Fig. 7 Power losses in snubber resistors.

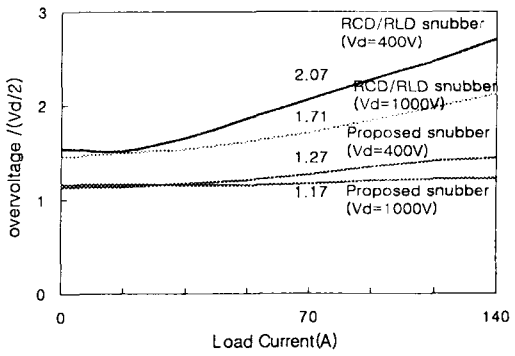


Fig. 8 Maximum overvoltage in main switching devices.

RCD/RLD snubber. In order to compare characteristics of the proposed snubber with those of conventional RCD/RLD snubber, both snubbers are simulated under comparison conditions of the same turn-on inductor value and turn-off capacitor value, which provide identical di/dt and dv/dt values to both snubbers. Fig. 7 shows the snubber loss of proposed snubber compared with that of conventional RCD/RLD snubber. It proves that the proposed snubber make system efficiency improved by about 40% at 70A load current level. As the DC link voltage is increased as in practical case from 400 to 1000[v], the system efficiency can be shown to improve because of increase of the stored snubber energy at snubber capacitors CS1 and CS2. Fig. 8 shows the overvoltage of main switches in both proposed and conventional snubber. As shown in Fig. 8, the overvoltage of main switches in proposed snubber is reduced 1/2 or 1/3 times as good as that of main switches in conventional RCD/RLD snubber. This characteristics make it possible for the circuit designer to select lower rating of devices.

Fig. 9, 10, and 11 show the simulation results under the same time base so that the overall operation of the proposed snubber can be understood easily. Fig. 9 shows PWM-related reference signal Vr1 and Vr2, triangular waveforms

T1, and overall output voltage and current waveforms. The PWM gate signals G1 and G2 which are generated by comparing reference signal and triangular signals apply for switches S1 and S2 respectively, and their complemented signals also apply for switches S4 and S3, respectively. The output voltage and current waveforms shown in the third plot have good waveforms with no adverse effects of the proposed snubber.

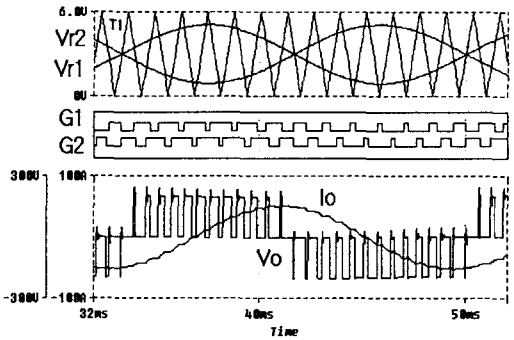


Fig. 9 PWM generation-related signals(first plot and second plot) and overall output voltage Vo and current Io waveforms during one fundamental period(third plot).

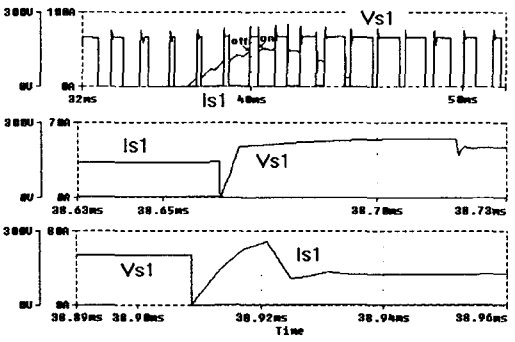


Fig. 10 Voltage Vs1 and current Is1 of switch S1 (first plot), zoomed waveforms during turn-off interval(second plot) and turn-on interval(third plot).

Fig. 10 shows the simulated voltage v_{S_1} and current i_{S_1} of switches S_1(first plot), also their detailed(zoomed) waveforms during turn-off(seccond)

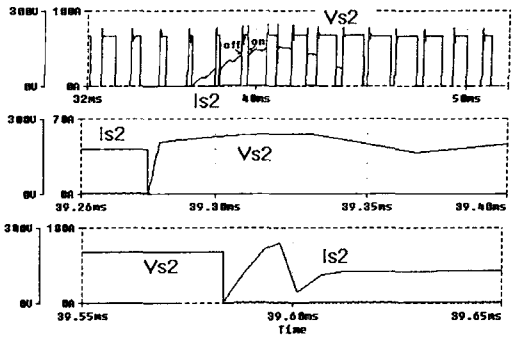


Fig. 11 Voltage Vs2 and current Is2 of switch S2(first plot), zoomed waveforms during turn-off interval(second plot) and turn-on interval(third plot).

plot) and turn-on(third) intervals, respectively. Fig. 11 also show the simulated waveforms in case of switch S2. They prove that the proposed snubber circuit have good snubbing effects on main switches in terms of transient switching peak values, dissipative power and snubber losses.

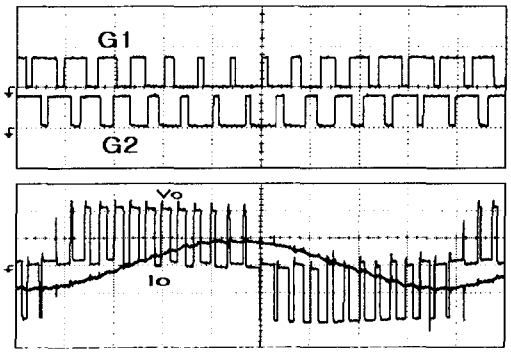
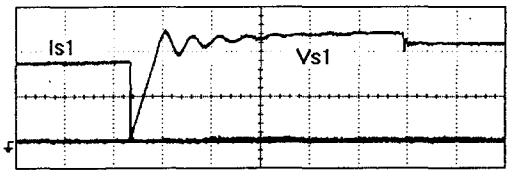


Fig. 12 Measured PWM gate signals G1, G2 of switches S1, S2(first plot), Overall output voltage Vo and current Io waveforms(second plot) [100V/div, 50A/div, 2mec/div].



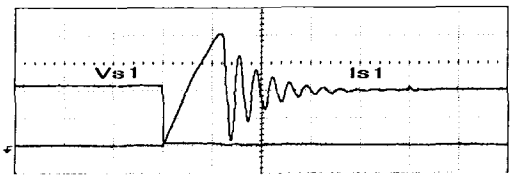


Fig. 13 Voltage and current waveforms of switch S1 during turn-off interval(first plot), Voltage and current waveforms of switch S1 during turn-on interval (second plot) [100V/div, 20A/div, 10μs/div].

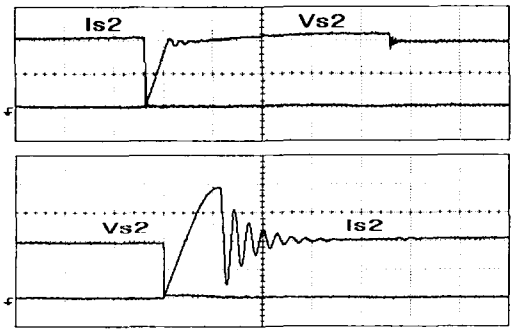


Fig. 14 Voltage and current waveforms of switch S2 during turn-off interval(first plot), Voltage and current waveforms of switch S2 during turn-on interval (second plot) [100V/div, 20A/div, 10μs/div].

V. EXPERIMENTAL RESULTS

In order to verify the operation of the proposed snubber circuit, one pole of 3-level inverter was properly implemented with rated power 8[kw] and output current 40[A]. The prototype inverter is controlled through triangular waveform carrier-based PWM operation with carrier frequency 780[Hz]. The inverter with the proposed snubber circuit utilizes IXYS IGBT MII(MID, MDI)100-12A3 of current rating 135[A] for main switches S1-S4, IXYS DSEI 2×31-06C for snubber diodes DS1 and DS2, ferrite core inductor of 25[μH] for snubber inductors L1 and L2, and polypropylene capacitor of 1[μF], 400[v] for snubber capacitors CS1 and CS2, polypropylene capacitor of 40[μF], 400[v] for snubber capacitors CO1 and CO2, snubber resistors R1 and R2 5[Ω]. The switching devices IGBT as main switches are used to check only the operation of the proposed snubber circuit. The DSP TMS320F240 is used to implement inverter controller as PWM generator.

Fig. 12 shows the measured PWM gate signals G1 and G2 of switches S_1 and S_2, and overall output voltage v_o with respect to neutral point N and current i_o waveforms. Fig. 13 shows the measured voltage v_{S_1} and current i_{S_1} of switches S_1 during turn-on interval and turn-off interval. Fig. 14 shows the measured voltage v_{S_2} and i_{S_2} current of switches S_2 during turn-on and turn-off intervals. It shows that the proposed snubber results in the good waveforms around the main switches S_1, S_2, S_3 and S_4 in terms of limiting the di/dt and dv/dt values and reducing switching losses. It also proves that the proposed snubber circuit have good snubbing effects on main switches and diodes in terms of transient switching peak values, dissipative power and snubber losses. Since the snubber for the main switches S_1, S_2, S_3 and S_4 is similar to Undeland snubber, the measured results are as good as those of Undeland snubber.

VI. CONCLUSION

This paper proposes a new efficient snubber circuit for flying capacitor 3-level inverter and converter. The snubber circuit makes use of Undeland snubber as basic snubber unit and can be regarded as a generalized Undeland snubber. The proposed snubber keeps such good features as fewer number of components, improved efficiency due to low snubber loss, capability of clamping overvoltage across main switching device. Compared with the conventional RCD/RLD snubber for flying capacitor multilevel inverter, the advantages of the proposed converter can be summarized

as follows:

1) the reduced number of the snubber components,

2) the low switch stress due to reduction of over voltage during switching transients,

3) efficiency improvements of overall system due to recovery of snubber losses

Furthermore, the proposed concept of constructing a snubber circuit for flying capacitor 3-level inverter and converter can easily apply to any level of multilevel converters.

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