Progress in Superconductivity Vol.3 No.1 pp87-90 31 October 2001

Design and Fabrication of High Temperature Superconducting Rapid Single Flux Quantum T Flip-Flop

J. H. Kim[*,a], S. H. Kim [a], K. R. Jung[+,b], J. H. Kang [c], G. Y. Sung [a]

[a] *Electronics and Telecommunications Research Institute, Taejon, Korea*

[b] *Korea Institute of science and Technology, Seoul, Korea*

[c] *University of Inchon, Inchon, Korea*

고온 초전도 단자속 양자 T 플립 플롭 설계및 제작

김준호[*,a], 김상협[a], 정구락[+,b], 강준희[c], 성건용[a]

Abstract

We designed a high temperature superconducting rapid single flux quantum(RSFQ) T flip-flop(TFF) circuit using Xic and WRspice. According to the optimized circuit parameters, we fabricated the TFF circuit with $Y_1Ba_2Cu_3O_{7-x}$(YBCO) interface-controlled Josephson junctions. The whole circuit was comprised of five epitaxial layers including YBCO ground plane. The interface-controlled Josephson junction was fabricated with natural junction barrier that was formed by interface-treatment process. In addition, we report second design for a new flip-flop without ground palne.

Keywords : RSFQ, T flip-flop, $Y_1Ba_2Cu_3O_{7-x}$, Josephson junctions

I. Introduction

Rapid-single-flux-quantum(RSFQ) circuits have attracted much attention because of their high speed operation and low power consumption[1]. Recently, the record of operation speed for T flip-flop approached 770GHz, using Nb trilayer junctions and electron beam lithography for a minimum junction area patterning less than $0.1\mu m^2$[2]. However, considering the operation speed is proportional to the I_cR_n value, RSFQ circuit using high-T_c superconductor that is expected to have larger I_cR_n is more desirable for high speed electronics.

Until now, the fabrication technology for uniform high-T_c superconducting junction has not been established while reproducible fabrication process for uniform low-T_c superconducting junctions has been developed. The inhomogeneous artificial barrier layer along the junction area was supposed to result in large I_c spread in junctions, which was not suitable for large integrated electronic circuit application. However, recently developed interface-engineered junction(IEJ) process adopted fabrication of natural barrier by ion bombardment and vacuum annealing instead of using artificial barrier[3]. The development of IEJ process has improved junction uniformity very much and NEC group has achieved I_c spread

*Corresponding author. Fax: +82 42 860 6836

e-mail: jhk@etri.re.kr

+Present address: Korea Photonics Technology Institute, Kwangju, Korea

as low as 8% of 1σ for 100 junctions by using interface-treated process[4].

In this paper, we report two designs of T flip-flop circuits with and without ground plane, respectively. And we discuss each features of two designs.

II. Experiments

a. The first design and fabrication

Before fabrication of T flip-flop, we designed and simulated circuit varying inductance, bias current, and I_c's of junctions. Fig. 1 shows the equivalent circuit of the fabricated T flip-flop. Josephson transmission line(JTL) and T flip-flop are two main parts in the circuit, where six Josephson junctions were used. Input signal is injected into the T flip-flop through JTL.

Using WRspice and Lmeter, we optimized circuit parameters. The optimized circuit parameters are as follows. BF1=BB1=0.5mA, BF2=BB2=0.9mA, IL=0.95mA, IF=0.85mA, IB=-0.1mA, L6=0.96pH. Margins of I_c in junction, inductance, and bias currents were obtained as in Table1.

Based on these simulations, we fabricated a T flip-flop circuit. $SrTiO_3$(STO) single crystal was used as substrate for fabrication of T flip-flop. First, for ground layer 300nm thick YBCO was deposited on STO substrate by pulsed laser deposition(PLD). After ground layer patterning, insulating

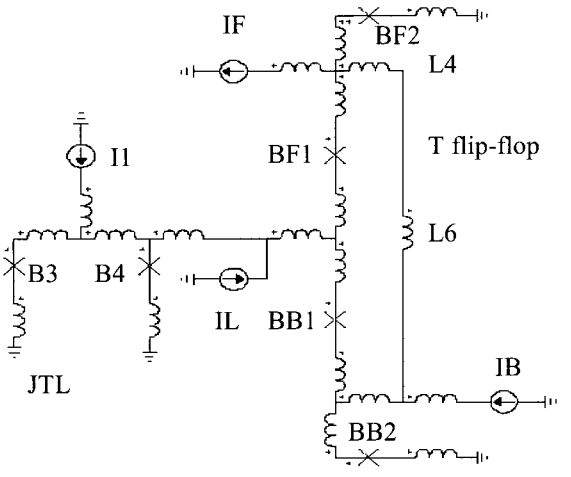

Fig. 1. Equivalent electric circuit of T flip-flop.

Table 1. Margins of T flip-flop circuit that was designed as the first version.

	Center	-margin(%)	+margin(%)
BF1	0.5mA	22	14
BF2	0.9mA	14	7
BB1	0.5mA	28	10
BB2	0.9mA	9	9
B3	1mA	34	104
B4	1mA	15	58
IL	0.95mA	26	30
IF	0.85mA	27	22
IB	-0.1mA	200	60
L6	0.96ph	45	129

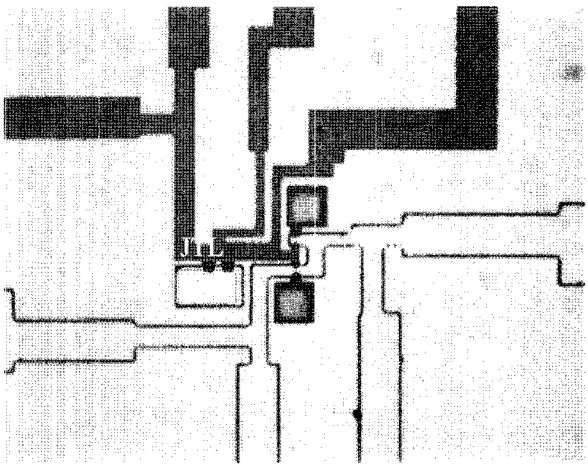

Fig. 2. Optical micrograph of T flip-flop circuit that was fabricated according to our first design.

Sr_2AlTaO_6(SAT) layer was deposited. Through the photolithography and Ar ion milling, via holes to the ground YBCO layer were made. Then, YBCO base electrode and SAT insulating layer were deposited successively with thickness of 200nm and 300nm, respectively. Next, using photolithography and Ar ion milling, the ramp-edge whose surface was damaged by the Ar ion bombardment was formed. Then, after 30min. annealing under oxygen atmosphere, 200nm thick YBCO counter electrode was deposited successively. Finally, Ag/Au was deposited for electrode contact pad. The detailed

description for fabrication of Josephosn junction is reported elsewhere[5]-[6].

Fig. 2 shows an optical micrograph of a fabricated T flip-flop. The junction width in T flip-flop is 2.5 ㎛ for small one and 4.5 ㎛ for large one. We measured I-V curves of all the six Josephson junctions. Even though we got RSJ-like I-V curves of Josephson junctions without ground plane, all the six junctions showed flux-flow type I-V curves. This indicates that fabrication of ramp-edge Josephson junction with ground plane is somewhat different from that without ground plane.

b. The second design and layout

We designed another T flip-flop that would be fabricated without ground plane. In this case, we reduced I_c's of junctions in T flip-flop, assuming the reduction of the leakage current in real junctions. Fig. 3 is simulation result of newly-designed circuit.

When an input pulse is injected into the circuit, BB2 that was already biased is switched and immediately BF1 is switched. When next pulse is injected, BF2 and BB1 are switched. This pair switching is typical operation of T flip-flop. When we monitor the output pulse at BB2(or BF2), we get signal at every other input pulse. If we measure the output and input pulse for some time periods, the average dc voltage of output is half of that of input.

Through the optimization process with WRspice and Lmeter, we obtained margin values for circuit parameters. Table 2 shows margins of circuit parameters for the second design. The decrease of I_c's of junctions in T flip-flop induced the increase of loop inductance, L6, and the improvement of margin balance. The inductance of T flip-flop without ground plane will be increased in comparison with that of the T flip-flop with ground plane. However, the optimized inductance centering at 2pH with margin –50%~80% does not make it severe problem.

According to the results of new simulations, we made a new layout with Xic. Fig. 4 shows our new layout of T flip-flop without ground plane. In our new layout, "Bottom YBCO I" plays a role of ground plane. "Bottom YBCO I" is electrically isolated from

Table 2. Margins of T flip-flop circuit that was designed as the second version.

	Center	-margin(%)	+margin(%)
BF1	0.3mA	33	40
BF2	0.54mA	15	22
BB1	0.3mA	27	40
BB2	0.54mA	19	19
B3	1mA	35	40
B4	1mA	40	35
I1	0.9mA	44	33
IL	0.5mA	80	48
IF	0.62mA	16	19
IB	-0.16mA	50	75
L6	2pH	50	80

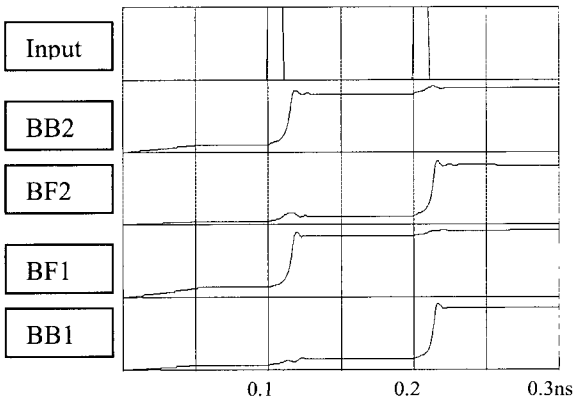

Fig. 3. Simulation result of our second T flip-flop circuit.

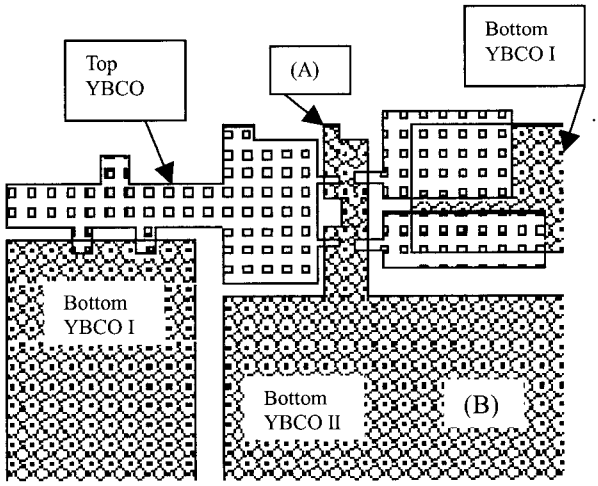

Fig. 4. Layout of a T flip-flop without ground plane.

"Bottom YBCO II". For the ground of BB2 and BF2, we made two large pads that are overlapped with "Bottom YBCO I". This method of making T flip-flop without ground plane is already used by Saitoh et al.[7]. Bias currents IF and IB are supplied through "(A)" and "(B)", respectively.

III. Summary

We have designed and fabricated a T flip-flop with ground plane. However, I-V characteristics showed flux-flow type, although we obtained RSJ-like I-V curves from Josephson junction without ground plane. We guess that fabrication condition should be modified to get good junction characteristics in T flip-flop with ground plane. For example, a new insulation layer such as CeO_2 may be adopted for good oxygen mobility.

On the other hand, we designed a new T flip-flop circuit that does not need a ground plane. However, the storage loop inductance of junction without ground plane is expected to be increased. So, in our new design, by reducing I_c's of junction, we got larger loop inductance ranging from 1~3.6pH. Comparing with first designs, the margins of circuit parameters are a little bit widened in our new design. We implemented two isolated bottom layers in a new T flip-flop layout. "Bottom layer I" plays a role of ground plane, and "Bottom layer II" is for formation of serial junctions in T flip-flop. We believe that this new T flip-flop circuit without ground plane will work better than our first T flip-flop.

Acknowledgement

The authors would like to thank Ms. Mi Ran Jin for her technical assistance. This work was supported in part by the Korea Research Council for industrial science and technology and the Ministry of Science and Technology, Rep. of Korea. The work at University of Inchon was partly supported by the Korea Science and Engineering Foundation through the Multimedia Research Center at University of Inchon.

References

[1] K. K. Likharev and V. K. Semenov, "RSFQ logic/memory family: a new Josephson junction technology for sub-terahertz clock frequency digital systems," IEEE Trans. on Appl. Supercond., 1, 3-28(1991).

[2] W. Chen, A. V. Rylyakov, V. Patel, J. E. Lukens, K. K. Likharev, "Rapid single flux quantum T-flip flop operating up to 770 GHz," IEEE Trans. on Appl. Supercond. 9, 3212-3215(1999).

[3] B. H. Moeckly and K. Char, "Properties of interface-enginnered high Tc Josephson junctions," Appl. Phys. Lett. 71, 2526-2528(1997).

[4] T. Satoh, M. Hidaka and S. Tahara, "High-temperature superconducting edge-type Josephson junctions with modified interfaces," IEEE Trans. on Appl. Supercond. 9, 3141-3144(1999).

[5] G. Y. Sung and J. H. Kim, "Fabrication of interface-controlled Josephson junction using Sr_2AlTaO_6 insulating layers," IEEE Trans. on Appl. Supercond. 11, 151-154(2001).

[6] S. H. Kim, J. H. Kim, and G. Y. Sung, "The improvement of properties of interface-controlled junctions by ion milling and annealing process," Proc. 8th Intern. Supercond. Electronic Conf. (ISEC'01), 251 (2001).

[7] K. Saitoh, Y. Soutome, T. Fukazawa, Y. Tarutani, and K. Takagi, "Voltage divider operation using high-Tc superconducting interface-engineered Josephson junctions," Appl. Phys. Lett. 76, 2606-2608(2000).