A Novel EST with Trench Electrode to Immunize Snab-back Effect and to Obtain High Blocking Voltage

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A vertical trench electrode type EST has been proposed in this paper. The proposed device considerably improves snapback which leads to a lot of problems of device applications. In this paper, the vertical dual gate Emitter Switched Thyristor (EST) with trench electrode has been proposed for improving snab-back effect. It is observed that the forward blocking voltage of the proposed device is 745V. The conventional EST of the same size were no more than 633V. Because the proposed device was constructed of trench-type electrodes, the electric field moved toward trench-oxide layer, and the punch through breakdown of the proposed EST is occurred at latest.

Keywords : Trench Eelctrode, Latch-up, Snab-back, on-state voltage drop, Forward Blocking Voltage

1. INTRODUCTION

Power transistors used in Power Integrated Circuits (PIC's) are generally required to have low on-resistance, fast switching speed, and high breakdown voltage. Silicon-On-Insulator (SOI) Lateral Insulated Gate Bipolar Transistor (LIGBT) has several advantages such as complete dielectric isolation, high packing density and high switching speed. However, one of the biggest problems of LIGBT is the latch-up of a parasitic thyristor. IGBTs have an inherent thyristor structure that is composed of p+ anode – n- drift region – p- base – n+ cathode. A MOS gate does not control the electron currents when latch-up occurs. Latch-up due to the parasitic thyristor limits the maximum operating current of IGBTs [1]. Therefore, the prevention of latch-up is very important when designing power transistors with wide SOA (Safe Operating Area).

In order to increase latch-up current density, several IGBT structures such as deep p+ implantation under the n+, reverse channel and p+ diverter have been proposed. Previous studies could reduce the voltage drop due to hole currents in the p-base region and increase the latch-up current density. In spite of previous efforts the latch-up of parasitic thyristor remains a key problem that limits the maximum operating current of LIGBTs.

Recently, a Lateral Trench-gate IGBT (LTIGBT) with improved the latch-up characteristics was proposed. LTIGBT is an effective structure to increase the latching current density as the p base length under n+ cathode layer is controlled [2-6]. However the LTIGBT is not driven in scaling down because that the length of n-drift layer cannot be reduced due to rating voltage.

In this paper, we proposed a Lateral Trench Electrode IGBT(LTEIGBT) in which the length of the n-drift layer was no more than 19 ㎛. Currently, the length of the n-drift layer of the conventional LIGBT and LTIGBT was over 80 ㎛, and the electrodes of LTEIGBT were replace with trench-type ones. Numerical simulations on the latch-up current densities were shown in comparison with those of the same sized conventional LIGBT and LTIGBT. And the characteristics of LTEIGBT such as forward blocking, turn-off and on state were investigated by numerical simulations and compared with those of the conventional LIGBT and LTIGBT. Moreover, we investigated how the length of p+ cathode layer, SOI thickness and buried oxide thickness affected the latch-up current density, forward blocking voltage and forward voltage drop of the LTEIGBT.

2. DEVICE STRUCTURE AND OPERATION

Fig. 1 illustrates the conventional EST and the proposed lateral trench electrode EST. And the main difference between conventional EST and the proposed EST is the placement of the cathode and the gate electrode.

With zero gate bias, the device operates in the forward blocking mode and the junction formed by the p-base and the n- drift regions supports any applied positive anode voltage. The device can be turned on by application of a positive gate bias to create a channel. Electrons from the cathode flow through the channel. This provides the base current for the pnp transistor in the main thyristor. Holes are injected from the p+ anode into the n- drift regions. Prior to the main thyristors latch-up, these holes flow beneath the floating n+ emitter region into the cathode electrode via the base resistance. Under these condition, the device operates like an IGBT. As the current is increased, the n+/p-base junction of npn transistor becomes sufficiently forward-biased to latch-up the main thyristor.

The integration of the MOSFET and the thyristor results in a parasitic thyristor. This parasitic thyristor can latch up at high current densities resulting in loss of gate control. The latch-up of the parasitic thyristor is determined by the resistance of the p-base region under the n+ cathode layer. The injection of electrons from the n+ emitter of the parastic thyristor is suppressed by shorting it to the p+ cathode region.

3. SIMULATION AND RESULTS

The I-V characteristics of both the proposed EST and the conventional EST are shown in Fig. 2. The conventional EST exhibits snapback with the anode voltage and current density 2.73V and 6.4A/㎠, respectively. Note that the proposed trench electrode EST exhibits snapback at 1.21V that is, as expected, a relatively low anode voltage at 18.4A/㎠ that is higher than the conventional one. It is inferred that this higher anode current density of the proposed one results from n+ floating region shorter than the conventional structure, leading to lower lateral resistance component. However, since the length through which the current flows becomes shorter and large currrent flows even at low voltage, the snapback of the proposed device occurs at about a half voltage as high as the conventional one.When the thyristors are operating properly, the current flowlines of the conventional device and the proposed one are illustrated in Fig. 3. As shown in Fig. 3, before the parasitic thyristors are in effect, both thyristors are operating by the current which is flowing through p+ anode, n+ buffer, n drift, p floating and n+ floating region in turn all the way to the cathode electrode. The proposed trench electrode EST device is also operating as a thyristor like the conventional one.

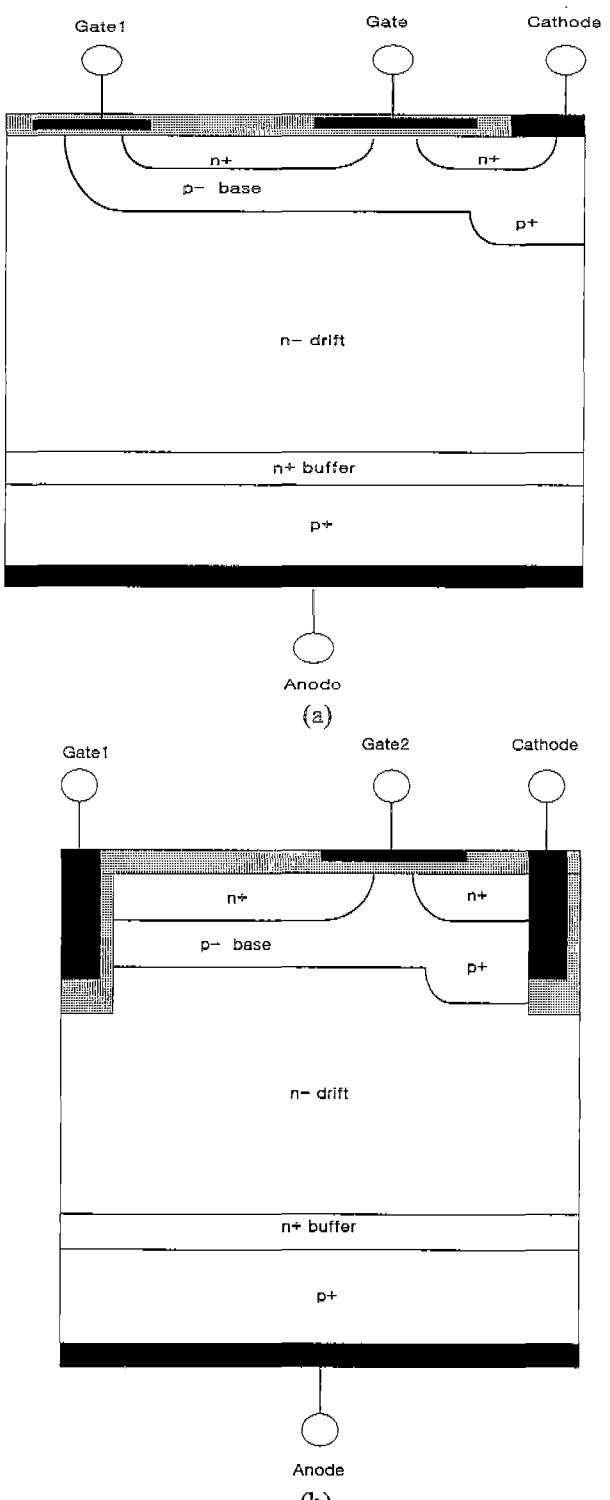


Fig. 1. The structure of the conventional and the proposed Dual Gate EST (a) the conventional Dual Gate EST (b) the proposed Dual Gate EST.

Table 1. Design parameter for simulation.

	Width (μm)	Depth (μm)	Concent rat-ion (cm^{-3})
n-drift region	40	55	1×10^{14}
n+ cathode region	10	0.5	1×10^{21}
n+ floating region	18	0.5	1×10^{20}
p- base region (n+ floating)	22	2.5	1×10^{16}
p+ cathode region	8	3.5	1×10^{18}
p+ anode region	40	1.5	1×10^{21}
n+ buffer region	40	3.0	1×10^{18}
Trench oxide layer	5	6	
Gate oxide		0.05	
Channel length	5		

When latch-up occurs, The current flowlines of each device are shown in Fig. 4. Both devices have more holes which move into the p- base region of the cathode as the anode voltage is increased. Thus, main operation of the devices is due to parasitic thyristor operation caused by latch-up rather than thyristor operation.

The breakdown characteristics of the forward blocking region are shown in Fig. 5. With a voltage of 0V applied to the gate electrode, the breakdown voltage was measured by increasing the anode voltage. In the case of the conventional vertical EST, the breakdown occurred at the anode voltage of 633V. On the other hand, the proposed vertical EST was found to have the breakdown voltage of 745V which was improved by 110V compared to that of the conventional one. It is inferred that since the electric field applied to the conventional device is distributed on the whole, the punch-through breakdown of the conventional one is lower than that of the proposed one whose electric field is concentrated on the trench oxide layer. When the depth of the proposed device is designed to become 200 ㎛, the breakdown voltage maintains 1200V.

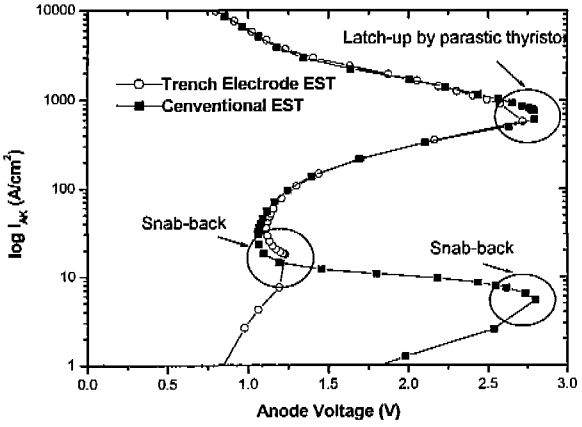


Fig. 2. I-V Characteristics of the devices.

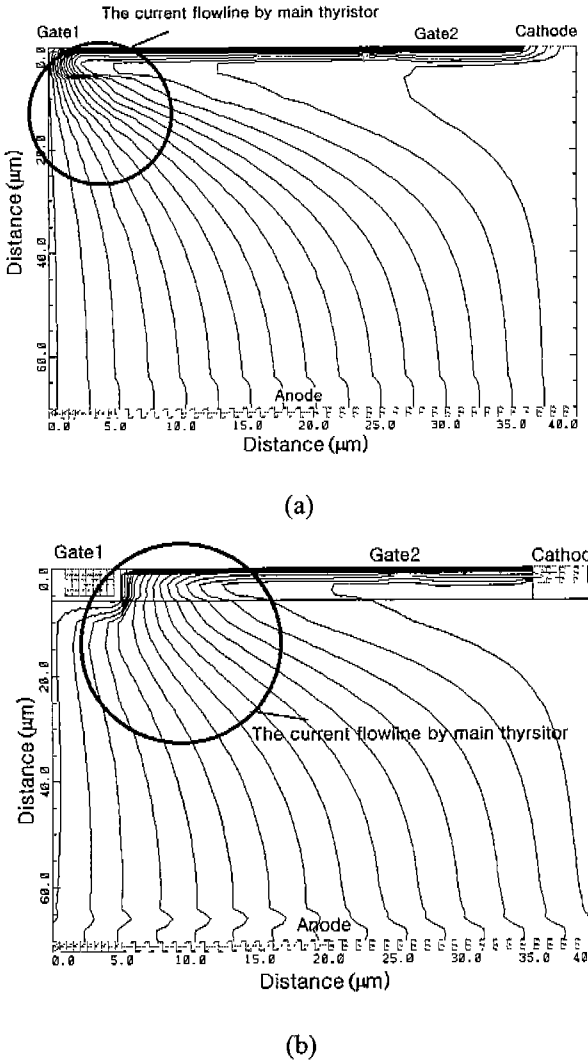
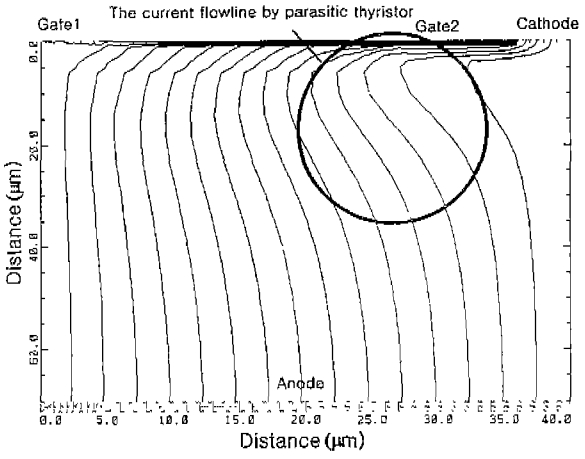
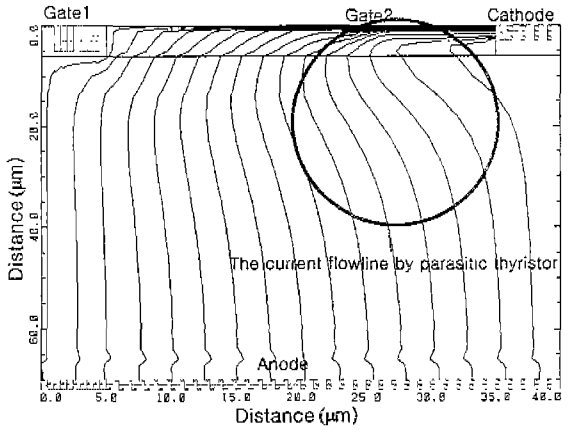


Fig. 3. When the devices are on-state, flowline of the devices (I_A=10 A/cm^2) (a) the conventional DG EST (b) the proposed DG-EST.



(a)



(b)

Fig. 4. When the latch-ups are occurred, flowline of the devices (a) the conventional DG EST (b) the proposed DG-EST.

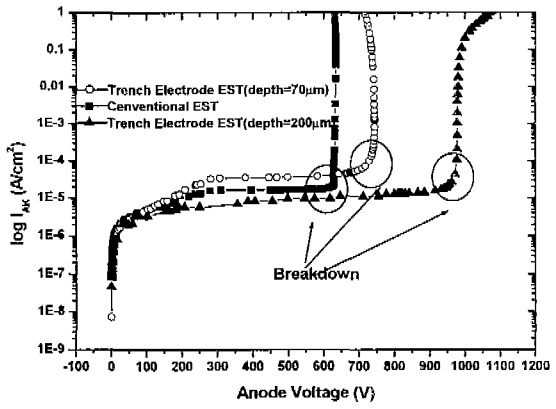
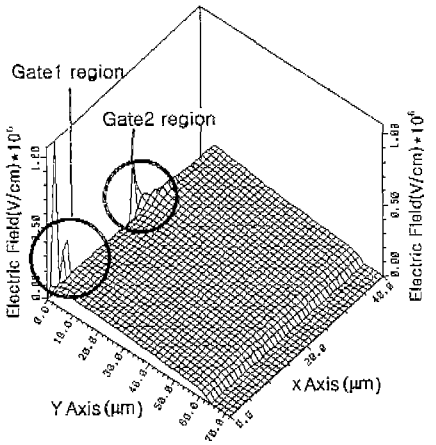
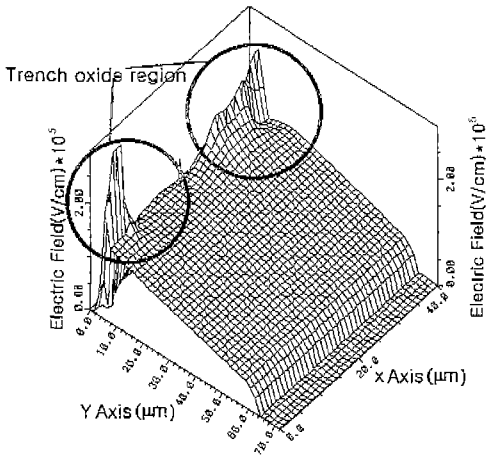


Fig. 5. The breakdown characteristics of the devices at the forward blocking mode.



(a)



(b)

Fig. 6. When the breakdown is occurred, the electric field distribution of the devices (a) the conventional DG-EST (b) the proposed DG-EST.

Thus, this application is expected to put on spurs to a field of a tolerance for high voltage. In addition, since the conventional electrode is replaced by the trench type with the same size and then the breakdown voltage of the proposed structure is improved considerably, the control over the concentration of p-base is expected to be facilitated to improve snapback.

The 3-dimensional electric filed distribution of each device is illustrated in Fig. 6. As expected, when the breakdown of the conventional device occurs, the whole electric field is distributed throughout the device. On the other hand, the whole electric field applied to the proposed device is concentrated strongly on the trench oxide layer. On the basis of this result, if trench

electrode-type EST devices are fabricated like previously reported trench electrode-type LIGBTs, vertical ESTs maintaining high tolerance with the same size will be able to be fabricated.

4. CONCLUSION

A vertical trench electrode type EST has been proposed in this paper. The proposed device considerably improves snapback which leads to a lot of problem of device application. In addition, It can maintain a wide safe operation region like the conventional device since latch-up caused by the parasitic thyristor occurs at the almost same current density, The simulation confirmed that it has high tolerance for more than 110V compared to the conventional one. If ESTs with a tolerance for high voltage are fabricated and trench electrode ESTs which is more useful than the conventional structure can be utilized, They could greatly contribute to high voltage and current power semiconductor market.

ACKNOWLEDGMENT

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