The Effect of Manipulating Package Construct and Leadframe Materials on Fracture Potential of Plastically Encapsulated Microelectronic Packages During Thermal Cycling

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It was studied in the present work how the thermal cycling performance of LOC (lead on chip) packages depends on the package construct or leadframe materials. First, package body thickness and Au wire diameter were manipulated for the selection of proper package design. Secondly, two different types of leadframe materials (i.e. copper and 52%Fe-48%Ni alloy) were tested to determine the better material for improved reliability margin of plastically encapsulated microelectronic packages. This work shows that manipulating package body thickness was more effective than an increase of Au wire from 23㎛ to 33㎛ for the prevention of wire debonding failure. Further, this work indicates that the LOC packages including the copper leadframes can be more susceptible to thermal cycling reliability degradation due to chip cracking than those including the alloy leadframes.

Keywords : plastic package, LOC, leadframe, Au wire, cracking failure, numerical calculation

1. INTRODUCTION

As microelectronic packages continue to be thinning, their performance and reliability become increasingly influenced by the ultimate difference in thermal expansion between packaging materials[1-4]. Accordingly, it is important to understand how an alternating sequence of structurally and physically dissimilar packaging materials interacts to cause thermal stress-related damage within the plastically encapsulated microelectronic package, in particular during temperature cycling. This work was done to understand how thermal cycling performance and reliability margin of plastic LOC (lead on chip) packages are affected by manipulating packaging materials or package design.

2. EXPERIMENTS

All of the test specimens were prepared through the conventional LOC packaging process where the top surface of the chip is directly attached to the area of the leadframe with a double-sided adhesive tape[4]. Fig. 1 shows a LOC construct. The predetermined chip size was 0.65x1.5 ㎠ and the predetermined package size was 0.8×1.7 ㎠. All LOC packages compromise a sequence of 300 ㎛ for the Si chip and 150 ㎛ for the leadframe in thickness. However, the thickness of the package body was grouped into two categories; 1000 ㎛ and 2500 ㎛. Gold wires were used for interconnects in plastic-encapsulated microcircuits. The diameter of the gold wires was also grouped into two categories; 23 ㎛ and 33 ㎛ (as shown in Fig. 2). Further, two different sets of the leadframes (i.e. copper and 52%Fe-48%Ni alloy) were adopted to study the dependence of package reliability on leadframe material selection. The reliability test performed in the present study was confined to thermal cycling. All test specimens underwent thermal displacement-induced fatigue: a temperature range from -65℃ to +150℃ and a 30 minute time period[4]. Predetermined time to validate reliability was 1000 cycles. For each set of experiments, nominally identical specimens were placed in the thermal cycle chamber, then individual was cross-sectioned after 1000 cycles and inspected under an optical microscope and scanning electron microscope to identify the failure region.

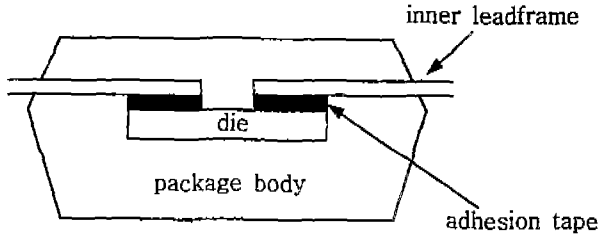

Fig. 1. Schematic of a LOC package construct.

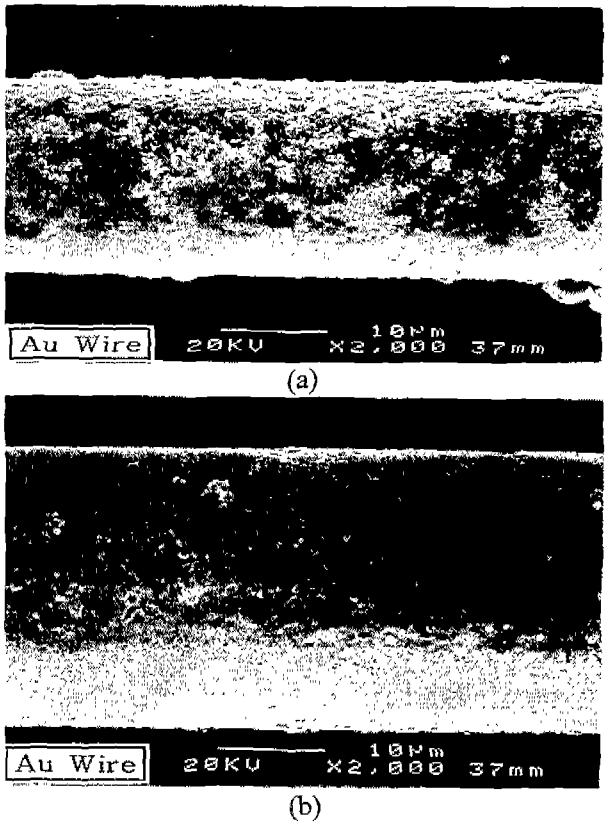

Fig. 2. Scanning electron micrographs of gold wires: a) wire diameter is 23 ㎛; b) wire diameter is 33 ㎛.

Fig. 3. Top view of one test specimen after thermal cycling of 1000 cycles.

3. RESULTS

LOC packages, whose thickness is 1000 ㎛ and leadframe material is copper, were first subjected to thermal cycling. All test specimens were cross-sectioned after thermal cycling of 1000 cycles. Fig. 3 is a scanning electron micrograph showing the top view of one test specimen. This micrograph shows a crack running parallel along the package edge that is a typical damage behavior in moisture-induced packages[3]. In general, such a crack initiates from the bottom corner of the chip (or chip support paddle) within the package body due to the disparities in the coefficients of thermal expansion among packaging materials that are contained within a plastic package. Delamination between a die support paddle and its underlying package body has been known to be responsible for the initiation of such moisture-induced package cracking[5]. In the LOC packages tested in the present work, delamination between the bottom surface of the chip and its underlying package body was more often observed because the bottom surface of the chip is directly attached to its underlying package body without using a chip support paddle. Fig. 4 is a scanning electron micrograph showing delamination formed along the interface between the bottom surface of the silicon chip and its underlying package body. Thermal cycling then allows stress to concentrate at a tip of the delamination due to thermal expansion mismatch among packaging materials, eventually leading to crack initiation. The prevention of package cracking due to such delamination requires the reduced disparities in the coefficients of thermal expansion among packaging materials. In the present study, the thickness of the package body was decreased from 2500 ㎛ to 1000 ㎛ and two different leadframe materials were adopted to compare the effect for suppressing thermal stress-related damage in the LOC packages.

When copper is used as leadframe materials, much more cracking failures were observed for the LOC packages having a thickness of 1000 ㎛ than those having a thickness of 2500 ㎛. On the other hand, when 52%Fe-48%Ni alloy is used as leadframe materials, no cracking failure was observed for the LOC packages having a thickness of 1000 ㎛. Fig. 5 is a graph showing the number of thermal stress-induced failure as a function of package thickness for two different leadframe materials. When 52%Fe-48%Ni alloy is used as leadframe materials, delamination along the interface between the chip and its underlying package body was hardly observed for the LOC packages having a thickness of 1000 ㎛. These results indicate that the

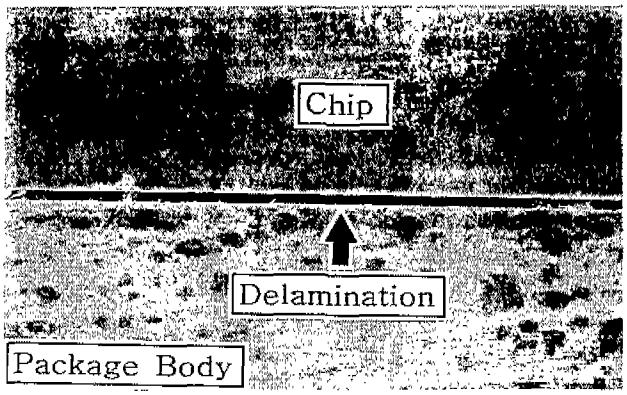

Fig. 4. A Scanning electron micrograph showing delamination along the interface between the chip and its underlying package body.

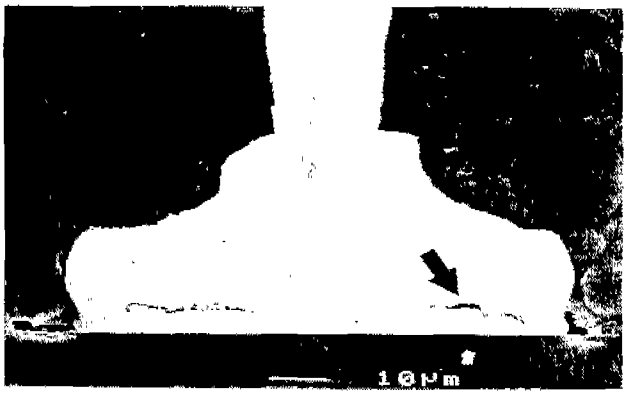

Fig. 6. Scanning electron micrograph showing wire debonding failure due to thermal expansion mismatch between the chip and leadframe.

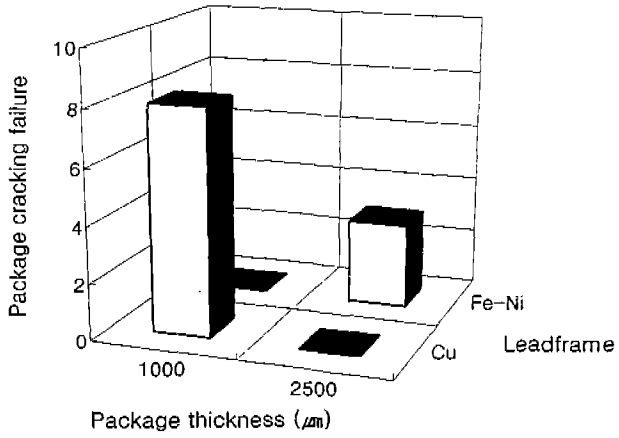

Fig. 5. Number of package cracking failure as a function of package thickness for two different leadframe materials.

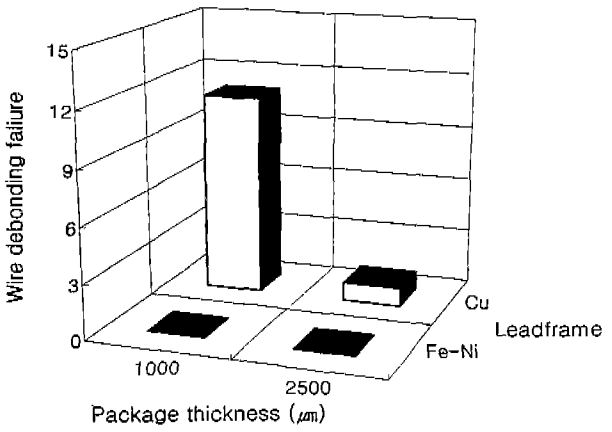

Fig. 7. Number of wire debonding failure as a function of package thickness for two different leadframe materials.

thinner package body including the alloy leadframe exhibits better thermal cycling reliability.

It has been also investigated how leadframe material selection or package thickness control influences debonding failure of a wire attached to a metal pad of the active chip surface. Fig. 6 shows the cross-sectional view of a wire partially-debonded from a metal pad after thermal cycling of 1000 cycles. Fig. 7 shows the number of wire debonding failure as a function of package thickness for two different leadframe materials. When copper is used as leadframe materials, the number of wire debonding failure is decreased to 1/10 for the LOC packages having a thickness of 2500 ㎛, compared with the LOC packages having a thickness of 1000 ㎛. However, the use of 52%Fe-48%Ni alloy as leadframe materials results in no wire debonding failure, regardless of package thickness. The effect of wire enlargement on debonding failure was also tested. Fig. 8 shows the dependence of wire debonding failure on wire diameter for the LOC packages that are assembled with the copper leadframe. Even though an increase of wire diameter from 23 ㎛ to 33 ㎛ considerably reduces the number of debonding failure, it is not so effective as much as an increase in package thickness from 1000 ㎛ to 2500 ㎛. These results show that the proper combination of leadframe material and package thickness contributes to the reduction of wire debonding failure as well as package cracking failure in the LOC packages. In this example, for the LOC packages having a thickness of 1000 ㎛, it is preferable to select the alloy leadframe for the suppression of wire debonding failure as well as package cracking failure.

2-dimensional mechanical simulation was also performed in order to estimate the extent which cracking potential in LOC packages is reduced by the

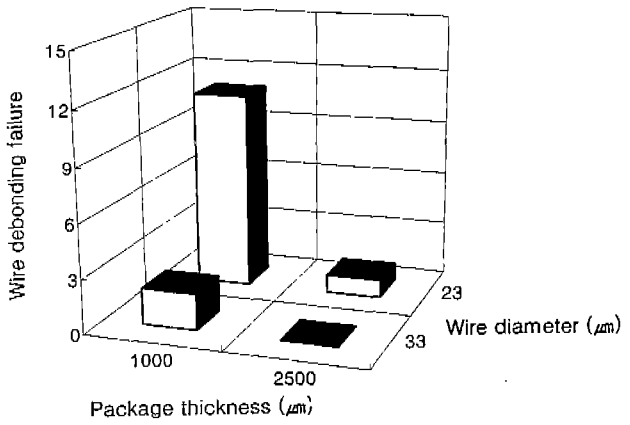

Fig. 8. Number of wire debonding failure as a function of wire diameter and package thickness.

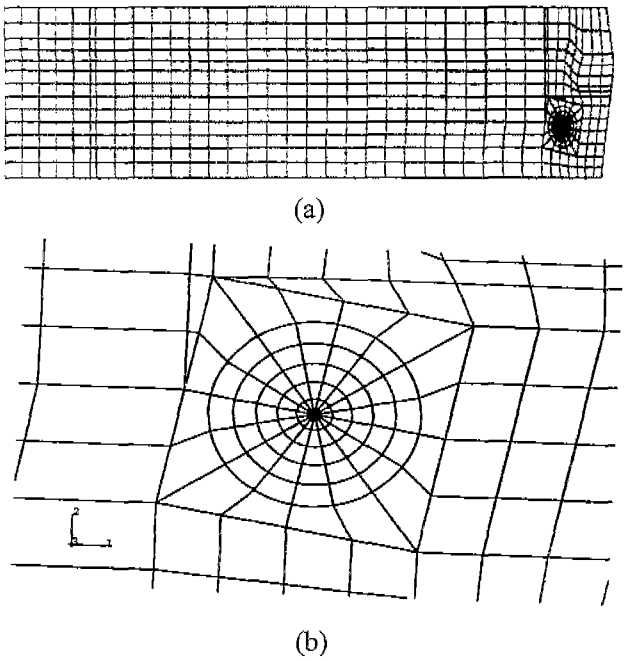

Fig. 9. 2-dimensional mesh of one half of the LOC package: a) one half of the package construct; b) close-up of the delamination tip.

appropriate design of the package structure or the proper selection of leadframe materials. The finite element model of a LOC package was developed using the mesh generation program PATRAN and converted into an ABAQUS input file[6]. Since the actual dimensions of the LOC package were used in the computer-aided calculations, more than 5,000 noded elements were required for modeling. Fig. 9 shows 2-dimensional meshes of one half of the LOC package construct. The present numerical calculation was done under an assumption that there exists delamination between a chip and its underlying package body. Cracking potential at a tip of delamination was then expressed by a value of J integral. The resulting calculation shows that in a case of the LOC packages having a thickness of 1000 ㎛, the maximun value of J integral (which designates a degree of cracking potential) is 0.12MPa-㎜ for the copper leadframe and 0.08MPa-㎜ for the alloy leadframe. This calculation agrees well with the experimental result showing that the use of Fe-Ni alloy as the leadframe material is more effective than the use of the copper leadframe for the suppression of cracking failure of the LOC packages having a thickness of 1000 ㎛.

Consequently, in a case of the LOC package having a thickness of 1000㎛, the amount of plastic resin to encapsulate the chip is too small to accommodate thermal expansion mismatch between the leadframe and the chip. Accordingly, in such thin LOC packages, cracking potential is determined by thermal expansion mismatch between the chip and the leadframe rather than that between the chip and the plastic package body. Note that copper has a coefficient of thermal expansion of 17ppm/℃, while that of silicon is about 2.6ppm/℃ and that of a typical 52%Fe-48%Ni leadframe is around 4.5ppm/℃. So, when the packages cool down from 150℃ to - 65℃, thermal displacement mismatch (due to temperature difference of 215℃) will be larger for the copper leadframe. The resulting cracking potential in such thin packages is higher for the copper leadframe having the larger disparity in the coefficient of thermal expansion with the silicon chip. Thus, an increase of package thickness is required for allowing the package body to have sufficient elasticity to compensate for thermal expansion mismatch between the copper leadframe (α=17ppm/℃) and the silicon chip (α =2.6ppm/℃).

4. SUMMARY

In the LOC packages, in which the use of the copper leadframe is essential for the enhanced electric speed, a thickening of the plastic package body was required for the prevention of thermal cycling reliability degradation due to chip cracking. Further, an increase of package body thickness was more effective than an increase of Au wire from 23㎛ to 33㎛ in reducing the number of wire deboding failure. Consequently, the appropriate design of the plastically encapsulated package structure may lead to improved reliability margins which provide practical guidance for the proper selection of leadframe materials.

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