A Study on Characterization and Modeling of Shallow Trench Isolation in Oxide Chemical Mechanical Polishing

Sang-Yong Kim*

ANAM Semiconductor Co., LTD, 222-1, Dodang, Wonmi, Buchon, Kyunggi, 420-130, KOREA

Hun-Sang Chung School of Electrical & Electronic Engineering, Chosun University, 375, Seosuk-Dong, Kwangju, 501-759, Korea

E-mail: ksy@aaww.com

(Received 23 May 2001, Accepted 31 July 2001)

The end point of oxide chemical mechanical polishing (CMP) have determined by polishing time calculated from removal rate and target thickness of oxide. This study is about control of oxide removal amounts on the shallow trench isolation (STI) patterned wafers using removal rate and thickness of blanket (non-patterned) wafers. At first, it was investigated the removal properties of PETEOS blanket wafers, and then it was compared with the removal properties and the planarization (step height) as a function of polishing time of the specific STI patterned wafers. We found that there is a relationship between the oxide removal amounts of blanket and patterned wafers. We analyzed this relationship, and the post CMP thickness of patterned wafers could be controlled by removal rate and removal target thickness of blanket wafers. As the result of correlation analysis, we confirmed that there was the strong correlation between patterned and blanket wafer (correlation factor: 0.7109). So, we could confirm the repeatability as applying for STI CMP process from the obtained linear formula. As the result of repeatability test, the differences of calculated polishing time and actual polishing time was about 3.48 seconds. If this time is converted into the thickness, then it is from 104 Å to 167 Å. It is possible to be ignored because process margin is about 1800 Å.

Keywords: Chemical Mechanical Polishing (CMP), Shallow Trench Isolation (STI), blanket (non-patterned), End Point Detection (EPD), removal rate (RR), correlation factor

1. INTRODUCTION

Shallow trench isolation (STI) is an enabling technology for the fabrication of advanced Sub-0.25 micron integrated devices.[1, 2] Requirements for STI planrization are much more severe than those for interplanarization. dielectric (ILD) mechanical polishing (CMP) has been accepted in recent years as a critical step in mainstream IC fabrication technology, and has enabled the fabrication of the multilevel interconnect up to 5 or 6 metal levels. However, for STI planarization, CMP is "essential", but typically insufficient by itself in meeting all the requirements. As the devices scale down, the trench filling becomes more difficult due to its high aspect ratio, thus the key issues are the optimized thickness control.

For the most of oxide CMP process, end point

detection (EPD) has been depend on the polishing time. It could be calculated from removal oxide thickness divided by removal rate[3,4]. Because of continually changeable process condition according to consumable. for example, polishing pad quality, the removal rate of the blanket wafer which have linear characteristics must be constantly monitored and applied during CMP process [5,6]. To apply the removal rate of the blanket wafer for calculating polishing time need to analyze correlation of polished oxide amount between the blanket and the pattern wafer. [7, 8] In this work, we investigated the correlation between blanket and STI patterned wafer to ensure STI CMP process conditions. such as effective thickness condition and accurate polishing time. So, the removal target oxide of blanket wafer can be determined by using analyzed result. The post CMP thickness is converted into removal target oxide of blanket wafer, and the converted removal target oxide is used for determining the polishing time to control the target of post CMP thickness. The difference between calculated polishing time and actual polishing time was 3.48 second.

2. EXPERIMENTS

The polishing experiment was performed on an IPEC 472 chemical mechanical polisher with optimized process conditions. The VERTEQ A2S cleaning system were used for the post CMP cleaning. Also, the polyurethane based polishing pad and silica based slurry were used for the polishing. The plasma enhanced chemical vapor deposition (PECVD) tetra-ethyl orthosilicate (TEOS) wafers and specific STI pattern wafers of 200 mm were used for the experiments. The oxide thickness was measured before and after CMP as polishing time using a film thickness measurement tool, NANO M8000. The step height and total indicated range (TIR) were measured on pattern wafers as polishing time using a Tencor P30 Profilermeter. Below items are summarized for each experiments.

2.1. Oxide removal property as a function of polishing time

The blanket wafer with PECVD TEOS of 16000 Å and two STI patterned wafers were polished in good order at intervals of 20 second. The polished oxide thickness of the blanket wafer was measured with 49 points with 7 mm edge exclusion at intervals of 20 second, and that of field oxide trench and moat nitride (Si₃N₄) of pattern wafer were measured and analyzed. The step height and TIR on 120 μ m large trench in the middle of 7 \times 7 μ m dummy moat array of the pattern wafer.

2.2. Repeatability test and correlation analysis

Each thickness data, strictly speaking, polishing amount of blanket and STI pattern wafer was collected with 85 lots that were polished on the same polishing condition. And, the repeatability test of 50 lots performed to confirm the analyzed result.

3. RESULTS AND DISCUSSION

3.1. Oxide removal property as a function of polishing time

Figure 1 shows the thickness reduction as a function of polishing time in the PECVD-TEOS blanket wafer of 16000 Å. As the polishing time increases, the oxide thickness linearly decreases. Figure 2 and Figure 3 shows the reduction of the field oxide thickness and

moat nitride thickness in the pattern wafer, respectively. The thickness was slowly reduced in the polishing time between 0 second and 40 seconds (step 1), and then the thickness was little abruptly reduced to 60 seconds (step 2), again slowly reduced in the polishing time between 60 seconds and 100 seconds (step 3). The step 1 of Figure 2 means that shook (shark's fin) structure in the edge of field oxide was polished. Because the measured points are in the center of field oxide, the thickness change looks like a little bit. The step 2 of Figure 2 means the real polishing step. The removal rate of step 3 was again reduced because the polishing step meets to Si₃N₄ of moat region. The removed nitride amount in step 1 of Figure 3 is the smaller than other steps which contact to most nitride film directly. The mechanical removal effect in this step is very small because there is no any touch directly between polishing pad and wafer. There is a only chemical effect in this step 1. The moat nitride thickness reduced rapidly in the polishing time of above 60 seconds (step 2 and 3), because of dishing effect. Figure 4 shows the step heights as a function of polishing time in the STI patterned wafers. The step height was rapidly decreased to polishing time of 40 seconds. The lowest step height was observed in the polishing time from 40 seconds to 60 seconds. Figure 5 Figure 6 shows the cross sectional SEM photographs in pre- and post-CMP planarization, respectively.

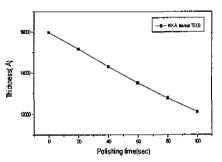


Fig. 1. Thickness reduction as polishing time in 16000 Å PECVD TEOS blanket wafer.

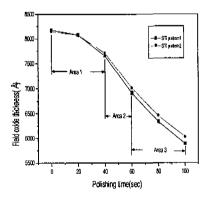


Fig. 2. Field oxide thickness reduction as polishing time in STI pattern wafer.

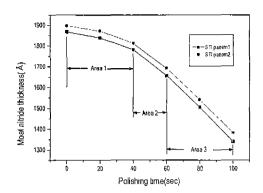


Fig. 3. Moat nitride thickness reduction as polishing time in STI pattern wafer.

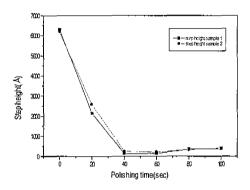


Fig. 4. Step height as a function of polishing time.

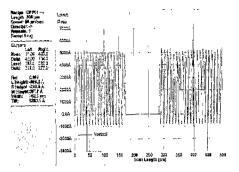
3.2. Repeatability test and correlation analysis

As the polishing time is increased, the oxide thickness of the blanket wafer is linearly decreased (See Figure 1), but the thickness reduction of STI patterned wafer didn't show the linear change (See Figure 2 and 3).

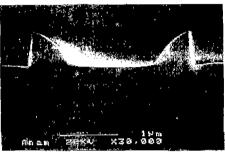
Thus, we carried out repeatability test of total 85 lots to analyze the correlation for oxide removal amounts between the blanket and STI patterned wafer. Figure 7 shows the analyzed correlation for oxide removal amounts between the blanket and STI patterned wafer. It has a strong correlation (correlation factor: 0.7109). And this correlation formula can be shown with linear function as follows;

$$Y = 0.9871 \times X + 1649.7 (R=0.7109)$$

Where, X is the required removal oxide target amount in the pattern wafer, Y is the removal oxide amount target in the blanket wafer.

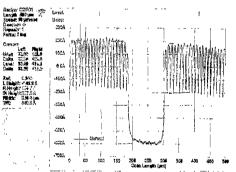


(a) Profiling at 0 [sec] of polishing time

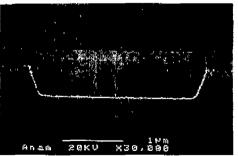


(b) Cross Sectional SEM Photograph.

Fig. 5. Pre-CMP planarization, (a) profiling at 0 [sec] of polishing time, (b) cross sectional SEM photograph.



(a) Profiling at 100sec of Polishing time



(b) Cross sectional SEM pjhotograph

Fig. 6. Post-CMP planarization, (a) pProfiling at 100sec of polishing time, (b) cross sectional SEM photograph.

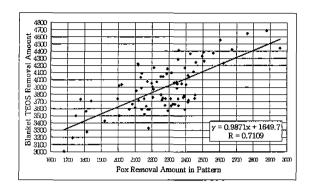


Fig. 7. Correlation analysis graph for polished oxide amount between blanket and STI pattern wafer.

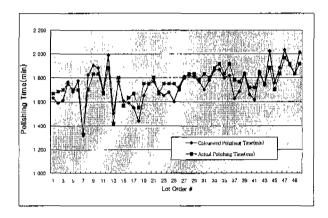


Fig. 8. Difference between caculated and actual polishing time.

Finally, we did the reproducibility test with total 50 lots. There is a little difference in between calculated polishing time and actual polishing time. Figure 8 shows the difference in between calculated polishing time and actual polishing time. The time difference is 3.48 seconds for 50 lots. If this time difference is converted into the thickness, then thickness is 104~176 Å. It is possible to be ignored because the process margin is about 1800 Å.

4. CONCLUSION

The removal properties for the blanket and STI pattern wafer were analyzed to control accurate post CMP thickness in the pattern wafer. As a result of this analysis, in manufacturing STI CMP process, we could use the removal rate of the blanket wafer which was changed by linear reduction as polishing time because of using the two data of the pre and post CMP thickness. In addition, the removal target oxide of the blanket wafer could be obtained by the linear fitting formular induced through the correlation

analysis between the blanket and pattern wafer. Finally, the polishing time could be calculated from removal rate and removal target thickness of the blanket wafer, and the difference is 3.48 second for time and 104~167 Å for thickness. It is possible to be ignored because the process margin is about 1800 Å.

REFERENCES

- [1] Ohmori and Toshio Kasai, "New Ultra-precision CMP Technique Applying Direct Air-Back Method and Non-foaming Plastic Pad", IEEE Trans., Electron Device, pp.225-228, 1999.
- [2] Sang-yong Kim, Nam-Hun Kim, Yong-Jin Seo, Chang-Il Kim, Woo-Sun Lee, Eui-Goo Chang, "A study on Relationship between Pattern wafer and pattern wafer for STI CMP", J of KIEEME, PA-2, pp. 211-213, 1999.
- [3] G. Popescu, M. Lauwidjaja, L. Denney, K, Richardson, and A. Dogariu, "Aging effect in CMP slurries probed by multiple light scattering", Electrochem. Soc. Proc., Vol. 98, pp.59-68, 1999.
- [4] Bih-Tiao Lin and S-N Lee, "An Effective End Point Detector on Oxide CMP by Motor Current", IEEE Trans., Electron Device, pp. 295-298, 1999.
- [5] Sang-yong Kim, Chang-Il Kim, Eui-Goo Chang ,Yong-Jin Seo, "A study on EPD of STI CMP Process with Reverse Moat Pattern" J of KIEEME,OA-4, pp. 14-17, 2000.
- [6] William J. Patrick, "Application of Chemical Mechnical Polishing to the Fabrication of VLSI Circuit Interconnections", Journal of Electrochem. Society, Vol. 138, pp.555-561, June 1991.
- [7] Sang-yong Kim, "Understanding of process parameter in Chemical Mechanical Polishing", J of KIEEME, Vol.12, No. 10, pp.9-18, 1999.
- [8] Tseng WT, Chin JH, Kang LC, "A comparative study on the roles of velocity in the material removal rate during chemical mechanical polishing", Journal of the Electro- chemical Society, Vol. 146, No. 5, pp. 1952-1959, 1999.