Top Level Software and Hardware Mapping Method of the SAR Processor

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ABSTRACT

It is essential design process to analyze processing load and set up top level software and hardware mapping using main parameters before implementation of the SAR processor. This paper identifies the requirements upon the software and hardware mapping to be assessed and suggests its practical method to the SAR processor. Also, simulation is performed to the E-SAR processor to examine the practicability of the method and the results are discussed. Thus, this method can be applied to the SAR processor.

Ⅰ. Introduction

Synthetic Aperture Radar(SAR) can provide all weather, high-resolution images of the earth over a wide area[1]. SAR data represent an important source of information for a large variety of scientists around the world[2]. A SAR image is a two-dimensional mapping of received signal energy. The intensity assigned to individual pixels is the computed energy in the signal received from the corresponding location within the illuminated scene. A separate computation is necessary for each of the many pixels that form an image[3].

The generation of SAR images from the raw radar data is computationally demanding, and depends on the radar platform and the chosen processing parameters[4]. The SAR processor is the primary image-generating component of the SAR system. Work during initial design stage set out the processing algorithm definitions and performance analysis of the SAR processor. These definitions and results constitute the starting point of this paper. It is principal design process to estimate processing load and set out top level software(SW) and hardware(HW) mapping before implementation of the SAR processor.

This paper has identified requirements upon the SW and HW mapping to be assessed. This assessment has led to a rationale which confirms the top level HW configuration, defines the SW and HW mapping method and which will be able to lead to a definition of the criteria against which a suitable HW system may be selected.

Also, it is assumed a spaceborne SAR processor for simulation and called Experimental-SAR(E-SAR) processor. In section Ⅱ, the echo processing flow through the E-SAR processor and parameter values based on SAR processor design criteria are presented.

Ⅱ. E-SAR Processor

Range- Doppler algorithms are built around the fundamental benefits of the Range- Doppler domain. SAR processors using them have evolved over the years, with newer versions including more terms in their approximations to the hyperbolic phase term in the azimuth modulation[5]. The Range-Doppler algorithm is selected for E-SAR processor processing. Fig. 1 illustrates the range and azimuth compression processing flow that is used for the HW and SW mapping analysis of the E-SAR processor.

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The parameters and requirements of the E-SAR processor used for simulation are shown at below Table 1.

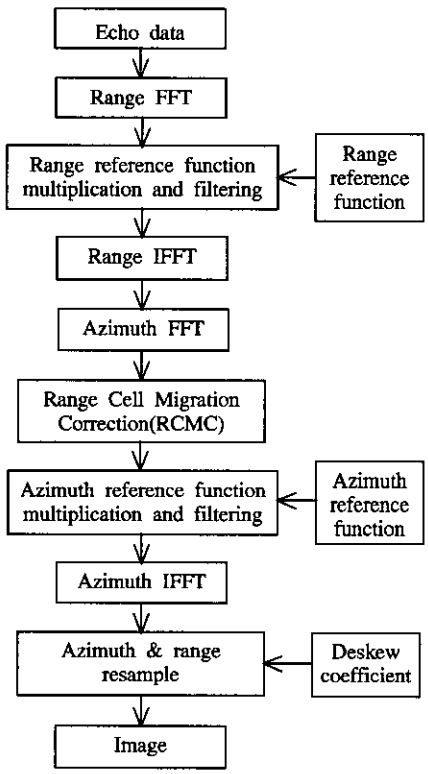

Fig. 1 The processing flow of the E-SAR processor.

Ⅲ. Top Level SW and HW Mapping Method & Simulation

The basic unit of space SAR image processing is a scene. This is an approximately square image product of 10^4 by 10^4 resolution cells. It is a fundamental property of a spaceborne SAR that its synthetic aperture constitutes a large proportion of the along track imaged scene.

The types of processing tasks involved in SAR processor processing reveal the top level SW and HW mapping concepts best suited to the situation. Top level tasks can be categorized as follows: tasks associated with scene-wide tasks associated with extracting and deriving data and processing parameters which apply to the entire scene, block-wide tasks associated with deriving the parameters for processing discrete data blocks independently of one another, sample-by-sample computationally intensive tasks involved in processing independent data blocks to generate the image output, Man Machine Interface(MMI) tasks, and Input & Output(I/O) tasks. In order to process an entire scene the scene-wide, block-wide, and sample-by-sample tasks must be implemented in sequence.

3.1 Scene-wide Tasks

These tasks are parameters evaluation and derivation types : product and radar mode determination such as scene extent definition, orbit determination, attitude determination, scene Doppler center frequency determination, Doppler surface evaluation, processing block definition, range reference function, and range radiometric correction parameters.

These scene-wide operations are carried out on small to moderate volumes of input data and generate low volume output. To be able to derive the scene-wide parameters so that the bulk data

Table 1. The parameters and requirements of the E-SAR processor

Contents	Values	Unit	Remark
Number of range & azimuth FFT point	8192(=2^{13})		N
Number of interpolation point	10		
Pulse Repetition Frequency(PRF)	2500	Hz	
A CPU processing rate	3×10^8	FLOP/sec	Floating point operations
The margin of processing load	25	%	
The implementation efficiency of CPU	33	%	
The margin of over sampling	20	%	
The size of a scene	$10^4\times10^4$		The number of resolution cells
Scene processing rate	1/10th real time processing		

processing can proceed in the sequence dictated by the sequence of input echo data implies a requirement for sample data to be extracted from the scene data ahead of scene-wide, block and sample-by-sample tasks. The tasks necessary to the concept of data assembly are to extract and record : radar auxiliary data, replica data, and along track sample blocks. Tasks that it is convenient also to include are echo sequence checks, Block Adaptive Quantizer(BAQ) sample de-commutation, and echo data extraction.

3.2 Block-wide Tasks

Variations in the focus parameters over the extent of the scene mean that we cannot process the entire data set using only one set of parameter values. The consequence is that compression operations have to be carried out on blocks of echo data much smaller than the entire scene. Block-wide tasks take the block definitions, the product definition and formatted geometric parameters from the scene-wide processing and derive from them sets of block processing parameters.

Block-wide processing tasks operate on low volume data input and generate low volume data output. Block-wide tasks evaluate : azimuth reference functions or their parameters, look definitions, RCMC parameters, range re-sample parameters, azimuth radiometric correction parameters, de-skew parameters, spectral correction parameters, phase correction parameters, and pixel location output pointers. Thus, each processing block has associated with it a set of processing parameters enabling the block echo data to be processed at sample-by-sample level independently of every other block.

3.3 Sample-by-sample Tasks

These tasks operate upon echo data samples organized within processing blocks. They are the computationally intensive tasks that generate the scene image output. The volume of input data is high ; the volume of output data is at least comparable with the input volume ; operations are significantly computationally intensive. The impact of the top level throughput requirement and data volumes upon the sample-by-sample processing SW and HW mapping is significant.

In order to assess the design requirement we need estimates of : the expected number of FLOP per scene sample, the required scene processing rate, the capability of current CPU's, the expected data I/O rates, and the capability of current disc controllers and buses.

3.3.1 Estimated processing load per scene sample

This estimate assumes : a Single Look Detected(SLD) output image, and only the heaviest loading tasks need to be considered[6]. The result to the E-SAR processor is illustrated in Table 2.

Table 2. The estimated FLOP per sample

Step	Basis of FLOP estimate	FLOP per sample
Range FFT	$5 \log_2 N$	65
Range IFFT	$5 \log_2 N$	65
Azimuth FFT	$5 \log_2 N$	65
RCMC/re-sample	2 × interpolation length × 2	40
Azimuth IFFT	$5 \log_2 N$	65
Azimuth resample	2 × interpolation length × 2 × 2	80
Range resample	2 × interpolation length × 2 × 2	80
Total		460

The minimum number of FLOP per sample is expected to be 460 not allowing for : less intensive computations, address computation, data transfer operations, and data overlap processing. It is safe to allow an overhead of approximately 25% for these operations giving an estimated 600 FLOP per sample.

3.3.2 Required scene processing rate and capability of CPU's

We require 1/10th real-time processing rate (7 minutes of data processed in approximately 70 minutes). At a PRF of 2,500Hz the data for a scene is gathered in about 4seconds. This corresponds to a scene processing time of about 40seconds. We assumed that a power PC CPU is capable of 3×10^8 FLOP/sec. Requirement tells us

that we can expect to achieve an implementation efficiency of approximately 33%.

3.3.3 The requirement for multiple CPU's

From the estimates set out in the previous section : One scene requires a total of : $600\times10^4\times10^4=6\times10^{10}$ FLOP. Allowing for 20% over sampling in range and azimuth this becomes : 9×10^{10} FLOP.

We require 1/10th real time processing rate corresponding to a scene processing time of about 40seconds. Therefore we require an effective processing rate of : $(9\times10^{10})/40=2.3\times10^9$ FLOP/sec. Currently a power PC CPU is capable of 3×10^8 FLOP, which at an efficiency of 33% implies we require : $(2.3\times10^9)/(0.33\times3\times10^8)$ CPU's to achieve the processing rate requirement. i.e. The sample-by-sample operations of the E-SAR processor require the resources of 23CPU's processing simultaneously.

3.3.4 I/O data rates

One scene consists of $10^8\times4\times2$bytes. This is a worst case(largest) figure for the SLD product. Mean data input rate, at 1/10th real time rate, is of the order of 2.5Mbytes/sec. In 40seconds the processor mean output rate $\cong (8\times10^8)/40 \cong$ 20 Mbytes/sec.

Using current technology one disk controller can deliver a peak read/write rate of 20 Mbytes/sec sequential access(pseudo random access rates are lower). Therefore one disk controller each for I/O may be sufficient for the E-SAR processor system. The aggregate I/O data rate of 200Mbits/sec must be handled by a Local Area Network (LAN). This can be achieved with current technology using a 1Gbit/sec Ethernet. A SUN workstation, for example, will support total disc I/O rate of 100Mbytes/sec, so the aggregate mean I/O rate of 23Mbytes/sec is feasible with plenty of margin.

Ⅳ. The Result and Discussion

4.1 Top level SW Mapping

Scene-wide and block-wide tasks are executed in sequence and depend upon the data assembly tasks having been executed first. Whether or not the block-wide tasks are grouped together with the scene-wide tasks or are placed in the main sample-by-sample processing is a question of the balance between the volume of block-wide data output and processing speed. Optimal balance and operational speed can be achieved by grouping the block-wide tasks with the scene-wide with block data parameter transfer by RAM. Doing this enables us to identify the top level SW mapping to the E-SAR processor as Fig. 2.

Fig. 2 shows that the SAR processor can be conveniently subdivided into three functional segments. The Data Assembly Processor(DAP) takes as its input a stream of echo data records from the synchronized data. It checks the state of completion of the data in terms of its status as a sequence of radar echoes and extracts and records the echo, replica, and sample & auxiliary radar data. The completed echo data is passed to the Main Processor(MP) and the auxiliary data passed to the Support Processor(SP) where the processing parameters for the MP are derived. The SP performs those calculations that need to look at information on a scene-wide basis. The results are broken down into data sets applicable to independent data blocks. Each data block can then be processed without reference to the processing of any other block.

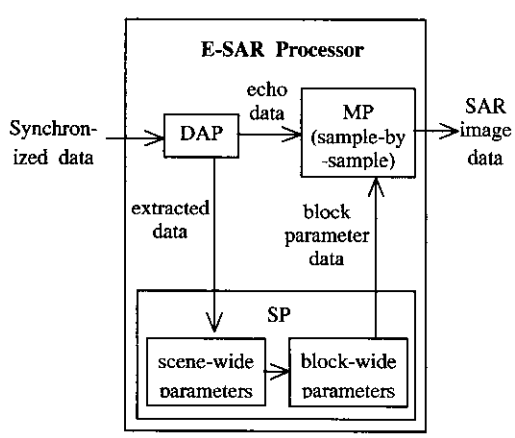

Fig. 2 Top level SW mapping of the E-SAR processor

This allows the MP, which handles most of the processing load, to be efficiently implemented on a parallel array processor. The SP is organized (by algorithm type and by SW unit) into two stages. One derives scene-wide processing parameters from the data extracted by the DAP; the other derives the block-wide processing parameters required by the MP enabling it to generate and organize the image data according to the image quality requirements.

4.2 Top level HW Mapping

The requirement for a multi-CPU MP has been identified. Best efficiency is always achieved when each CPU is working independently on a partitioned data blocks. A general purpose multi-CPU workstation, for example a SUN workstation, does not give a computational rate increase in linear proportion to the number of CPUs added primarily because of its methods of memory access and co-ordination. In addition multi-CPU workstations do not support the number of CPUs required by the E-SAR processor. A different HW and SW architecture is required for the MP. An array processor is a more efficient system for executing many similar tasks in parallel using partitioned data blocks.

However, an array processor requires a host computer system to isolate it from the LAN and to co-ordinate its activities. Operationally we can take advantage of this situation since the DAP and SP tasks can in principle be executed on the host workstation. Once the host has initiated the array processor activities it can be used to process the parameters for the next scene and to handle the MMI activities of the current process. This facilitates operational pipelining. Then, the proper top level HW mapping to the E-SAR is shown in Fig. 3.

Data common to all processors, for example radar auxiliary data, universal constants, can be declared as read only so that each CPU takes a copy to its own local memory partition. I/O should be supported by non-blocking methods. 1 disc controller is required for input and at least 1

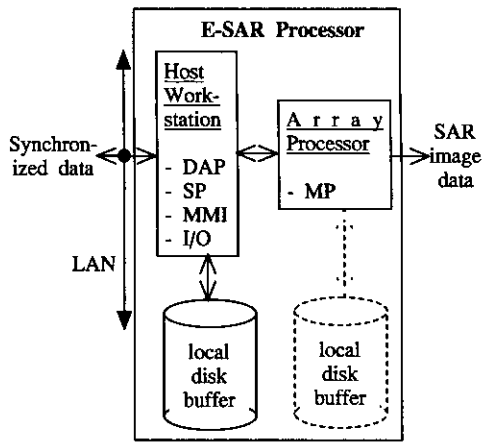

Fig. 3 Top level HW mapping of the E-SAR processor

controller for output, served either by the array processor or host. Having first defined the MP throughput capability the host workstation resources can be defined so that neither of them constitutes a data flow bottleneck.

V. Conclusion

The generation of SAR imagery involves an extensive amount of computation and data manipulation. Most of the data handling in a SAR processor can be thought of as correlation of the received signal with a two-dimensional reference function. Thus, it is very critical to apply the top level SW and HW mapping method for the SAR processor during design stage before implementation.

This paper identifies requirements upon the SW and HW mapping to be assessed. It describes work on the derivation of top level SW and HW mapping method and sets out configuration of the SAR processor. Also, simulation has been performed to prove the practicability of the method. It suggests proper top level SW and HW configuration of the E-SAR processor. It is shown that HW can be selected from currently available equipment that meets all the E-SAR requirements. In summary this constitutes : multiple CPU(2) SUN workstation host with multiple disc controllers, 1Gbit/sec Ethernet LAN, and 23CPU parallel processing array. No special HW is

required and SW can be developed without dependence upon final HW selection, since no HW dependent protocols are required.

Therefore, our approach can provide a practical method for applying the top level SW and HW mapping to the SAR processor.

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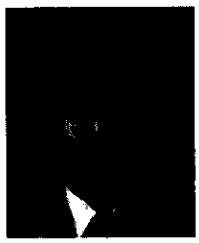

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