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Quasi-Continuous Operation of 1.55-μm Vertical-Cavity Surface-Emitting Lasers by Wafer Fusion

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Room temperature quasi-continuous operation is achieved near 1556 nm with threshold current as low as 2.2 mA from a 5.6-μm oxide-aperture vertical-cavity surface-emitting laser. Wafer fusion techniques are employed to combine the GaAs/AlGaAs mirror and the InP-based InGaAs/InGaAsP active layer. In this structure, an Al_xO_y/GaAs distributed bragg reflector and intra-cavity contacts are used to reduce free carrier absorption.

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I. INTRODUCTION

Vertical-cavity surface-emitting lasers (VCSELs) at long-wavelength range (1.3 μm - 1.55 μm) are of great interest for future high-capacity fiber-optical communication systems. Their vertical geometry and small dimensions are advantageous for on-chip-testing, effective fiber coupling, packaging and potential low-cost fabrication [1]- [3]. However, in contrast to GaAs based VCSELs operating at wavelength <1 μm, the progress of long-wavelength devices has been much slower. This is mainly due to intrinsic problems in the InGaAsP material system [4]. One of them is the small refractive index difference between InP and InGaAsP that leads to unforgivingly thick VCSEL structure. The fundamental constraint limiting the design of long-wavelength VCSELs has been the lattice matching within a structure. Non-lattice matched growth results in defect formation, thereby degrades crystal quality. To overcome this barrier, techniques of wafer fusion have been used to by-pass the condition of lattice matching [5]- [7]. Using wafer fusion techniques, one can combine two materials of different lattice constants without degrading the crystal quality away from the interface. In the present work, we employ wafer fusion techniques to combine InP-based InGaAs/InGaAsP active layers with GaAs-based bottom and top DBRs to make long-wavelength VCSELs [8]- [11].

II. WAFER FUSION AND ITS CHARACTERISTICS

Wafer fusion is a process in which two wafers are combined to form a device without the use of any intermediate layer [5]- [7]. Two epitaxial surfaces are cleaned/passivated such that there are minimal contaminants on the surface. Then the two epitaxial surfaces are placed together in intimate contact under pressure. With the wafers in contact, one heats up the wafers near the growth temperature of one of the materials. This allows atomic redistribution near the surface. Additionally channels are etched into one of the wafers to remove gases generated at the fused interface and to produce a bubble-free interface.

1. Surface roughness and cleaning

Before the wafer fusion process, we examine the surface roughness of InP and GaAs substrates to be fused by an atomic force microscope (AFM). After wet etching and/or photoresist (PR) process, a clear increase in surface roughness is observed as shown in Table 1. Usually the wet etching process produces spatially non-uniform surfaces. The surface roughness generated during the etching and PR processes plays an important role in uniform wafer bonding. We also investigate residual ingredients on surfaces cleaned by

TABLE 1. Surface roughness of several epitaxial layers examined by an atomic force microscope (AFM). The scanned area is 250 μm^2.

Samples	Treatment	Root-mean-square roughness
P-type mirror (GaAs/AlAs)	As grown	~ 0.15 nm
Active layers (GaInAs/InGaAsP)	As grown	~ 0.14 nm
Active layers	(InP cap layer/GaInAs etch-stop layer) are removed by wet etching.	0.57 ~ 0.1 nm (Average) ~ 0.3 nm
Active layers	The wafer is coated with photoresist and cleaned by acetone.	~0.56 nm

different processes (Table 2). The atomic elements of the wafer within 2~3 nm depth from the surface are examined by an Auger electron microscope (AEM).

The fusion process could also be influenced by impurities at the interface. Different preparation procedures result in different impurities of varying amounts. We focused on oxygen (O) and carbon (C) atoms that are related to contamination at the surface. The total fraction of O and C atoms on the surface is always about 30% regardless of the chemical treatment. The process that produces minimal oxide atoms at the fusion interface and maintains good surface roughness is preferred. Therefore, the solvent cleaning (SC) - buffered oxide etchant (BOE) - deionized water (DI water) cleaning process is chosen and followed by etching in BOE and in NH_4OH solution. DI water is used to rinse the samples. Base on this results, we treat all wafers in this way for wafer fusion.

2. Electrical properties

Previously good conduction through an n-InP/n-GaAs interface has been reported [12]. However, it is nontrivial to get low-resistance through an p-InP/p-GaAs interface [13]. To understand electrical properties at the p-InP(100)/p-GaAs(100)

TABLE 2. Residual surface elements on GaAs surface after cleaning investigated by the Auger electron microscope (AES). OPE: oxygen plasma etching, BOE: buffered oxide etchant, DI water: deionized water, SC: solvent cleaning.

Samples	C (%)	O (%)	Ga (%)	As (%)
Reference GaAs	15.6	16.1	30.9	37.5
SC-BOE-DI water	12	12.3	34	41.5
SC-BOE-DI water -NH_4OH-DI water	26	9.4	28.2	36.6
OPE-BOE-DI water -NH_4OH-DI water	15.6	13	33.4	37.9
Ar milling	12.7	23.2	33.6	29.5
Ar milling-BOE-DI water	26.4	4.6	25.8	43.2

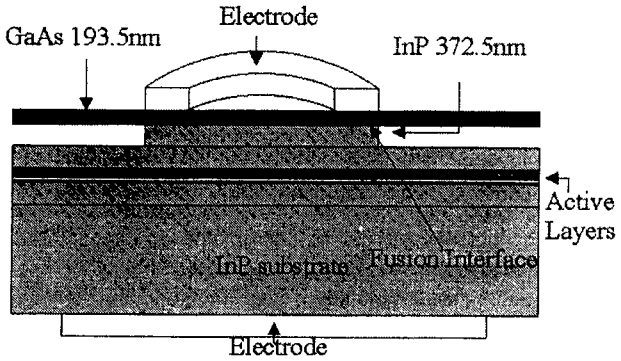


FIG. 1. Schematic cross section of an active layer fused with a thin GaAs layer forming a p-p fused junction. Turn-on voltage and electro-luminescence of this device are measured.

fused interface of real devices structure, a wafer having a p-doped GaAs/AlAs mirror is fused with an other wafer having quantum wells. Then all the layers above the p-mirror except a 193.5-nm GaAs layer next to the fused interface with 4×10^{18} cm^{-3} of carrier concentration (Zn doped) are etched by ion milling. And p-type electrodes (AuZn) are deposited on the GaAs layer. The other electrode is made on the n-type InP substrate. (Fig. 1) The InP layer near the fused interface is doped with Zn of 1×10^{18} cm^{-3}. In the I-V characteristic curve, we observe turn-on of current. The turn-on voltage decreases with fusion temperature. The voltage-drop at the interface ranges from 0.12-0.92 V depending on fusion temperature. (Ta

TABLE 3. Turn-on voltage of the thin GaAs layer fused with the active medium. These values include the voltage drop at the active layer of 0.68 V.

Fusion temperature (°C) →	700	650	550
Turn-on voltage (Active layers + P-type mirror)	0.8~1.34 V	0.88~1 V	1.1~1.6 V

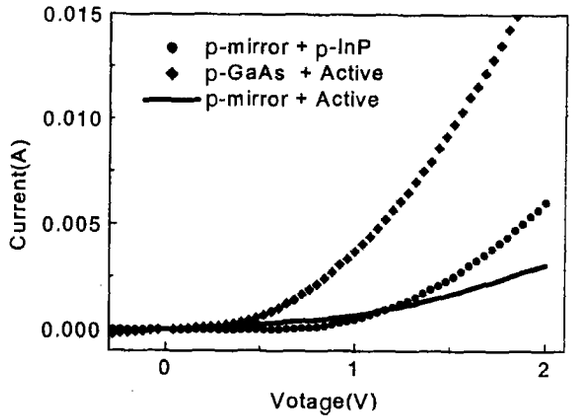


FIG. 2. Turn-on voltage of several wafer combinations fused at 650°C.

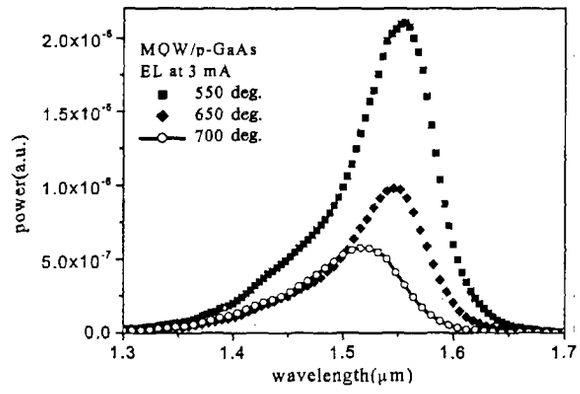


FIG. 4. Electro-luminescence after fusion at different temperatures. The reference electro-luminescence is obtained from as-grown GaInAs quantum wells.

-ble 3) As fusion temperature becomes high, the voltage-drop at the fused interface tends to decrease. To find out which side is responsible for the voltage-drop at the fused interface, additional fusion is done as shown in Fig. 2. Because the bare wafer is flat and the root-mean-square (RMS) roughness of all samples is less than 0.15nm, the voltage-drop at the interface is attributed to the rigid GaAs-based P-type mirror which a has slightly curved surface formed during the growth process. (Fig. 3.) We think the curvature promotes uneven pressure applied to the samples resulting in non-uniform bonding together with the above-mentioned surface roughness.

3. Luminescence of fused active layers

Because the high pressure and temperature of wafer fusion can affect luminescence of quantum well structure, electro-luminescence (EL) of a fused strain-compensated GaInAs/InGaAsP multiple quantum well (MQW) structure is investigated. The wafer structure is as shown Fig.1. and the distance of the MQW from fused interface is 177 nm. In this experiment, fusion temperature is varied but applied pressure is fixed.

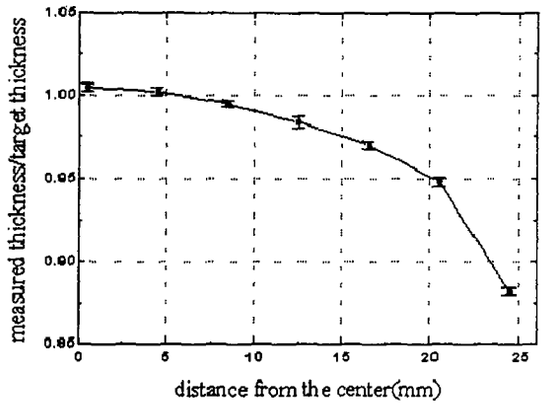


FIG. 3. Measured thickness variation of the p-mirror across a wafer.

Fig.4 shows the EL spectra from the fused wafers. In the case of 700 °C, full width at half maximum (FWHM) is larger than the other cases indicating that the quality of the fused active layers is degraded. The peak intensity of the wafer fused at 550 °C is largest among these samples and decreases for the sample fused at high temperature. Assuming that the degradation of EL comes from interfacial defects penetrated into the active layer, low temperature annealing is advantageous in limiting the diffusion of both dopants and defects into materials [5,6]. On the other hand, the fusion temperature at 550 °C results in higher electrical resistance compared to the 700 °C fusion. In fact, the real VCSELs structure is fused at 600 °C to have good optical and electrical properties.

III. FABRICATION PROCEDURE

To reduce free carrier absorption which is sensitive to hole concentration at long-wavelength, we employed Al_xO_y/GaAs DBR as a top mirror and as intra-cavity contacts (Fig. 5) [8,11,14]. The short effective thickness of the Al_xO_y/GaAs DBR also helps in the reduction of the free carrier absorption. We expect that our device employing the Al_xO_y/GaAs DBR and AlAs/GaAs bottom DBR shows good thermal conductivity.

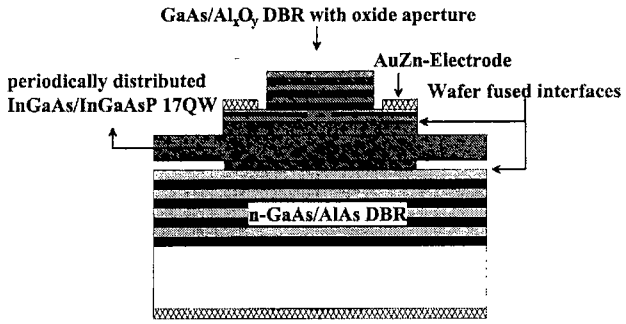


FIG. 5. Schematic cross section of the fabricated long-wavelength VCSEL.

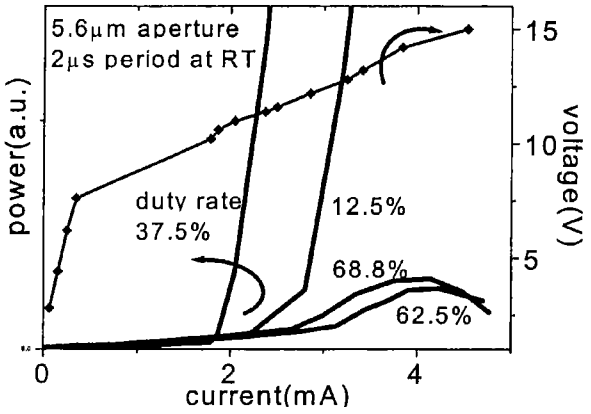
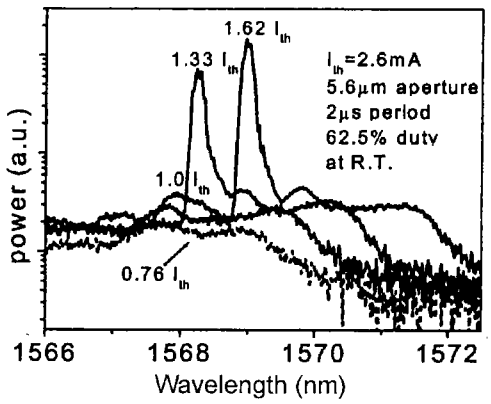


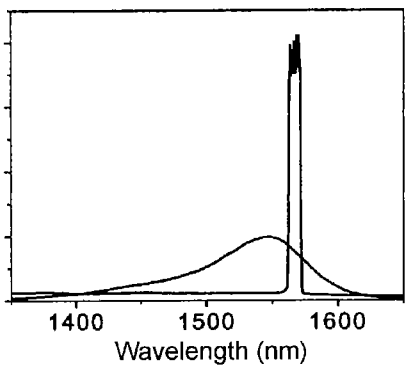
FIG. 6. Output characteristics under pulsed operation at room temperature.

Our device consists of an AlAs/GaAs bottom DBR, a 2 1/2λ thick spacer and an Al_xO_y/GaAs top mirror grown by metal organic chemical vapour deposition (MOCVD). The active medium consists of compressively-strained (0.7%) 3.8-nm-thick $In_{0.6}Ga_{0.4}As$ quantum wells. Total of 17 InGaAs quantum wells are distributed periodically at field intensity maxima [15] and 10-nm-thick lattice-matched InGaAsP layers whose bandgap wavelength is 1.24 μm are used as barriers. The bottom n-mirror consists of 33 GaAs/AlAs pairs on a GaAs substrate. For the top mirror, 7 pairs of undoped GaAs/AlAs and p-GaAs/p-$Al_{0.75}Ga_{0.25}As$/p-GaAs layers are grown on GaAs. To locate the Al_xO_y aperture, a 70-nm AlAs layer is inserted in the middle of the p-AlGaAs layer at the bottom of the top mirror. The active medium on InP is bonded to the mirror layers on GaAs under hydrogen atmosphere at 600 °C for 30 minutes and is gradually cooled to room temperature for 1.5 hours. During the fusion process the applied pressure is kept uniform through the surface using a specially designed graphite sample holder that is fastened with a bolt. We use a torque wrench to estimate the pressure applied to samples and it is about 4kg·f·cm that is equal to about 12 Mpa. The trench is etched into the active medium for uniform wafer fusion. To make top mirror mesas that require precise etching depth control, the chemically assisted ion beam etching (CAIBE) is used. After p-electrodes are made and isolated by mesa etching, the devices are oxidized in a wet oxidation system to form Al_xO_y/GaAs top mirrors and oxide apertures simultaneously.

The oxidation system is composed of a mass flow controller, a water vapor source and a furnace. Nitrogen gas is bubbled through a heated bath of water with a rate of 0.8 l/min and it is injected into the furnace at a temperature of 425 °C where samples are



(a)



(b)

FIG. 7. (a) Optical spectra of the VCSEL of 5.6-μm oxide aperture. (b) A PL spectra of the active layer and the position of the cavity resonance.

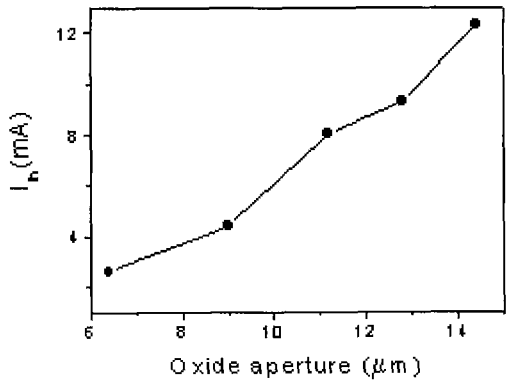


FIG. 8. Threshold current as a function of the oxide aperture at room temperature.

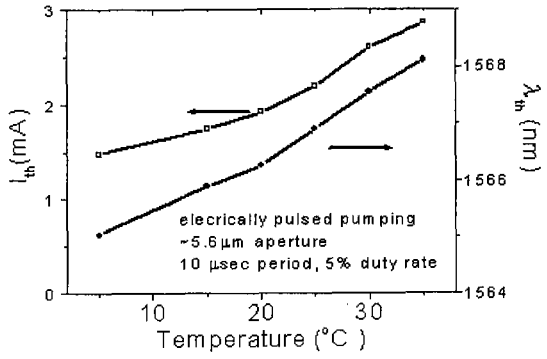


FIG. 9. Temperature dependence of the threshold current and lasing wavelength at threshold.

oxidized. We can directly see the oxidation in an optical microscope or CCD camera and therefore measure the oxidation depth. The measured oxidation depth versus oxidation time gives a linear relationship. Therefore we can control the oxidation depth by the time.

IV. RESULTS AND DISCUSSION

The light output versus injected current (L-I) characteristics for the double fused long-wavelength VCSEL are shown in Fig. 6. Lasing is achieved near 1556 nm and the device operates at room temperature using 2-μs period pulses. The devices with 5.6-μm oxide aperture operate until the maximum duty rate of 68.8% (1.3 μs). The injected current versus applied voltage (I-V) curve shows a high turn-on voltage of 7 V from which the voltage drop at the fused junction is estimated to be 4.2~2.8 V. This high turn-on voltage seems to result from non-uniform bonding of the curved p-mirror and the low doping level at the fused junction [8]. The lasing spectra for the device operating with 62.5% duty cycle are shown Fig.7, measured with an optical spectrum analyzer with minimum resolution of 0.24 nm. Due to Joule heating, the lasing wavelength moves toward longer wavelength. The threshold current increases almost linearly with the diameter of oxide aperture as shown in Fig. 8. The minimum threshold current is 2.2 mA for a 5.6-μm oxide aperture device. It corresponds to J_{th} of 7 kA/cm^2 if uniform current injection is assumed. Temperature dependence of threshold current is also studied using a thermo-electric cooler. (Fig. 9) The Fabry-Perot resonance peak is located at longer wavelength than the gain peak at room temperature. (Fig.7.b) This cavity peak red-shifts at a rate of 0.1 nm/K while the gain peak of the InP-based active layer is known to shift at a rate of 0.54 nm/K [16]. The increase of the threshold current with temperature can be explained by the substantial decrease of the peak gain due to the spreading of the Fermi distribution of carriers.

Although only one longitudinal mode falls within the bandwidth of the DBR, many transverse modes are still allowed. The output spectra from the VCSELs with different oxide apertures (50-ns pulse width, 200-ns period at room temperature) are shown in Fig. 10. The fundamental transverse mode, LP_{01} mode where LP stands for "linear polarized" is linearly polarized along the corner of the square oxide aperture. The higher-order transverse mode LP_{11} splits into two orthogonal polarizations. The VCSEL of 3.3-μm oxide aperture shows fundamental mode operation up to 3.3 mA ($2.7I_{th}$). As we increase the current, the higher mode begins to show up together with the fundamental mode. For the 8-μm oxide aperture device, single mode emission with a side-mode suppression ratio (SMSR) of more than 25 dB is observed up to a driving current of 6.2 mA. (Fig. 11) And the maximum SMSR is measured to be 29 dB. This value is 4 dB higher than that of the VCSEL of 3.3-μm oxide aperture. This improvement of fundamental mode power is attributed to the reduced scattering loss that decreases as mode size and aperture size become similar [17]. On the other hand, for the VCSELs with over 10-μm oxide aperture, multimode lasing is generated from the threshold.

To achieve continuously operating long-wavelength VCSELs at room temperature, the voltage-drop at the p-p fusion interface should be reduced. The high voltage drop could be ascribed to the nonideal bonding of the curved GaAs surface and the relatively low doped layer at the interface [8]. Therefore, a more flat and smooth surface with higher doping profile

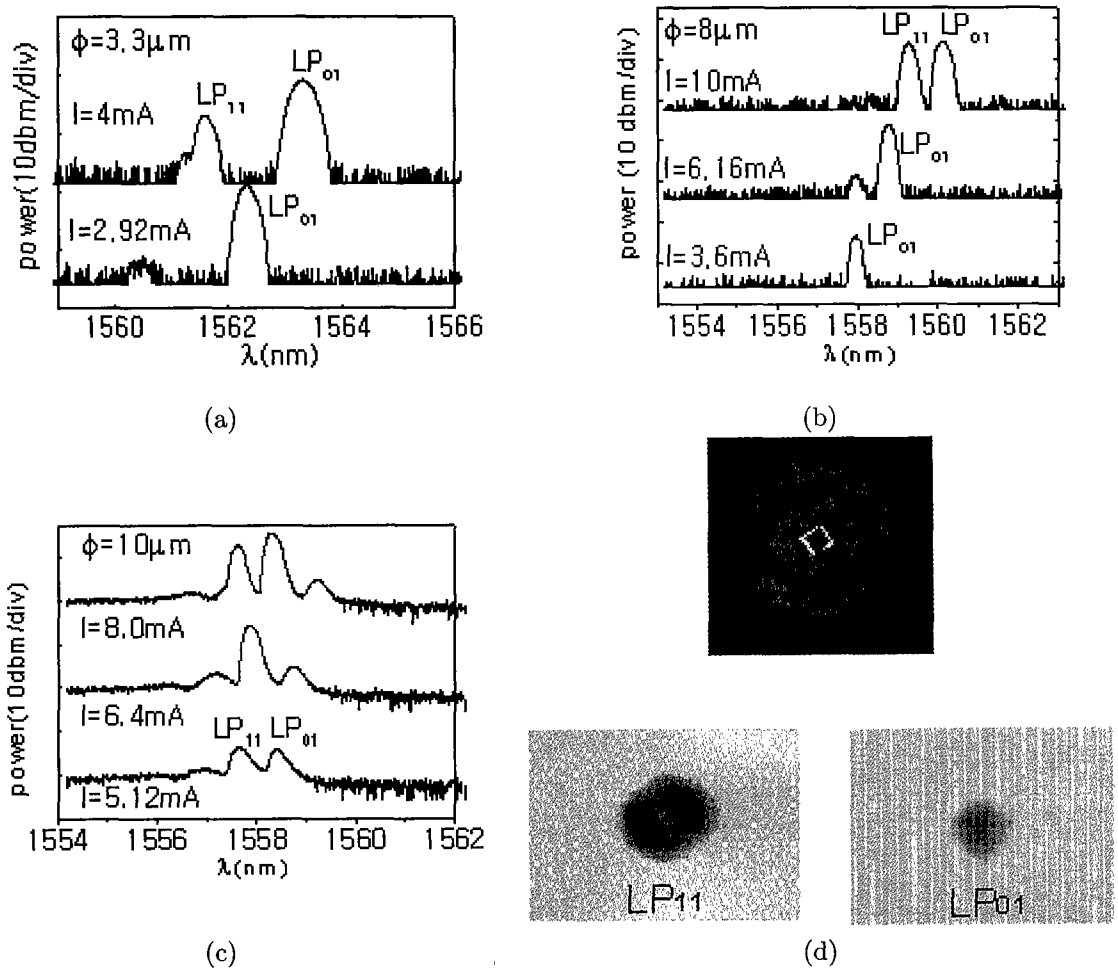


FIG. 10. Lasing spectra of the VCSELs of (a) 3.3-μm, (b) 8-μm, (c) 10-μm oxide aperture. Threshold currents are 1.2 mA, 3.7 mA and 5.1 mA respectively. The white square is a visual aid to indicate the square-shaped oxide aperture in (d). Near-field profile of LP_{01} and LP_{11} modes are taken by a CCD camera.

would certainly be helpful for continuous laser operation. In the present devices the contact resistance of the p-electrode still has room for improvement.

V. SUMMARY

Room temperature quasi-continuous operation from long-wavelength VCSELs using wafer fusion techniques is achieved. The threshold current is as low as 2.2 mA for 5.6-μm oxide-aperture lasers. It is found that the surface roughness, cleanness, and flatness play critical roles in wafer fusion. The VCSELs with oxide aperture below 10 μm show single mode operation. From the 8-μm oxide aperture device, single mode emission with a SMSR of more than 25 dB is observed up to 6.2 mA.

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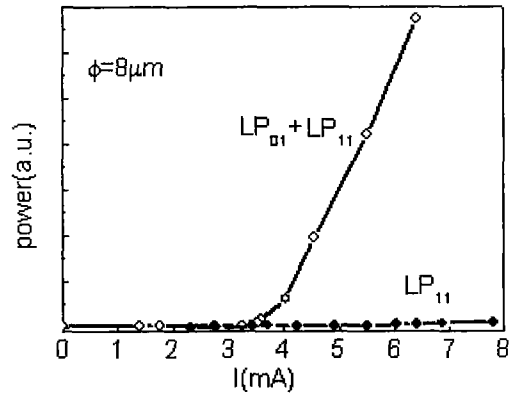

FIG. 11. Output characteristics of an 8-μm oxide VCSEL.

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