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Phosphorus doping in silicon thin films using a two-zone diffusion method

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Abstract – Single crystal and polycrystalline Si thin films were doped with phosphorus by a 2-zone diffusion method to develop the low-resistivity polycrystalline Si electrode for a hemispherical grain. Solid phosphorus source was used in order to achieve uniformly and highly doped surface region of polycrystalline Si films having rough surface morphology. In case of 2-zone diffusion method, it is proved that the heavy doping near the surface area can be achieved even at a relatively low temperature. SIMS analysis revealed that phosphorus doping concentration in case of using solid P as a doping source was about 50 times as that of phosphine source at 750°C. Also, ASR analysis revealed that the carrier concentration was about 50 times as that of phosphine. In order to evaluate the electrical characteristics of doped polycrystalline Si films for semiconductor devices, MOS capacitors were fabricated to measure capacitance of polycrystalline Si films. In ±2 V measuring condition, Si films, doped with solid source, have 8% higher C_{min} than that of unadditional doped Si films and 3% higher C_{min} than that of Si films doped with PH_3 source. The leakage current of these films was a few fA/μm^2. As a result, a 2-zone diffusion method is suggested as an effective method to achieve highly doped polycrystalline Si films even at low temperature.

I. Introduction

As semiconductor device is scaled down, the precise doping control is essential for proper device operation. In current VLSI device, the ion implantation is mainly used for doping the single crystal Si. However, both In-situ PH_3 and $POCL_3$ doping are widely used for doping the polycrystalline Si except dual gate electrode (N+ and P+) doping by implantation using dopants such as P and BF_2 for logic device transistor formation.

HSG (Hemi-Spherical Grain) is being formed on the storage electrode of DRAM capacitor by going through high vacuum annealing (1E-8 torr or below) in order to increase the capacitor surface area [1-3]. But the migrated HSG grain size is being affected by the doping concentration of the storage electrode. As the storage node is doped more heavily, HSG grain size tends to get diminished. To resolve this problem, the doping concentration of storage node before HSG formation needs to be maintained at a low level. However, to compensate the surface doping concentration for gaining maxiumum C_{min}/C_{max} ratio, the subsequent heavy doping process using such as PH_3 in-situ anneal should be performed. The implantation can not dope uniformly the rugged surface of polycrystalline Si. Also, since the $POCL_3$ doping method requires additional native oxide removal step, the surface area of each HSG grain becomes decreased which, in turn, results in a reduced DRAM cell capacitance. The dipping into HF oxide etchant also results in heavy dopant loss because dopants get sucked out into HF etchant. In this research, the 2-zone diffusion method is being used to study the doping characteristics (P-doping) in both single and polycrystalline Si. The differece between solid P doping and phosphine doping has been examined.

II. Experiments

The system which has been prepared for 2-zone controlled diffusion test can be operated in three different stages. The first is vaporizing stage where P vapor is formed by solid P. At second stage, the P will be out-diffused to P doping zone. In the final stage, the wafer will be maintained at room temperature while both vaporizing and doping region reach the

desired temperature. The scrubber has been installed into this system to exhaust the P vapor gas safely. During this experiment, the inner region of quartz tube has been maintained at a vacuum level in order to dope the wafer by vaporizing solid P. Based upon the basic test result, the each recipe condition has been set as follows. 1) Evaporation temperature : 400°C, 2) Stabilization Time : 10 min, 3) System inner pressure : 0.01 atm

Red P has been selected as a source material for solid P since this material is less poisonous and reactive. The stability and reactivity of red P lie between white P and black P. The vapor pressure of red P is far less than white P. It is also known that red P is not poisonous [4]. The p-type 4-inch single crystal Si wafer is used as a sample and is dipped into 7 : 1 BHF etchant in order to remove the native oxide before carrying out the experiment. The pre-cleaning method before experiment is the same. The distribution of P-dopant diffusion and its carrier concentration were observed by SIMS and ASR, respectively. The device characteristics have been analyzed by C-V and I-V measurements.

III. Results and Discussion

3.1. The doping characteristics of phosphorus introduced by 2-zone diffusion method

When P dopant is diffused into single crystal Si, the impurity atoms show abnormal distribution which is quite different from Gaussian or complementary error-function [5, 6]. The P distribution has three distinctive regions such as 1) heavily doped region, 2) transition (kink) region, and 3) low doping (tail) region. These regions can not be described by simple equation. Also, it was observed that P diffusivity in tail region of P distribution profile was increased by thousand times at 800°C. There are numerous and representative P diffusion models for single crystal Si such as Schwettmann-Kendall-Carpio (SKC), Yoshida (Y), Fair-Tsai (FT), and S. M. Hu *et al.* models [7-10].

The single crystal Si was used to examine the P-doping characteristics. The doping time split 60/90/120 min within 800~900°C range has been performed to evaluate the dependency of time on diffusion characteristics. Fig. 1 shows the normalized maxium doping concentration level at a given temperature and time where doping time has been set by 60 min

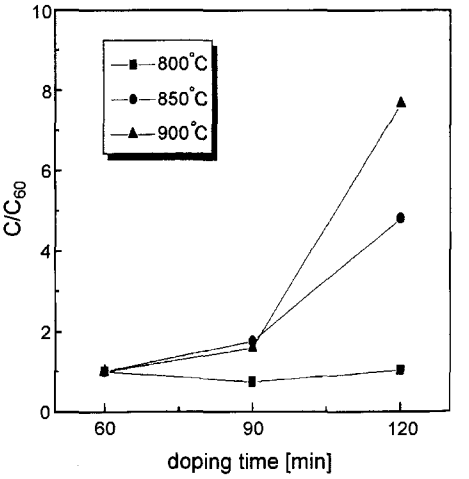

Fig. 1. Normalized maximum concentration as a function of doping time with various doping temperature.

basis. At 850°C and 900°C, there has been a clear trend of increase in doping level with respect to time. But, at 800°C, no such a trend has been detected up to 120 min. In this picture, it can be seen that the doping concentration level at a given time interval is increased as temperature rises. To see the diffusion trend depending upon process temperature, the single crystal Si was doped for 60 min within 750~850°C range. It has been observed that the junction depth was increased as temperature rises. However, the heavily doped region close to the surface area was not much affected by temperature rise. In general DRAM process, the low temperature below 800°C is required because the capacitor process comes after the source/drain formation. In case of 2-zone diffusion method, it is proved that the heavy doping near the surface area can be achieved even at a relatively low temperature.

3.2. The comparison of doping characteristics between PH_3 and red-P as a doping source

The differece between solid P-doping and phosphine doping has been examined. To see the diffusion trend depending upon process temperature, the single crystal Si was doped with solid P and phosphine, respectively, for 60 min within 700~800°C range. The phosphorus depth profile and the depth profiles of the carrier concentration were measured by SIMS and ASR, respectively. The process time was set to 60 min. In case of phosphine doping, the condition of 180 min

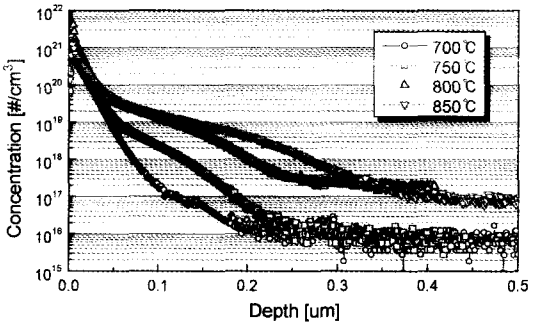

Fig. 2. SIMS doping profile of phosphorus at the different doping temperatures during 60 min in single-crystal Si.

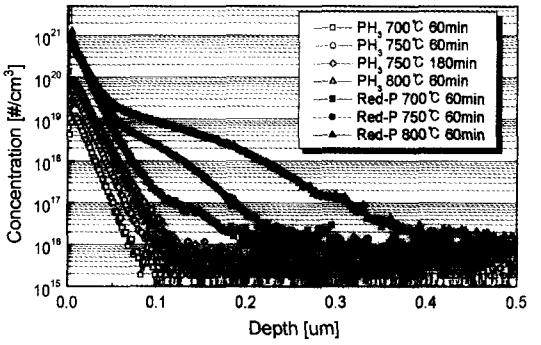

Fig. 3. SIMS phosphorus concentration with respect to the different doping sources in single-crystal Si thin films.

doping was added. To activate the doped phosphorus, all samples were annealed at 850°C for 1 min. The results of measuring the doping concentration by SIMS and ASR are shown in Fig. 3 and Fig. 4, respectively. In Fig. 3, for phosphine source, a surface concentration of 1.0E19~7.0E19 #/cm^3 range was obtained. For solid P source, on the other hand, it was about 50 times as that of phosphine source with 9.0E20~1.5E21 #/cm^3 range. In case of phosphine, the condition of 180 min doping at 750°C was similar to that of 60 min doping at 800°C. For solid P source, the heavily doped region close to the surface area was not much affected by temperature rise. For phosphine source, however, there has been a clear trend of increase in doping level with respect to the process temperature. These results show that the phosphorus formed by solid P was doped with saturation value below 800°C, but the phosphorus formed by phosphine was not. For both solid P and phosphine source, the concentration of bulk increased with respect to the process temperature. And the faster diffusion rate of

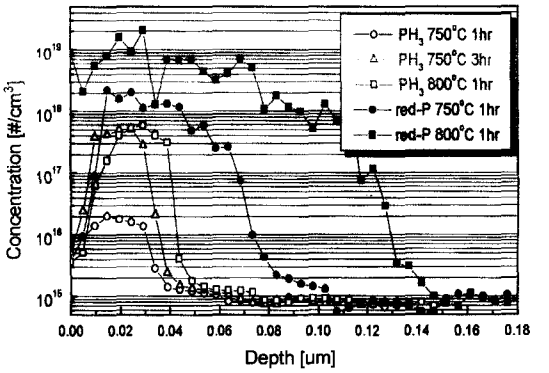

Fig. 4. ASR phosphorus concentration with respect to the different doping sources in single-crystal Si thin films.

junction profile was found in the case of solid P. These results explained that the increased defect density was caused by high doping level and high diffusivity was caused by increased defect density. The carrier concentration of P-dopant was measured by ASR as shown in Fig. 4. The samples doped at 700°C were not measured. ASR analysis revealed that phosphorus which were electrically activated doping concentration in the case of using solid P as a doping source was about 50 times as that of phosphine source at 750°C and 800°C. However, in the case of using solid P at 750°C and 800°C, the concentration of phosphorus in the heavily doped surface region was not different in SIMS results, but there was a difference of 1o times in ASR results. This result was caused because dopants, which were not fully activated in the condition of 1 min annealing at 850°C. In case of using solid P as a doping source, it is proved that the doping level near the surface area can be achieved about 50 times high as that of phosphine source at 750°C process temperature. In order to evaluate the electrical characteristics of doped polycrystalline Si films for semiconductor devices, MOS capacitors were fabricated to measure the capacitance of polycrystalline Si films. Fig. 5 shows a cross sectional view of capacitor. The experimental procedure and the experimental conditions to fabricate a capacitor are as follows.

First, Buffer oxide is prepared on p-type (100) silicon substrate by thermal oxidation. Next, HSG growing process was performed, followed by lightly doped polycrystalline Si of 6000 Å thick was deposited to use as a bottom electrode. After that, sample-1

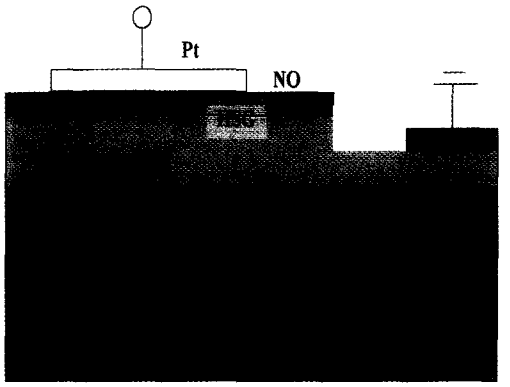

Fig. 5. Schematic diagram of a capacitor fabricated for measuring the capacitance of dielectrics.

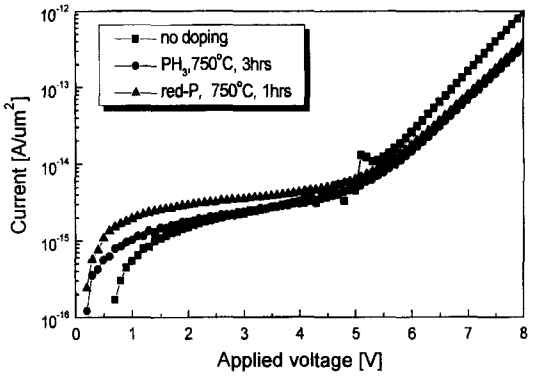

Fig. 7. Leakage current characteristics of capacitors with respect to the different doping conditions using HSG and NO.

was not doped additionally, sample-2 was doped by phosphine at 750°C for 180 min, and sample-3 was doped solid P at 750°C for 60 min, respectively. For dielectric material, SiN of 200 Å thick was deposited by LP-CVD method. To prevent leakage current, all samples annealed for 60 min at 800°C in oxygen atmosphere. To connect bottom electrode, the SiN and the heavy doping region near the surface of polycrystalline Si was selectively patterned by photo lithography and dry etching process. For the electrical measurement, Pt was used for the bottom and the top electrode. The bottom electrode was not masked and the top electrode was masked by dot mask. The area of top electrode was variously formed as a diameter of 100~1000 μm range. Finally, the fabricated capacitors were post-annealed at 500°C for 30 min in nitrogen atmosphere. The capacitance-voltage (C-V) characteristics were measured by using a HP4280A at 1 MHz by superposing 30 mV small ac signal on −2.5~2.5 V biases. The current-voltage (I-V) characteristics were also measured by using a HP4155B semiconductor parameter analyzer. A staircase-shaped dc bias voltage, with 0.1 V-high step and 2 seconds-long delay time, was applied to the platinum top electrode from 0 to −10 V while the bottom electrode was grounded. To evaluate C_{min}/C_{max} ratio, the measured C-V data were normalized in ±2 V measuring condition. In Fig. 6, Si films, doped with solid source, have 8% higher C_{min} than that of unadditional doped Si films and 3% higher C_{min} than that of Si films doped with PH_3 source. The leakage current of these films was a few fA/μm^2 as shown in Fig. 7.

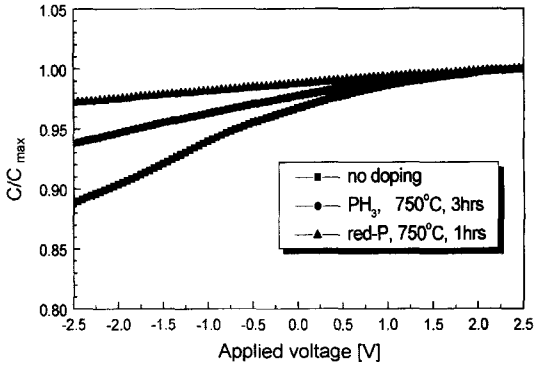

Fig. 6. Normalized capacitance value of capacitors with respect to the different doping conditions using HSG and NO.

IV. Conclusion

The doping concentration was increased as the process time increased, while the doping rate increased as the process temperature increased. As a result, phosphorus atoms piled up near the surface of Si films, and doping concentration swiftly reached to a saturation value at low temperature than at high temperature. Thus, in case of 2-zone diffusion method, it is proved that the heavy doping near the surface area can be achieved even at a relatively low temperature. SIMS analysis revealed that phosphorus doping concentration in case of using solid P as a doping source was about 50 times as that of phosphine source at 750°C. Also, ASR analysis revealed that the carrier concentration was about 50 times as that

of phosphine. In ±2 V measuring condition, Si films, doped with solid source, have 8% higher C_{min} than that of unadditional doped Si films and 3% higher C_{min} than that of Si films doped with PH_3 source. The leakage current of these films was a few fA/μm^2. Considering the doping concentration, however, this result did not meet the expectation. It seems that the increase of contact resistance, which is induced while capacitors are fabricated, deteriorates the electrical properties of the capacitors. In the gap area of HSG, the dielectric film was so thick that it cant increase the capacitance effectively. As a result, a 2-zone diffusion method is suggested as an effective method to achieve highly doped polycrystalline Si films even at low temperature.

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