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DSP 기반 위성 모뎀의 설계 및 구현
(Design and Implementation of DSP-based Satellite Modem Unit)

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요 약

본 논문은 DAMA-SCPC 위성통신 시스템의 디지털 모뎀의 기능 및 성능 규격들을 제시하고, 제시한 규격을 만족하는 위성모뎀의 구조 설계 및 구현에 대하여 기술한다. 다양하면서 융통성이 요구되는 위성모뎀의 규격들을 만족시키기 위하여 디지털 신호 처리기(DSP)와 프로그래머블 게이트 어레이(FPGA)를 기반으로 하여 설계 및 구현되었다. 구현된 위성모뎀은 DAMA-SCPC 위성통신 시스템에 통합하여 수행한 시험에서 안정된 동작과 제시된 기능 및 성능 규격을 모두 만족함을 검증하였다. 연속모드(at Eb/No=4.7, FEC=3/4)에서 측정된 BER은 약 1×10E-4의 성능을 보여 주었다.

Abstract

This paper describes the architecture and characteristics of the satellite modem unit (SMU) developed for the DAMA-SCPC Ground System(DGS), which is a Demand Assignment Multiple Access-Single Channel per Carrier (DAMA-SCPC) satellite network. There are several requirements for the SMU from the system architecture and design concept. To meet these requirements the SMU was designed and implemented by extensively applying digital signal processing (DSP) technique and field programmable gate array (FPGA). The developed SMU met the functional and performance requirements, and has been working well. The measured BER was about 1×10E-4 in continuous mode(at Eb/No=4.7, FEC=3/4).

I. Introduction

The DAMA-SCPC Ground System(DGS) is full mesh, centralized, single-hop DAMA-SCPC satellite network[1]. It provides the circuit-switched voice and data services. The satellite modem unit(SMU) has been developed to be applied to the DGS. The SMU exhibits many worth mentioning features such as high degree of flexibility and reliability, multiple operation modes, multiple transmit rates, the absence of any adjustment except TX power level, and finally, compact realization with single board[2-4]. The realization of such a versatile satellite modem unit is only possible by extensively applying DSP and FPGA techniques.

In this paper, we present the overview of the DGS including system architecture and features,

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and present the requirements for the SMU. We then describe the overall SMU architecture and the function and characteristics of each sub-unit using functional block diagrams. In addition, we present some aspects of implementation for each sub-unit.

Ⅱ. System Overview

The DGS provides satellite-based voice and data(up to 64 kbps) communication between two DAMA Remote Stations (DRS). DRSs are interconnected in a mesh configuration allowing communication by single hop. Call connection is established on demand(DAMA) or can be fixed assigned. The DGS network architecture is shown in Fig.1.

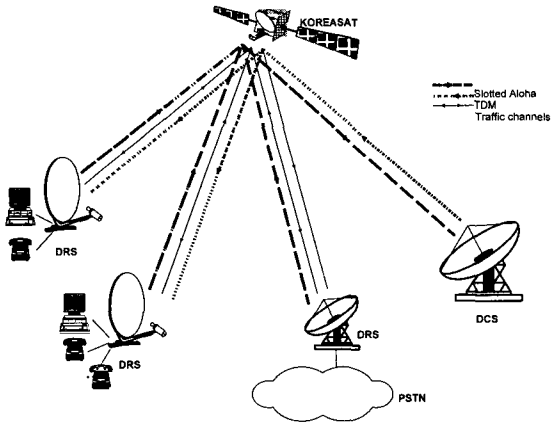


Fig. 1. DGS network architecture.
그림 1. DGS 시스템의 망 구조

The DAMA Central Station (DCS) controls the centralized network with maximum of 2,000 DRSs. The DCS continually transmits call setup information via broadcasting channel(outbound channel) in TDM mode. The information is addressed to specific remote stations, which continually monitor call setup information. When a DRS needs to communicate with the DCS, it transmits call request information via Slotted Aloha channel(inbound channel). All DRSs share the Slotted Aloha channel in a contention mode. The star network, which consists of these two channels, is called as service data network (SDN).

Call setup is provided over the SDN. When the subscriber goes off-hook and dials the destination number, the DRS transmits a call request via the Slotted Aloha channel. Upon receiving the request the DCS transmits the call setup information, which includes two traffic satellite channels to be used, to the calling and called DRSs. Two DRSs communicate with each other on the assigned traffic channels.

The DGS utilizes not only DAMA, but also low rate encoding of voice signals and voice activation of the satellite carrier (VOX) to provide maximum utilization on the space segment.

Ⅲ. SMU Requirements

In addition to the requirements derived from the above system architecture and features, the SMU should be totally redundant, i.e., it is required that any SMU can replace the SMU operating for the SDN when it fails. Moreover, the SMU is required to be implemented on single board.

In summary, the SMU has to meet the following requirements:

- Multiple operation modes : Voice (burst), Data (continuous), TDM (continuous), Slotted Aloha (burst)
- Independent configuration of each side(TX, RX) in any mode
- Two selectable FEC code rates(1/2, 3/4) and modulation type (BPSK, QPSK)
- Two selectable data rate(32kbps, 64kbps) in Data mode
- Short preamble length in burst mode, especially in Slotted Aloha mode
- ADCPM coding in Voice mode
- Voice activation in Voice mode
- Digital echo cancellation in Voice mode

- Exchange of signaling data between traffic SMUs via voice and data frame for call setup, release, and test of link connection during communication
- Small size : single board

All the possible configurations of the SMU are summarized in Table 1.

Table 1. All the possible configurations of the SMU.
표 1. 구성 가능한 SMU의 운용 모드

Mode	Data Rate (kbps)	FEC Code Rate	Modulation	TX Symbol Rate (Kbaud)
DATA	32.508	1/2	QPSK	32.508
VOX	32.508			
DATA	32.508	3/4	QPSK	21.672
VOX	32.508			
DATA	65.016	1/2	QPSK	65.016
DATA	65.016	3/4	QPSK	43.344
S/ALOHA, TDM	32.000	1/2	QPSK	32.000
TDM	32.000	3/4	QPSK	21.333
S/ALOHA, TDM	32.000	1/2	BPSK	64.000

In addition, for the frequency drift compensation, the SMU is required to use the frequency synthesizer with high resolution(<1Hz), and especially in TDM(RX) mode it can acquire the RX carrier with large frequency offset(up to 32kHz or more if necessary) and estimate the RX frequency error, which is reported to the station master processor, which is called as Common Processing Module(CPM), on request, in TDM (RX) mode. Moreover, the recovered clock(32kHz) in TDM RX mode is used to generate a reference system clock(2048kHz) for the network synchronization. The realization of such a versatile satellite modem unit is only possible by applying DSP technique and other advanced technology such as Surface Acoustic Wave (SAW) filter and Direct Digital Synthesizer (DDS).

Ⅳ. SMU Architecture and Implementation

The SMU is single board equipment, which consists of the following sub-units:

- Channel Unit Processor (CUP)
- Speech/Data Processor (SDP)
- Timing Distributor (TD)
- Modulator
- Demodulator
- TX/RX Frequency Synthesizers (TX/RX FSs)

The Fig. 2. shows the simplified block diagram of the SMU.

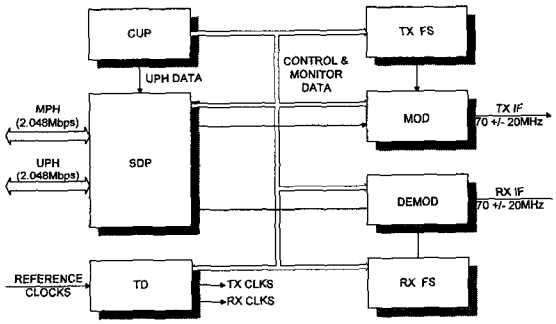


Fig. 2. Functional block diagram of SMU.
그림 2. SMU의 기능 블록도

The SDP processes the received data from one of two buses(i.e., Main PCM Highway (MPH) bus for exchanging continuous data or digital voice data with Telephone Data Card (TDC) or Trunk Interface Port(TIP) and Utility PCM Highway (UPH) bus for exchanging TDM or S/ALOHA data with CPM), and transmits the processed digital signal to the modulator. And also, it processes the received data from demodulator and transmits the resultant signal to one of the above buses. The CUP performs monitor and control of the overall SMU operation according to the CPM command and allows the CPM and the SDP to exchange the signaling data, via UPH bus.

The modulator accepts digital bit streams from SDP and provides a BPSK/QPSK modulated

carrier to the TX side of the RF subsystem. Its frequency is selected, according to the output frequency of the TX FS. The demodulator accepts the IF signal from the RX side of the RF subsystem and selects the wanted carrier by using the RX FS, and then performs BPSK/QPSK coherent demodulation by recovering the synchronous carrier and symbol timing from the selected carrier. It is operated in burst or continuous mode by control of the CUP.

The TX/RX FSs provide the sinusoidal signal for the modulator/demodulator's up/down conversion to selected frequencies on the nominal IF range from 50 MHz to 90 MHz.

1. Channel Unit Processor

Under control of the CPM, the CUP controls the SMU operation, reports the SMU status to the CPM. In addition, the CUP performs the following algorithms:

- Voice detection and noise evaluation in Voice mode
- Noise generation in Voice mode
- Aiding the frequency search and tracking in TDM RX mode
- Frequency correction of TX and RX FSs for frequency drift compensation in VOX, Data, and Slotted Aloha modes.

Moreover, it allows the CPM and the SDP to exchange the signaling data by writing signaling words into the assigned slot of the data frame at the TX side and extracting the received words from it at the RX side.

2. Speech/Data Processor

The block diagram of the SDP is subdivided in 11 functional blocks as shown in Fig. 3. The SDP functions include bus interfacing, ADPCM coding, voice activation detection with background noise evaluation/generation, digital voice echo canceling, signaling multiplexing/demultiplexing, channel encoding/decoding, burst generation/reassembling.

The bus interface provides the physical interfacing between the SMU and external bus. This block is composed of 485 bus driver/receiver for converting electrical level of incoming or outgoing signals via MPH/UPH buses, TX/RX data handler for extracting/inserting 32 or 64 kbps data of a specified slot from/to 2.048 Mbps bus stream, time slot assignment logic for providing assigned TX/RX slot timing by control of CUP. These functions are implemented by using high density FPGA and commercial 485-bus transceivers.

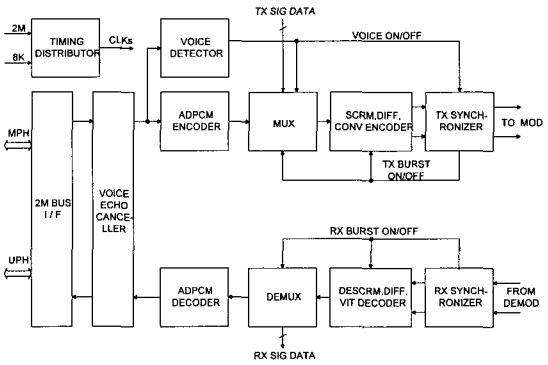


Fig. 3. Block diagram of SDP.
그림 3. SDP의 기능 블록도

The Adaptive Differential Pulse Code Modulation (ADPCM) codec converts conventional 64 kbps PCM signal into 32 kbps ADPCM signal and operates with voice band data (up to 4.8 kbps). The CCITT G.721 standard is used as the ADPCM algorithm for voice compression. It is controlled the selection of the PCM companding law by the CUP. The commercial product is used.

The voice activation detector[5] detects beginning and ends of voice burst to activate transmit satellite carrier. When voice burst is not detected, the transmit carrier is turned off. The detection algorithm is based on short-time energy level, short-time energy variation and zero crossing rates. The decision criterion of voice existence is examined in every 4 ms and hangover duration is 96ms. In addition, to give smoother transition between voice and idle period on receive side, the power level of background noise is evaluated on the transmit side, transmitted over the channel,

and used to generate the idle channel noise level. The evaluation period is 16 ms just after every talk-spurt and noise level to be transmitted is quantized in 2-bit, the maximum level to be inserted is limited about −40 dBm0 on receive side. This function is implemented in a part of DSP chip, which is used mainly to implement CUP function and programmed in C-language. The main parameters of voice detector are as follows.

- Operation time : 16 ms max.
- Hangover time : 96 ms
- Comfortable noise level : −42 dBm0 max.

The voice echo canceller removes echoes on satellite voice circuit. The voice echo canceller is designed to meet performance requirements of ITU-T G.165 for type C digital echo canceller. This echo canceller is capable of handling of tail circuit delays up to 25 milliseconds (200-tap) with the hybrid loss of minimum 6 dB. Final echo return loss enhancement (ERLE) after convergence in excess of 65 dB has been obtained and after 500 ms, the ERLE of 35 dB is measured. In addition, the tone, having frequency of 2,100Hz with periodic phase reversal and level of more than −31 dBm0, is detected by tone disabler algorithm. This detection signal is used to disable echo cancellation function to ensure proper operation of V-series modems. These two functions are implemented in a DSP chip and programmed in assembly language. The main parameters of the employed echo canceller are as follows.

- Tail circuit delay : 25 msec max.
- Final echo return loss
  - Nonlinear processor off : <=−36 dBm0
  - Nonlinear processor on : <=−65 dBm0
- Convergence rate : >= 27 dB in 500 msec
- Tone frequency range : 2,100 +/−21 Hz
- Tone phase reversal period : 450 +/−25 ms
- Tone phase inversion : 180 +/−25 degree

The MUX generates the multiplexed frame *including* start of frame(SOM) for frame *synchronization, traffic data(voice or continuous* data), flag for indication of frame formation, and signaling data for call set-up information or background noise level transferring. The frame generation is controlled by event counter output. The CUP controls the signaling data transferring. The DEMUX demultiplexes the received frame into traffic data and signaling data respectively, being based on frame synchronization by SOM detection. The SOM detection, for frame timing acquisition, is performed by complicated state machine with aperture control and it is consists of six state. There are two kinds of sate machines, due to different performance requirements; VOX or DATA operation mode. The flag detector *provides frame formation and timing to CUP, to* exchange signaling data. Fig. 4. shows the state diagram for frame synchronization acquisition in voice mode. In zero state, to reduce false detection, open aperture with low SOM detection threshold is applied and others' states have closed aperture with high detection threshold. These functions are implemented by using two FPGAs and two commercials FIFO buffers for data rate adaptation.

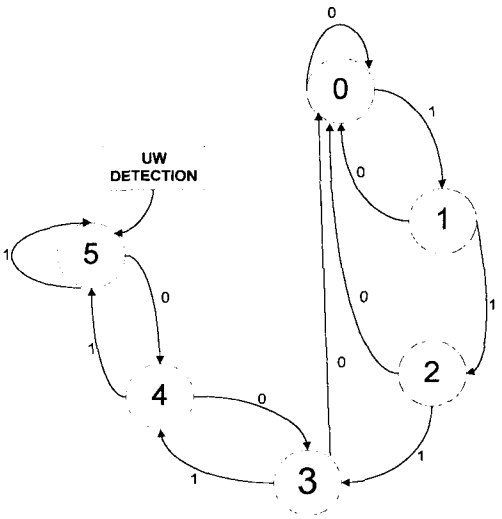


Fig. 4. The state diagram of frame sync. acquisition

그림 4. 프레임 동기 획득을 위한 상태 천이표

The channel codec block performs scrambling/descrambling, binary differential encoding/decoding and convolutional encoding/viterbi decoding. A self-synchronizing scrambler that meets the ITU-T V.35 standard is used to randomize the transmitted data for energy dispersal. The scrambler and descrambler are reset to a known value at the beginning of every burst.

To remove 180-degree phase ambiguity, the binary differential encoder/decoder is used. The convolutional encoder and viterbi decoder are utilized to provide better data integrity for operation with low Eb/No input signals. This codec provides 5.2 dB coding gain in rate 1/2 as compared to no coding. The generation polynomials of encoder are GP1 = $1+X+X^2+X^3+X^6$ and GP2 = $1+X^2+X^3+X^5+X^6$. It is designed to operate in combination of rate 1/2, 3/4(punctured coding) and modulation type BPSK, QPSK and continuous, burst mode. The selection of operation mode is controlled by CUP. These functions are implemented by using a FPGA and a commercial viterbi decoder. For proper operation in burst mode, additional circuits are designed and implemented. The preamble and postamble of burst are not processed in channel codec block.

The TX synchronizer generates the burst including preamble for carrier and timing recovery in the demodulator, unique word(UW) for detection of burst start timing and phase ambiguity resolution, multiplexed frame(voice) or data packet(S/ALOHA), dummy bits for proper operation of channel codec and postamble for detection of burst end timing. It also provides synchronized timings to the other blocks on the transmit side. The length of preamble, unique word and postamble of burst are selectable, according to the operation mode because of different threshold Eb/No. On receiving a start of burst(SOB) signal from the demodulator, The RX synchronizer starts to wait for UW. When detecting UW, it resolves the phase ambiguity using UW detection states and provides synchronized timings to the other blocks on the receive side. The unique word and postamble detection is based on the digital correlators with a decision logic. The detection thresholds of UW and postamble should carefully be decided by considering both of their miss and false-alarm probabilities. It is noted that the UW and postamble of burst are not encoded. When postamble is detected, it sends end of burst(EOB) signal to the demodulator to be ready for new burst. These functions are implemented by using two FPGA chips. Fig. 5. shows the burst structure in voice mode.

- 192 or 96-symbol preamble
- 32 or 24-symbol unique-word
- 6 or 4-symbol dummy bits
- 32 or 24-symbol postamble

Fig. 5. Burst structure in voice mode.
그림 5. 음성모드의 버스트 구조

3. Timing Distributor

The timing distributor provides the 11 clocks required on the SMU for operation. The reference clocks(2.048 MHz, 8 kHz) are provided by the CPM. These clocks are divided according to SMU operation mode and are resynchronized with 8 kHz. This function is implemented by using a FPGA and commercial PLL chip.

4. Digital Modulator

The digital modulator[6] is shown in Fig. 6. The the Stored Waveform Generator(SWG) accepts I and Q channel data streams from the SDP in either case of BPSK and QPSK(in BPSK, the two streams are the same), and performs the digital filtering for each binary stream and the digitall quadrature up-conversion of the filtered I and Q channel samples. Moreover, zeros(0s) are

repeatedly inserted between two samples in the output sequence, such that the wanted spectral component is located on the linear region of DAC's frequency characteristics curve. In reality, these are performed together using a lookup table. The SWG is implemented by using an EPLD and a PROM. A digital-to-analog converter then converts the modulated samples into analog waveforms at a low intermediate frequency(IF). There is no phase and amplitude unbalance on I and Q outputs and only one DAC is used due to the digitally modulated carrier.

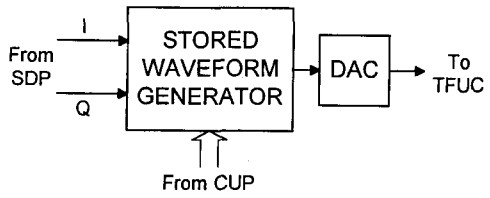


Fig. 6. Block diagram of digital modulator.
그림 6. 디지털 변조기의 기능 블록도

Fig. 7. shows the digital low-IF modulator output and the final IF output in the case of symbol rate 43.344Kbaud, QPSK, and roll-off factor 0.3.

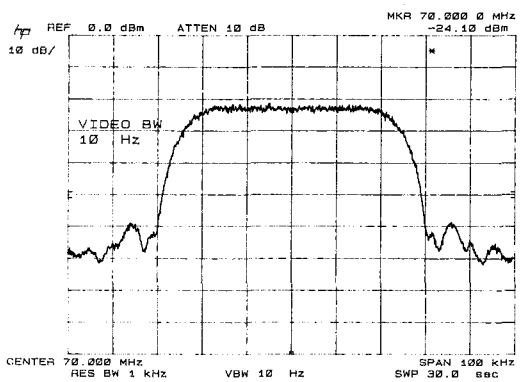


Fig. 7. Spectrum of the modulated carrier.
그림 7. 변조된 반송파 스펙트럼

5. Digital Demodulator

As shown in Fig. 8, the digital demodulator[7-11] has been fully digital-implemented using DSP technique. An Analog-to-Digital Converter (ADC) first samples the low-IF signal. Two DSP chips then process the resultant samples. The first DSP chip performs the down-conversion of the low-IF input samples to baseband via the digital quadrature demodulator and the decimating filter(2 samples/symbol) whose decimation factor is selected, according to the symbol rate, by the CUP. The CUP changes the second DSP chip's operation, according to the operation mode. It performs carrier recovery, timing recovery, and Automatic Gain Control(AGC), which is for soft-decision decoding, in any operation mode. In addition, in burst operation mode it estimates parameters using a preamble and then closes the loops(carrier recovery, timing recovery, and AGC loops) with the estimated parameters as the initial values, and in continuous operation mode it performs Automatic Frquency Control(AFC). For each loop, loop bandwidth could be S/W controllable if necessary. The timing correction is performed by an interpolating filter except in TDM mode, where an external VCXO driven by the internal clock recovery algorithm is used to synchronize the sampling clock as shown in Fig. 8. The VCXO output is frequency-divided to 32kHz and is used to generate a reference system clock(2048kHz) for the network synchronization in the CPM. Moreover, in TDM mode, the second DSP chip periodically delivers the frequency error to the CUP for frequency drift compensation.

Fig. 9. shows examples of the demodulated sample stream at Eb/No=∞ and Eb/No=8, which

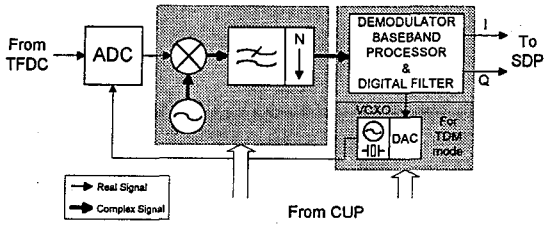
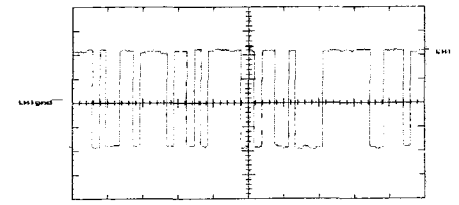
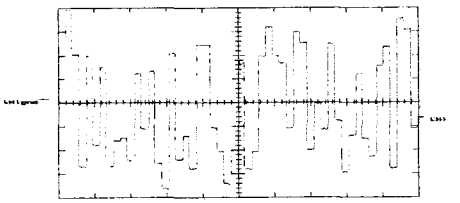


Fig. 8. Block diagram of digital demodulator.
그림 8. 디지털 복조기의 기능 블록도



Eb/No = ∞



Eb/No = 8

Fig. 9. Examples of demodulated sample stream.
그림 9. 복조된 스트림 파형

are quantized with 3 bits for soft decision viterbi decoding.

6. Up/Down Converters

In Fig. 10, the Tunable Frequency Up Converter (TFUC) performs an up-conversion of the low-IF(first IF) signal. The low-IF input signal is first mixed with the Reference Signal Generator(RSG) to be converted to the second IF. This one, after a sharp bandpass filtering by a sharp narrowband SAW filter, is mixed with the TX FS output to be converted to the assigned frequency within 7020 MHz. The final IF signal is fed into a digital controlled attenuator with 1 dB step, which is controlled by the CUP, to control the TX power level. Finally A switch is followed to control TX output on/off for burst mode operation.

The Tunable Frequency Down Converter (TFDC) performs a down-conversion of the input IF signal to the low-IF signal. The input IF signal is first mixed with the RX FS and then filtered by a sharp narrowband SAW filter to select the assigned channel. The resultant signal is mixed with the RSG output to be converted to the low-IF. This signal is filtered by an Anti-Ailiasing filter(AAF) and amplified by a variable gain amplifier, which is set manually, and sent to the ADC of the low-IF demodulator.

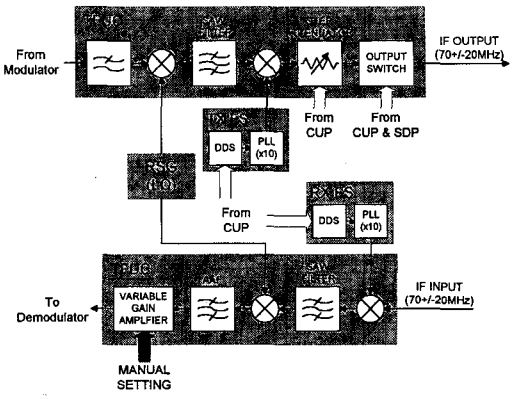


Fig. 10. Block diagram of up/down converters.
그림 10. 상향/하향 주파수 변환기의 기능블록도

As mentioned before, the resolution of the FS is required to be very high. To meet this requirement, we have developed a DDS/PLL hybrid synthesizer(or DDS-driven PLL). The resolution of the developed FS is less than 0.01Hz.

As shown in Fig. 10, the FS consists of two parts, i.e., a Direct Digital Synthesizer (DDS) and a Phase Locked Loop (PLL).

The DDS outputs a sinusoidal waveform at the frequency determined by the programming data from the CUP. The DDS output is used as the reference to the PLL. The PLL accepts the DDS output signal and outputs a carrier whose frequency is 10 times more than the DDS output, i.e., the PLL acts as a frequency multiplier for the signal to its reference input.

The above five analog subunits have been implemented with completely independent modules, which can be easily inserted and removed. In addition, no tuning is required for these modules(except the TX output level). These facts make the test and/or maintenance very easy.

Fig. 11. shows the photograph of the developed SMU with the shildering cover removed.

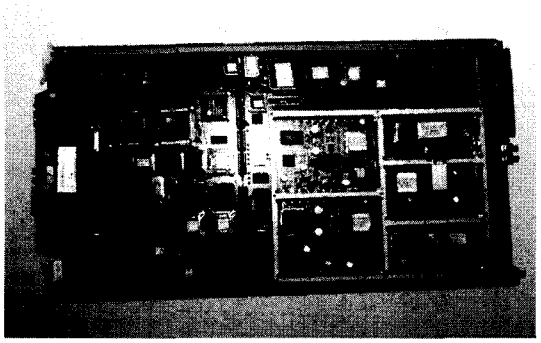


Fig. 11. Photograph of the implemented SMU.
그림 11. 구현된 SMU 사진

The measured BER performance was about 1× 10E-4 in continuous mode, at Eb/No = 4.7dB. The BER was measured by using HP3784A and under following environments:

- Operating freqency : 14GHz/12.25GHz
- Antenna size: 2.4m
- Modulation: BPSK
- Operating mode: continuous
- FEC rate: 3/4
- Data rate: 32kbps

V. Conclusion

By extensive use of DSP and other programmable logic, a highly flexible and compact digital satellite modem unit has been developed. It has been integrated on the DAMA-SCPC ground system and working well and conformed that it met all initial objectives and the system requirements. The measured BER was about 1× 10E-4 in continuous mode(at Eb/No=4.7, FEC= 3/4). Now we are developing some additional functions, such as on-line BER estimation, required for enriching the system features and/or improving the system performance.

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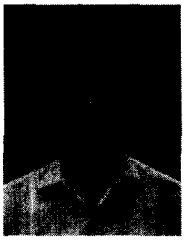

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