The Implementation of the Built-In Self-Test for AC Parameter Testing of SDRAM

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Abstract

We have proposed BIST method and circuit for embedded 16M SDRAM with logic. It can test the AC parameter of embedded 16M SDRAM using the BIST circuit capable of detecting the address of a fail cell of a 16M SDRAM installed in an Merged Memory with Logic(MML) generating the information of repair for redundancy circuit. The function and AC parameter of the embedded memory can also be tested using the proposed BIST method. The total gate of the BIST circuit is approximately 4,500 in the case of synthesizing by 0.25㎛ cell library. and verify the result of Verilog simulation. The test time of each one AC parameter is about 200㎳ using 2Y-March 14N algorithm.

Ⅰ. Introduction

In general, system used for information and communication includes memory devices and logic devices for control, operation and interface function. In conventional system, the logic devices and the memory devices are separate. However, as the need for low cost systems increases, together with developments in a semiconductor design and fabrication technology, research has been conducted into a single semiconductor chip containing both logic devices and memory devices. Actually, technology of integrating a logic semiconductor device and a small capacity, SRAM in a single chip is conventional. However, recently much research has been conducted into the technology of integration a DRAM, particularly, a common EDO(Extended Data Out) DRAM or SDRAM (Synchronous DRAM) having a large capacity from 1Mbit to 32Mbit, with devices in a single chip. As the semiconductor device is advanced to integrated system on a chip such as MML(Merged Memory with Logic) or embedded DRAM, it is impossible to connect every internal pad for voltages or signals related to embedded memory with external pin, because of the embedded memory has been tested by a direct access method.[2][3][4] According to the direct access method, a tester can directly access the memory in a test mode, such that the tester generates an address, test input and control signal according to a memory test algorithm, compares the test input with data output,

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thereby testing the memory. According to this method, a multiplexer is inserted into an input port of the memory and the input selected in a test mode is connects to IO pins. However, the direct access method has the disadvantage that the number of test pins is too many, and delay from the output of the memory to the final pad changes the measured value. Thus, it is difficult to accurately obtain the AC parameter of the memory. Also it is impossible to test the parameters at the real clock rate of 100㎒ because of the memory tester limitation. The functions and AC parameter of the embedded memory can also be tested using a BIST(Built-In Self-Test) method. In the BIST method, a BIST circuit is installed in an MML interface circuit. The merit of this method is that the functions of the memory are measured at the real clock rate by using a logic tester. However, the BIST method shows the result of whether or not the memory has failure as only one bit. Thus, it is difficult to detect the row and column addresses of the fail cell, so the application of a redundancy circuit is impossible. Also, because the fail test is performed on all the cells by using a read/write/read pattern composed of a single test parameter, it is impossible to analyze which AC parameter has no margin.[5].[6]

We present a BIST circuit capable of testing 16M Synchronous DRAM installed in a MML with multiple AC parameters. It is another objective to provide a BIST circuit capable of detecting the address of a fail cell of a 16M Synchronous DRAM installed in an MML. The proposed idea using the 16M Synchronous DRAM is different from the circuit of described in Chintsun et al., which has the BIST circuit using the 1M EDO DRAM.[1]

II. The Proposed BIST Method

2.1 SDRAM Specification

Table 1. shows some interesting features of 16M SDRAM for explaining the proposed BIST circuit. It has the organization of 512 Rows, 256 Column, 2 Banks and 64 IO.[7]

Table 1. Features of the 16M Synchonous DRAM

Name	Features
Operation	Dual bank, synchronous operation
Power Supply	6 pairs of 3.3V and Ground
Input/ Output	x64 separate data input and output
Address	Non-multiplex 512 row and 256 column
Refresh	Auto and self refresh mode
Refresh cycle	1024cycles/16㎳ (512 cycles/each bank)
CAS latency	2 only
Burst length	1 only
Clock cycle	100㎒ (maximum)
Loading	2.0㎊

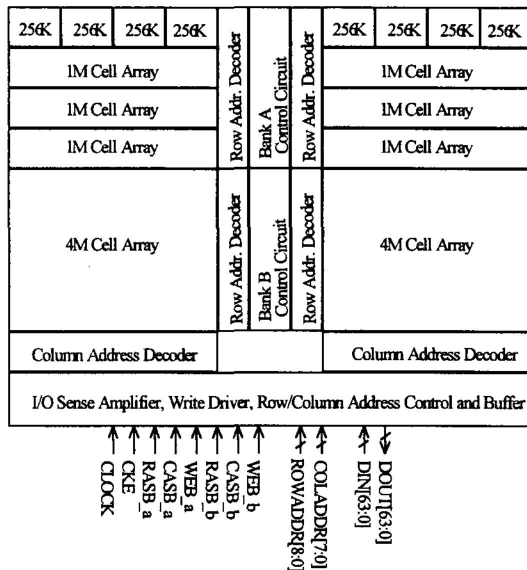

Fig. 1. Embedded 16M SDRAM architecture

Figure 1. shows the 16M SDRAM core architecture that has the 2 banks, each organized 8M array and 512 row, 256 column decoder. This 16M SDRAM core has been modified for better performance and optimized specially for embedded

DRAM and logic products. The separate data Input/Output and non-multiplexed row and column address are implemented. The basic timing and AC/DC parameters are based on existing 100MHz Synchronous DRAM. An initial pause of 20μs is required after powerup.

Table 2. lists the operating AC parameters for the same or different bank.[8]

The CAS latency of the embedded SDAM is 2. Figure 2. shows the Read/Write timing diagram and the AC parameters of the 16M SDRAM.

Table 2. Operating AC parameter of the 16M Synchronous DRAM

Parameter	Symbol	Same Bank	Diff. Bank	Unit
Row active to Row active delay	t_{RRD}	-	20	ns
RASB to CASB delay	t_{RCD}	30	-	ns
Row precharge time	t_{RP}	30	-	ns
Row active time	t_{RAS}	60	-	ns
Row cycle time	t_{RC}	90	-	ns
Last data into new col. address delay	t_{CDL}	10	-	ns
Column address to col. address delay	t_{CCD}	10	10	ns

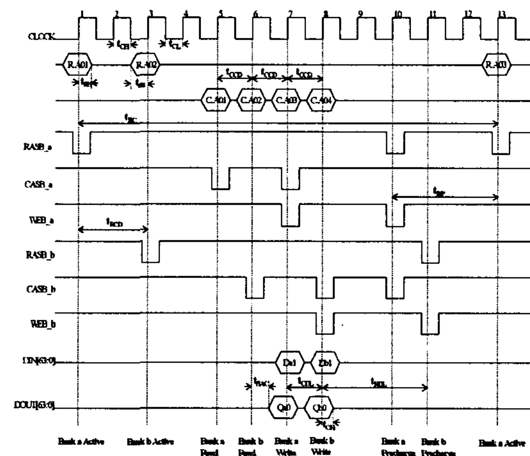

Fig. 2. 16M SDRAM Read-Write timing diagram

For embedded 16M SDRAM, which has no

pin count limitation, DIN and DOUT can be separate to simplify control, output enable OE can be removed without functionality. This timing diagram shows the interleaving Read/Write a and b bank of the 16M SDRAM.

The 2 bank acts independently and can be used interleaving read-write method.

2.2 The Function of BIST

Figure 3. shows the proposed Built In Self Test circuit, the interface circuit and the embedded 16M SDRAM. It comprises a BIST block generating a predetermined

Fig. 3. Embedded SDRAM connected to the proposed BIST circuit

BIST information signal in response to an external clock signal TCLKT and a logic information signal output from the logic circuit, in a normal mode, and outputting a signal to the memory by receiving the external clock signal and the BIST information signal. The BIST block detects the fail address by comparing data written to the memory with data output from the memory.[12]

The BIST circuit consists of a BIST information signal generator for outputting input data and control signal to the memory via the switch multiplexer while communicating with the BIST information signal generator and a expected/real DOUT comparator for comparing the input data generated by the BIST information signal generator, with real output data read from the memory.

In the Figure 3, the input MUX receives a logic information signal INL generated by a logic circuit and the BIST information signal BISTOUT, and provides the memory with a signal generated by the logic clock signal INL in the normal mode and a signal part includes a clock MUX and an input data MUX. The clock MUX receives a logic clock signal TCLKL generated by a logic circuit and an external clock signal TCLKT input from the outside, in a BIST mode. The memory installed in the embedded SDRAM can be tested by each AC parameter, to obtain information about the parameter.

III. Implementation

The proposed BIST circuit includes a BIST information signal generating portion, and address generating block.

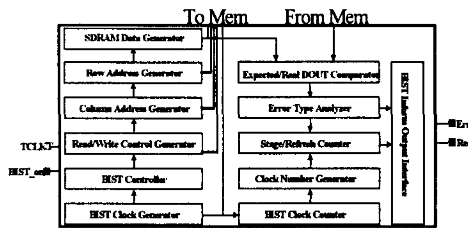

Fig. 4. The proposed BIST circuit

In the Figure 4, the BIST controller outputs input data DIN[63:0] and a control signal CON to the memory via the input 2X1 MULTIPLEXER ARRAY CIRCUIT in response to the external clock signal TCLKT and the BIST mode direct signal BISTON, in the BIST mode. The data generator output the same data as the input data DIN[63:0] generated by the BIST controller to the comparator.

The BIST portion generates a BIST information signal BISTOUT in the BIST mode, which includes a row address ROW-ADD-[8:0], a column address COLADDR[7:0], row strobe signals RASB_a and RASB_b of first and second banks, column strobe signals CASB_a and CASB_b, write enable WEB_a and WEB_b and input data DIN[63:0]. The BIST block compares data DIN[63:0] to be written to the memory with data DOUT[63:0] output from the memory, thereby detecting the address of a fail bank and an AC parameter causing the failure.

The address generating block outputs the addresses ROWADDR[8:0] and COLADDR[7:0] to the input MUX while communicating with the BIST information signal generator. The address generating block includes a stage counter. The stage counter directs change in mode for writing data to the memory or reading data from the memory. For example, test data is written to all addresses in a stagte 0, and the content of the addresses is read at a stage 1 by increasing the address number. Then, a determination of whether or not the content of the address is the same as the test data written in the stage 0, and a test data bar is written to the same address. Then, the same steps are repeated to the next address. The test data bar is read from each address in a stage 2 by decreasing the address number, and then the read test data bar is checked to determine whether or not the read test data bar is the same as the written test data. The test data is the written, and the pattern is read in the address.

The pattern is read from each address in a stage 3 and then it is determined whether or not the read pattern is the same as the pattern written in the stage 2. During the above steps, it can be detected whether or not the memory is in failure or not. The address counter designates an address by sequentially increasing or decreasing the address number of the memory. The comparator compares the output signal of the data generator with an output signal DROUT[63:0] output from the memory to generate a fail indication signal ERROR indicating whether or not the memory is in failure. That is, if failure occurs in the memory, the fail indication signal ERROR goes to 1 and otherwise the fail indication

signal ERROR is 0. The fail address indicating block stores the address of the memory of which the input data and the output data are different. Also, the fail address indicating block includes a clock counter and a clock number register. The clock counter counts the number of clock cycles until an error is detected in the memory.

The clock number register stores the number of clock cycles counted by the clock counter. The values stored in the clock number register are output in series after the test, as a redundancy information signal REDUN. The refresh counter counts the number of refreshes of the memory in a refresh mode while communicating with the BIST information signal generator.

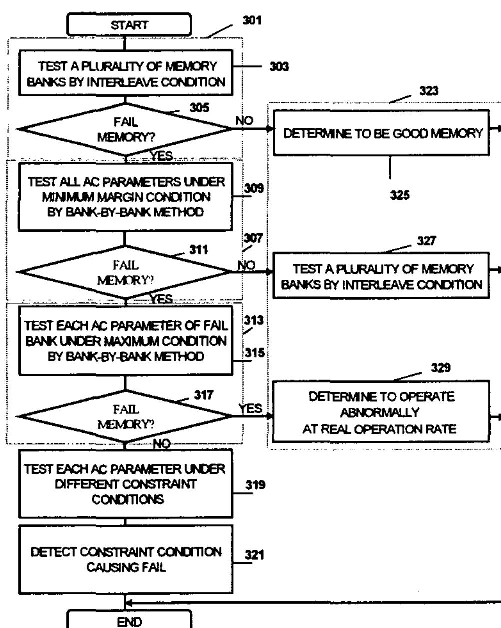

Fig. 5. Flowchart of the BIST circuit

Fig 5 is a flow chart illustrating a BIST method using the BIST circuit according to the paper. First, in step 301, a plurarity of banks are tested by an interleaving method (step 303) in order to determine whether or not the memory has failure (step 305). If it is determined in the step 301 that the memory has a fail bank, in step 307, AC parameters of each bank are tested by the bank-by-bank method under the minimum margin condition (step 309), to test whether or not the memory has failure (step 311). Also, if it is determined in the step 307 that the memory has a fail bank, in step 313, all AC parameters are tested by the bank-by-bank method under the maximum margin condition (step 315), to test whether or not the memory has failure (step 317).

Then, if the memory has no failure, each AC parameter is tested under different constrained conditions (step 319), and the corresponding constrained condition where the failure is detected is recognized to reveal the particular constrained condition under which failure occurs (step 321). In step 323, if it is determined in the step 301 that the memory has no fail bank, the memory is determined to be good (step 325). Also, if it is determined in the step 307 that the memory has no fail bank, the memory is determined to cause failure in the interleave read/write condition (step 327). If the memory is determined to have failure in the step 313, it is determined that the memory does not operate normally at a real operation rate (step 329).

The proposed BIST architecture described has been verified on Verilog RTL(Register Transfer Level) language. We used the test algorithm of 2 Y-March 14N which is the Y-March 14N with internal checker board and Y-March 14N with 5&A pattern. The test module consists of the 16M SDRAM model and the proposed BIST circuit with Verilog Register Transfer Language description. The size of the BIST circuit is about 4500 gates when synthesis this behavioral model using the .25㎛ 1poly 4 metal STD100 CMOS cell library. The test time of the proposed BIST circuit is approximately 200㎳ in the case of no AC parameter error for interleaving read/write test pattern. We made the error of the each AC parameters on the 16M SDRAM model step by step, then check the result of ERROR on the Figure 5. and output the REDUN which reports the address location of the fail bit cell. All aspects of the proposed BIST architecture described have been demonstrated with this Verilog Register Transfer Level mode, and the result of the simulation is the same of the expected output on the Verilog simulator.

Ⅳ. Conclusion

We have proposed BIST method and circuit for embedded 16M SDRAM with logic. It can test the AC parameter of embedded 16M SDRAM using the BIST circuit. This BIST design is based on the embedded 16M dual bank Synchronous DRAM. We present a BIST circuit capable of testing 16M Synchronous DRAM installed in a MML with multiple AC parameters. The proposed BIST circuit also has the capable of detecting the address of a fail cell of a 16M Synchronous DRAM installed in an Merged Memory with Logic. The functions and AC parameter of the embedded memory can also be tested using the proposed BIST method. In the future, it will design on an implementation of this circuit using 0.25um design rule and verify the result of Verilog simulation. While this paper has been illustrated and described with reference to a specific 16M 2-bank SDRAM, further modification and alternations within the algorithm and circuit of this content will be implemented the other MML architecture.

Ⅴ. Reference

[1] Chih-Tsun Huang, Jing-Reng Huang, Chi-Feng Wu and Tsin-yuan Chang, "A Programmable BIST Core for Embedded DRAM", IEEE Design & Test of Computers, Vol.16, No.1, pp.59-70, Jan- Mar 1999.

[2] Shinji Miyano, Katsuchhiko Sato and Kenji Numata, "Universal Test Interface for Embedded DRAM Testing", IEEE Design & Test of Computers, Vol.16, No.1, pp.53-58, Jan-Mar 1999.

[3] Subramana S. Iyer and Howard L. Kalter, "Embedded DRAM Technology: opportunities and challenges", IEEE Spectrum, Vol.36, No.4, pp.56-64, April 1999

[4] Yervant Zorian, "Testing the monster chip", IEEE Spectrum, Vol.36, No.7, pp.34-44, July 1999

[5] S. Hellebrand, "Error Detecting Refreshment for Embedded DRAMs", Proceeding of the 1999 17th IEEE VLSI Test Symposium, April 1999

[6] J. Dreibelbis, John Barth, Howard Kalter and Rex Kho, "Processor-Base Built-In Self-Test for Embedded DRAM", IEEE J. Solid-State Circuits, Vol.33, No.11, pp.1731, November 1998

[7] Samsung Electronics, ASIC STD90 Design Manual Preliminary, April 1998

[8] Samsung Electronics, Synchronous DRAM Data Book, Jan 1998

[9] S.B. Park, MML(Merged Memory Logic), IDEC, August 1998

[10] CHIPs and Technology, 69000 HiQ Video Accelerator with Integrated Memory Data Sheet, Feb 1997

[11] D&T Roundtable, "Testing Mixed Logic and DRAM Chips", IEEE Spectrum Vol.15, No.2, pp.86-92, Apr-June 1998

SDRAM 의 AC 변수 테스트를 위한 BIST 구현

박상봉*

요약

본 논문에서는 내장된 SDRAM 에 대한 기능 및 AC 변수를 테스트하는 BIST 회로의 알고리듬 및 회로 구현을 기술하였다. 제안된 BIST 회로를 사용하여 내장된 SDRAM 의 고장난 비트 셀의 어드레스 위치를 출력시킴으로써 Redundancy 회로 사용에 관한 정보를 제공하도록 설계하였다. 또 실지 동작 주파수에서의 내장된 SDRAM 의 AC 변수에 대한 테스트를 수행하여 메모리의 오동작이 발생된 경우 어떤 AC 변수가 설계 사양을 벗어나는지를 출력하도록 구현하였다. 0.25㎛ 셀 라이브러리를 이용하여 회로 합성하는 경우 전체 게이트 수는 약 4,500 개 정도이고, Verilog 레지스터 전송 언어를 사용하여 설계 및 시뮬레이션을 통하여 검증하였다. 하나의 AC 변수에 대해서 2Y-March 14N 알고리듬으로 테스트하는 경우 100㎒ 동작 주파수에서 테스트 시간은 200㎳ 정도이다

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