Fabrication of MFISFET Compatible with CMOS Process Using $SrBi_2Ta_2O_9$ (SBT) Materials

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(Received 2 March 2000, Accepted 24 March 2000)

Metal-ferroelectric-insulator-semiconductor field effect transistors (MFISFETs) were fabricated using CMOS processes. The Pt/SBT/NO combined layers were etched for forming a conformal gate by using Ti/Cr metal masks and a two step etching method. By this method, we were able to fabricate a small-sized gate with the dimension of 16/4μm in the width/length of gate. It has been chosen the non-self aligned source and drain implantation process. We have deposited inter-layer-dielectrics (ILD) by low pressure chemical vapor deposition (LPCVD) at 380°C after etching the gate structure and used TiW metal layers for metallization. The memory window and the threshold voltage of p-channel MFISFETs were about 1.0 and −2.1V, respectively. It was also observed that the current difference between the I_{ON} (on current) and I_{OFF} (off current) that is very important in sensing margin, is more than 100 times in I_D-V_G hysteresis curve.

Keywords : MFISFET, SBT, Si_3N_4, memory window, ferroelectric transistor

1. INTRODUCTION

Metal-ferroelectric-insulator-semiconductor field effect transistor (MFISFET) using $SrBi_2Ta_2O_9$ (SBT) ferroelectric materials have recently been widely studied and much attracted for a memory application. The MFISFET device, in which the gate is controlled by the spontaneous polarization of ferroelectric materials, has the potential advantages of applicability of the scaling rule and non-volatility unlike conventional FeRAMs. MFISFET device had brought out as a byproduct of metal-ferroelectric-semiconductor field effect transistor (MFSFET) device. For MFSFET, it is necessary that ferroelectric films must be deposited directly onto the semiconductors.

In this case, it is necessary that the ferroelectric film maintains its ferroelectric properties on the semiconductor and the interface state density at the ferroelectric film/semiconductor interface must be low for normal FET operation. Even though MFSFET device has been studied so far [1-4], there are few reports demonstrating its ferroelectric properties directly on semiconductor. Actually natural oxide is formed onto Si even though any process is made onto it. This unstable interface layer may not make the FET operable well. Therefore we got to choose MFISFET structure instead of MFSFET structure [5].

MFISFET device may have merits in aspects of high switching speed, non-volatility, radiation tolerance, and high density.

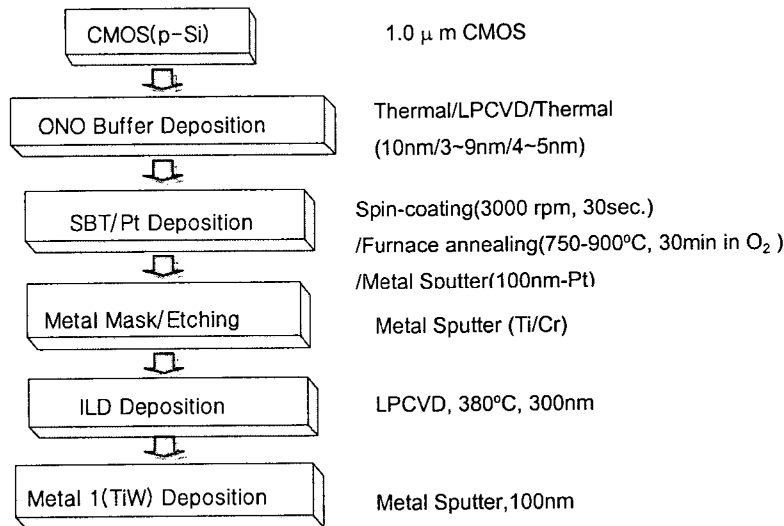

Fig. 1. Flow diagram of the experimental procedure.

high density. However there are several problems to overcome to realize the integration of these into semiconductor devices. Certain intermediate layers have to be incorporated between Si and ferroelectric layer to obtain a stable interface. These intermediate layers should have high dielectric constant, low leakage current, good interface characteristics and compatibility with CMOS process. Y_2O_3[6], CeO_2[7], $PbTiO_3$[8] and $SrTiO_3$[9] have been proposed as intermediate layers, but these materials have some disadvantages, which have not standard processes and mature tools for device integration yet. Therefore it can make the interface between ferroelectric materials and Si substrate unstable. The other problem is the etching of gate module. Minimizing the gate size depends on the etching technology wholly. Ferroelectric materials and Pt top electrode have been known to be very tedious materials for etching.

Therefore, it is necessary to develop a stable thin film process of intermediate layers and etching process for fabricating the MFISFET structure. We have tried to use NO layers as intermediate layers, which are considered to have immunity to ion drift and to bring out clean surface between Si-SiO_2[10]. And also we have developed etching process by using Ti and Cr metal mask. Thus, we could get the stable MFISFET device that the width/length of gate is 16/4 μm.

2. EXPERIMENTAL PROCEDURE

We have processed CMOS fabrication by non-self align process. We implanted Phosphor so that n-well concentrations became 6.0×10^{12} cm^{-2} by using a (100) p-type Si wafer. After the threshold voltage implantation was made, we formed source and drain regions. After that, the wafer was thermally oxidized to form a SiO_2 film, and a Si_3N_4 thin film was deposited using low pressure chemical vapor deposition (LPCVD). SBT solutions made by metal organic decomposition (MOD) were spin-coated at 3000 rpm for 30 seconds and subsequently dried at 250°C for 10 minutes. Two more cycles were repeated to obtain the desired thickness of 200nm. And SBT films were annealed at 750 - 900°C for 30min in O_2. Then, top electrode of Pt was deposited using DC sputtering at 200°C. Cr and Ti metals were deposited using DC sputtering as masks for gate module. The gate structure including Pt, SBT and NO was etched by inductively coupled plasmas (ICP)-reactive ion etcher using a two-step etching process which means two separate processes with different etching gas combinations. After etching of the Pt/SBT/NO gate module, recovery annealing of SBT films was made at 900°C for 30min in O_2. SiO_2 was deposited using LPCVD at 380°C as an inter-layer-dielectric (ILD) material. After ILD process, a proper annealing was made again. And metal contact etch and TiW deposition for metallization were followed. All lithography

processes on the back-end process were made by a contact aligner. The flow diagram of the experimental procedure is shown in figure 1. XRD and SEM analysis were used in order to identify the phase and the cross-sectional view of fabricated devices. Semiconductor device parameters were measured by a HP4156B. And the capacitance-voltage (C-V) characteristics was analyzed by a HP4275 LCR meter.

3. RESULTS AND DISCUSSION

Fig.2 shows XRD peaks of SBT thin films according to the annealing temperature in SBT/NO/Si-substrate structure. SBT phases of (105) and (110) of SBT films were shown clearly above 750°C. Above 800°C, a small peak appeared near 22 degree. However it was not shown to be a change of crystallinity as the annealing temperature increased up to 900°C. From this, SBT films are assumed to be crystallized well in the temperature range of 750°C to 900°C. Therefore the annealing temperature of 800°C was chosen for annealing SBT films.

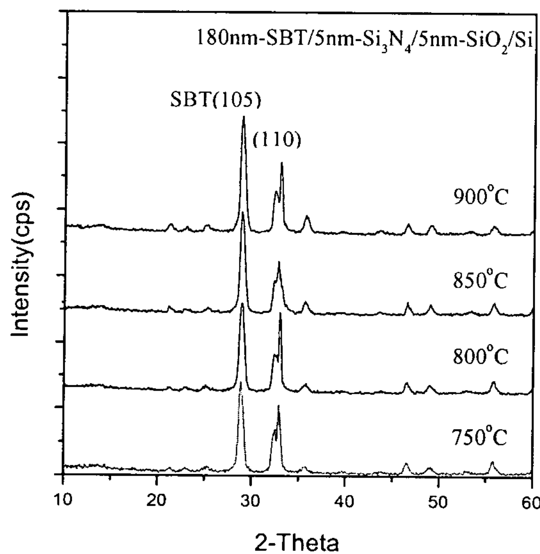

Fig. 2. XRD patterns of SBT films according to annealing temperatures.

Fig. 3 shows the 1MHz normalized C-V characteristics of metal-ferroelectric-insulator-semiconductor (MFIS) capacitor having the area of $9.6x10^{-4}$ cm^{-2}. The all C-V curves showed that the capacitance value varies from accumulation to inversion states. The thicknesses of Si_3N_4 and SiO_2 layer are 50 and 50Å. The memory window (width of the hysteresis loop) of C-V was about 2V for V_G sweep from -5 to +5V.

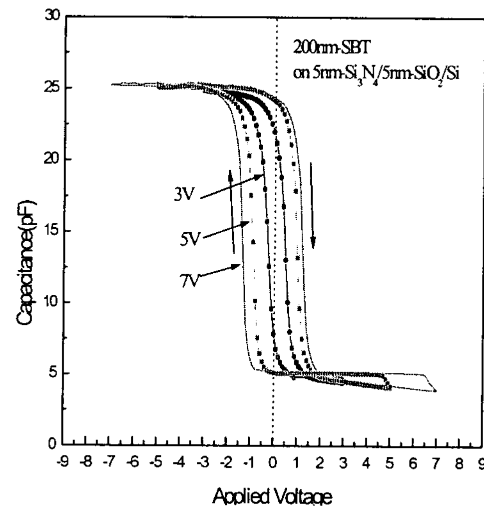

Fig. 3. 1MHz normalized (C-V) characteristics of MFIS capacitors.

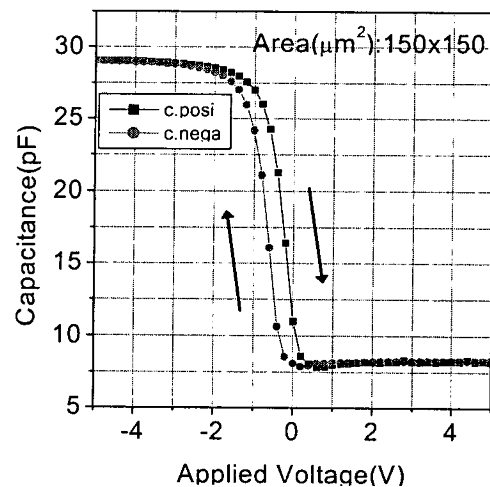

Fig. 4. 1MHz normalized (C-V) characteristics of MFIS capacitors.

Fig. 4 shows the C-V characteristics of MFIS capacitor

after ILD process. This C-V characteristics was for V_G sweep from −10 to +10V. Compared to the data of Fig.3, memory window is narrowed by more than 70% of 2V. This may be due to ILD process using SiH_4 gas. For compensating the loss of ferroelectricity, recovery annealing was made after ILD process.

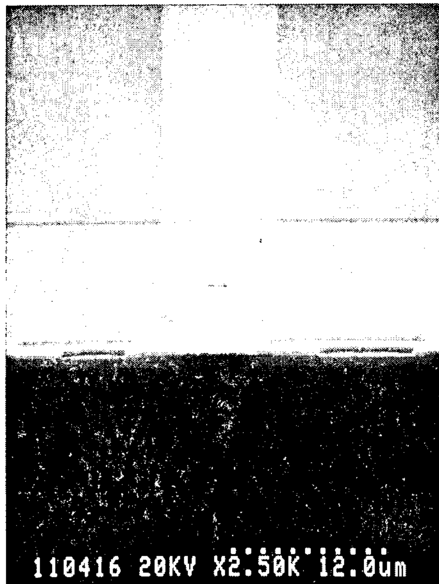

Fig. 5. Cross-sectional images of MFISFET stucture.

Fig. 5 shows the cross section of MFISFET (width/length of gate=16/4μm). Actually the gate length is 4μm even though the dimension of gate length is shown to be more than 4μm. This is due to the mixed methods of i-line lithography on the front-end process and back-end lithography process made by a contact aligner. Source and drain implant process was made by non-self alignment before the ferro-gate was formed.

Fig. 6 shows I_D-V_G characteristics of p-channel MFISFET having NO films of 50/50Å. In Fig. 6, a hysteresis loop was obtained with a counter-clockwise trace as indicated by the arrow by V_G sweeping −15 to +15V. This hysteresis loop was believed to be due to the ferroelectric nature of SBT films. Memory window was about 0.7V when the thickness of NO film is 50/50Å

Fig.7 shows I_D-V_D characteristics of p-channel MFISFET. We got I_{ON} and I_{OFF} data at the gate voltage of −2.5V after pulsing −15V on the gate. There was the difference between I_{ON} and I_{OFF} data by more than two times. It might be due to the ferroelectric properties of SBT films causing the induced charges on the p-channel electrically.

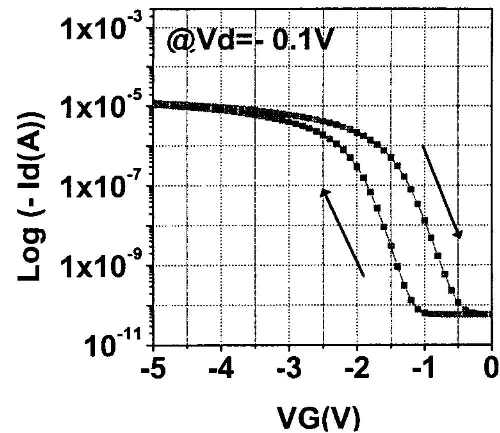

Fig. 6. I_D-V_G characteristics of p-channel MFISFET structure.

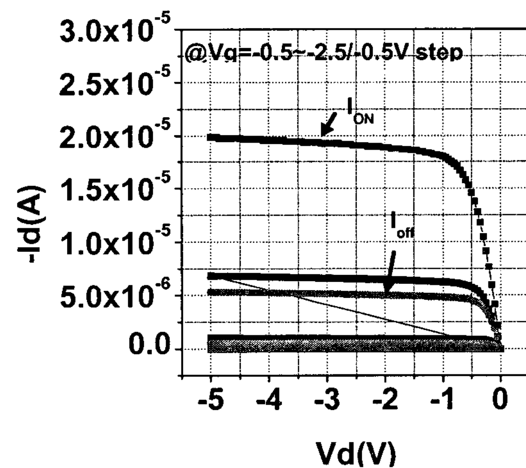

Fig. 7. I_D-V_D characteristics of p-channel MFISFET structure.

4. CONCLUSIONS

We fabricated the μm dimensional size-MFISFET using SBT ferroelectric materials successfully. And we acquired the compatibitiy of ferroelectric gate process with the 1.0 μm Si standard process.

To get a MFISFET device characteristics, we have to do recovery annealing after ILD process. The threshold

voltages of p-channel MFISFET are about −2.1V. And the memory window was about 0.7V, which was the value to be able to discriminate the difference between the I_{ON} and I_{OFF} for sensing margin.

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