Anneal Temperature Effects on Hydrogenated Thin Film Silicon for TFT Applications

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a-Si:H and poly-Si TFT (thin film transistor) characteristics were investigated using an inverted staggered type TFT. The TFT on as-grown a-Si:H exhibited a low field effect mobility, transconductance, and high gate threshold voltage. The poly-Si films were achieved by using an isothermal and RTA treatment for glow discharge deposited a-Si:H films. The a-Si:H films were crystallized at the various temperatures from 600℃ to 1000℃. As anneal temperature was elevated, the TFT exhibited increased g_m and reduced V_{ds}, V_T. The poly-Si grain boundary passivation with hydrogen increased the field effect mobility by 67 $cm^2/V{\cdot}s$. This paper investigates the grain boundary trap types and activation energies as a function of anneal temperature. The poly-Si TFT showed an improved I_{on}/I_{off} ratio of 10^6, reduced gate threshold voltage, and increased field effect mobility by three orders.

Keywords : a-Si:H, crystallization, poly-Si, thin film transistor (TFT), mobility

1. INTRODUCTION

Present a-Si:H thin film transistors (TFTs) are not fast enough to handle peripheral circuits of liquid crystal displays (LCDs) since the field effect mobility is low. On the other hand, the field effect mobility for poly-Si TFTs is sufficiently high to permit implementation of on-board logic circuits [1]. Presviously, crystallization of a-Si:H films on glass substrates was carried out with an anneal temperature below 600℃, over 10 h to avoid glass shrinkage [2, 3]. Previous study indicates that the crystallization is strongly influenced by anneal temperature and weakly affected by annealing duration time [4]. Conventional poly-Si films were achieved by either poly-Si film growth at high substrate temperature or high temperature annealing treatment after the thin film Si growth. Because the high temperature process and nonconducting substrate are required for poly-Si TFTs, the employed substrates have been limited by the following materials: quartz, sapphire, and oxidized Si wafer [5, 6].

We reported on poly-Si TFTs using high temperature anneal on a-Si:H/Mo structures. The metal Mo substrate was stable enough to allow 1000℃ anneal [7]. A novel TFT fabrication was achieved by using part of the Mo substrate as drain and source ohmic contact electrode. The as-grown a-Si:H TFT was compared to anneal treated poly-Si TFTs. Defect induced trap states of TFTs were examined using the thermally stimulated current (TSC) method. The poly-Si grain boundary traps were passivated by hydrogenation or fluorination because hydrogen or fluorine could compensate dangling bonds in the grain boundary [8, 9].

2. EXPERIMENT

The a-Si:H films were deposited onto 4"×8" Mo metal substrates by dc glow discharge decomposition of silane. Deposition temperature varied from 225 to 300℃ giving a deposition rate of around 0.5 ㎛/min. Prior to a-Si:H growth, a highly doped layer was deposited to achieve a good ohmic contact. Investigated sample structure was intrinsic a-Si:H/n^+ a-Si:H/Mo (i/n^+/Mo). The employed anneal techniques are anneal in nitrogen atmosphere, anneal in a vacuum, and RTA treatment. A novel TFT fabrication process was developed by usage of the Mo substrate as source and drain contact. The Si film side was bonded to a foreign substrate and source and drain were defined by chemically removing to Mo substrate, then the n^+ layer between source and drain was removed by isotropic Si etching. Inverted staggered type TFT output is strongly influenced by series resistance from source to channel and drain to channel. A film

thickness less than 0.5 μm was employed for the study. The investigated insulators were evaporated SiO, RF deposited SiO_2, RF magnetron sputter deposited amorphous $BaTiO_3$, Si_3N_4 and MgO. TFT output influencing factors were examined such as anneal temperature, gate dimension, Si film thickness, insulator thickness, and grain boundary passivation. Anneal temperature ranged from 200℃ to 1100℃ with an increasing step of 100℃. Gate length effect was studied by varing the gate length from 25 μm to 200 μm and fixing the gate width at 500 μm. The insulator thickness effect study was carried out with oxide thickness ranging from 50 nm to 1000 nm. The poly-Si grain boundary trap type was examined by thermally stimulated capacitance (TSCAP) and thermally stimulated current (TSC) measurements. The device was first cooled and then heated at a constant rate. Electron and hole traps were detected as the sample was heated. The poly-Si films formed by RTA 850℃, 2 min. were exposed to hydrogen grain boundary passivation. The investigated parameters of the grain boundary passivation were substrate temperature effect (275℃ ~400℃), hydrogen exposure time (10 min. ~7 h), and distance between electrode and substrate holder. Investigated TFT structure is illustrated in Fig. 1.

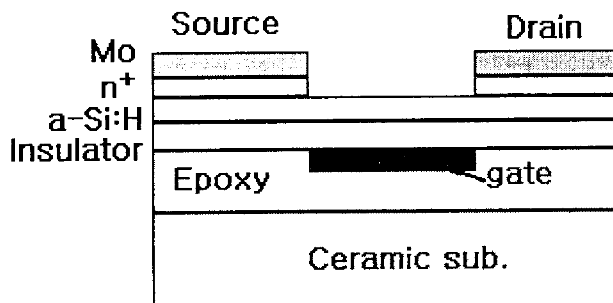

Fig. 1. Cross sectional view of the investigated TFT structure (Inverted staggered type TFT).

3. RESULTS AND DISCUSSION

To optimize gate insulator quality of TFT, a study was carried out on MIS capacitors. SiO and Si_3N_4 showed the existence of positive fixed charge and the effect of relatively high mobile charge. For RF sputter grown SiO_2, we observed negative fixed charge for high RF power (400 Watt) and positive fixed charge for low RF power (200 Watt). Fixed charges are compensated by the usage of double layers of SiO_2 doposited at low and high RF power.

The MIS capacitor high frequency and quasistatic C-V result on evaporated SiO with oxygen introduction showed a low interface density ranging from 10^{11} to 10^{12} $cm^{-2}eV^{-1}$ [10].

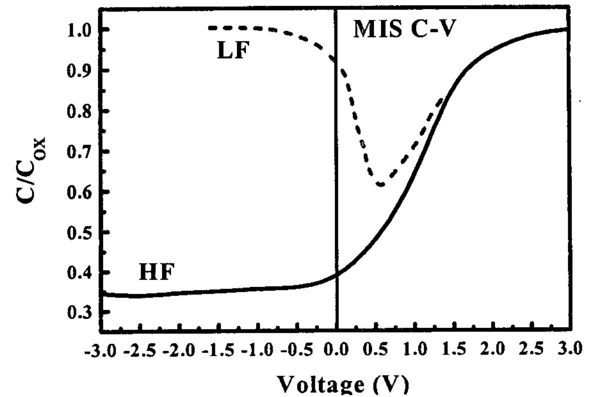

Fig. 2. C-V result on MIS capacitor for a low and high frequency measurements.

Figure 2 illustrates high frequency C-V result on MIS capacitor. I-V measurements of the MIM capacitor were performed to find capacitance per unit area and leakage current characteristics of the insulating layer. The thermally grown oxide capacitor exhibited the lowest leakage current and a high breakdown voltage. The second best was with double layer SiO_2 and the evaporated SiO in oxygen gas.

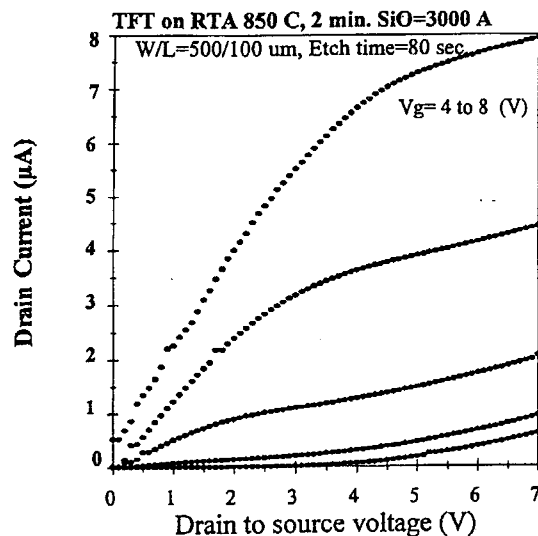

Fig. 3. The TFT I_d-V_{ds} characteristics on 0.3 μm thick poly Si.

The oxide thickness influences the gate threshold voltage (V_T) and capacitance per unit area (C/A) As oxide thickness increased, the V_T increased (V_T=1.5 V

for t_{SiO}=50 nm and V_T=10 V for t_{SiO}=800 nm) and the C/A was reduced. This indicates that manipulating oxide thickness can control the TFT switching voltage. As Si film thickness was reduced, the gate threshold voltage was reduced. The optimal Si film thickness for TFT application was 0.3 ㎛. Figure 3 shows the TFT output for a 0.3 ㎛ thick film with increased drain current and transconductance. As Si film thickness was less then 0.1 ㎛, TFT output degradation was observed. This may have come from Si film non-uniformity due to the Mo substrate surface conditions. The TFT on a 0.1 ㎛ thick Si film exhibited reduced drain current, reduced transconductance, reduced field effect mobility, and the drain current kink effect.

The TFT on as-grown a-Si:H exhibited a field effect mobility of 1.6×10^{-3} cm^2/V.s with and evaporated SiO gate insulator layer. The TFT on as-grown intrinsic a-Si:H shows a relatively high threshold voltage of 12 V and a low I_{on}/I_{off} ratio of about 10. TFT output characteristics after RTA 600℃ for 2 minutes exhibited well saturated drain current (I_d), improved trans-conductance, and reduced gate threshold voltage. A further improvement of TFT device performance was observed for high temperature (above 700℃) anneal of an intrinsic Si film which gave high ON current and low OFF current. The I_{on}/I_{off} ratio of 10^5 was achieved after RTA 850℃, 2 min.

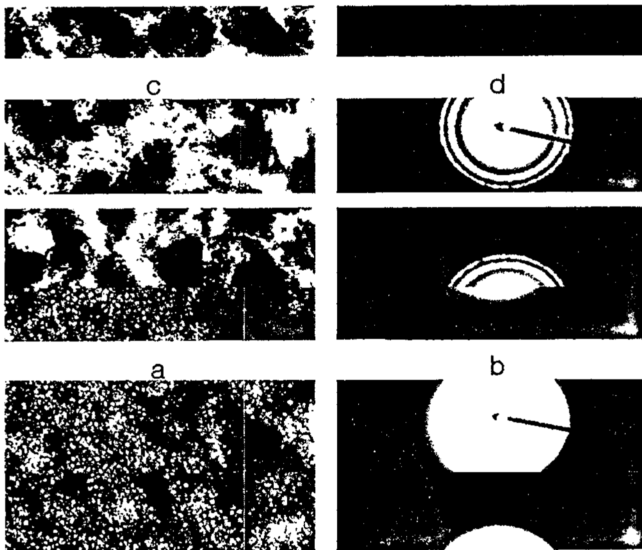

Fig. 4. Surface microstructural image and SAD pattern (a) bright field planar view of the as-grown a-Si:H (b) SAD pattern on the as-grown a-Si:H (c) bright field view of an 850℃, 4 h annealed sample (d) SAD pattern on intrinsic 850℃, 4 h annealed sample.

Figure 4 shows TEM surface microstructural image and the selected area diffraction (SAD) ring pattern of as-grown a-Si:H and annealed poly-Si film. Figure 4(a) shows an as-grown sample surface microstructure feature size of around 0.02 ㎛. The SDA ring pattern shown in Fig. 4 (b) indicated no crystalline component. A preferential etch was employed to reveal grain structure prior to the Si film thinning. Figure 4 (c) shows preferentially etched surface etch pits on an 850℃, 4 h anneal treated sample. Triangular type etch pits may indicate (111) orientation preferred crystallization. Because the etch pit sizes are around 0.5 ㎛, we interpret the grain size of poly-Si film can be larger than 0.5 ㎛. Figure 4 (d) shows the SAD diffraction patterns for an 850℃, 4 h annealed sample. The first diffraction ring indicates (111) orientation of the Si film. From these results, we confirm that post anneal treatment gave (111) preferred crystallization of thin film Si.

Table 1. Trap type and Activation Energy from TSC Study

Anneal (°C)	T_m (k)	Trap type	ΔE (eV)
As-grown	T_{m1}=345 T_{m2}=370	Hole Electron	0.45 0.49
600	T_{m1}=330 T_{m2}=370	Hole Electron	0.42 0.49
700	T_{m1}=170 T_{m2}=200 T_{m3}=225 T_{m4}=235 T_{m5}=370	Electron Hole Electron Electron Electron	0.18 0.22 0.25 0.27 0.49
850	T_{m1}=370	Hole	0.49
850, H^+ passivation 300°C, 4h	T_{m1}=370	Hole	0.49

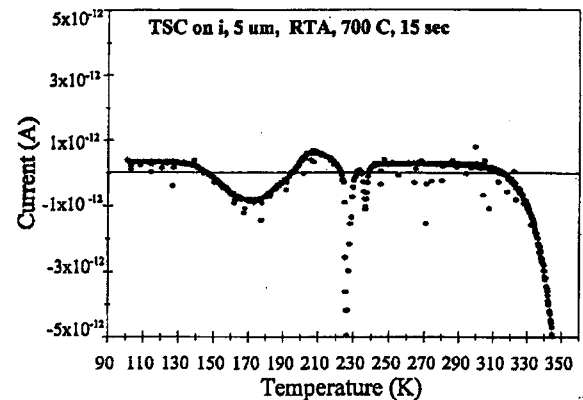

Fig. 5. TCS result of the thin film Si after RTA 700℃, 15 sec.

Table 1 shows only two different trap states (electron

or hole) for as grown a-Si:H films. We observed that the increased trap states with activation energy of 0.18 to 0.49 eV after RTA at 700℃. Hole trap states dominated after the anneal treatment higher than 850℃. Figure 5 shows the TCS results after RTA 700℃, 15 sec. Hydrogen grain boundary passivation was made on 850℃, 2 min. The RF plasma rehydrogenation was performed at 300℃. As hydrogen exposure time increased, mobility improvement was observed. The best exposure time for the RF plasma rehydrogenation was 6 hours at a substrate temperature of 300℃. The optimal distance between an electrode and a substrate holder using the RF plasma was 1/2 inch.

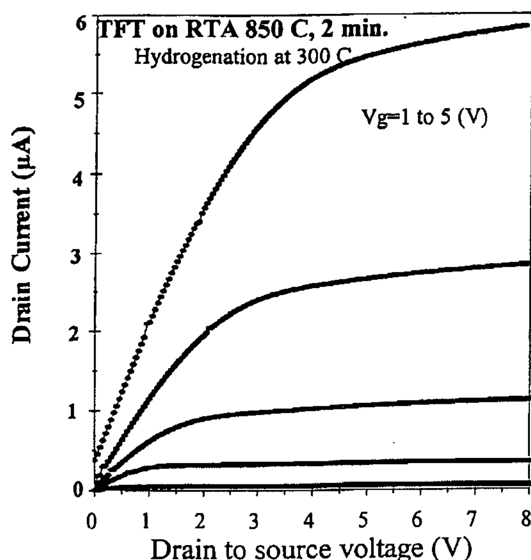

Fig. 6. The TFT I_d-V_{ds} characteristics on thin-film Si RTA 850°C, 2 min. annealed and RF plasma rehydrogenated at a substrate temperature of 300°C, 4 h.

An RF plasma rehydrogention at 300℃, 4 h improved the I_{on}/I_{off} ratio to 10^6. An increased drain current and transconductance contributed to improve field effect mobility after hydrogen grain boundary passivation (Fig. 6). Table 2 shows a summary of the anneal temperature effect on the TFT output characteristic parameters. As anneal temperature increased, the transconductance was increased and the drain voltage was reduced for TFT drain current saturation. The RF plasma hydrogen passivation on the poly-Si film improved the transconductance and field effect mobility. The field effect mobility was determined from the transconductance. Figure 7 shows a summary of change in mobility with anneal temperature. Mobility stays in the order of 10^{-3} cm²/V.s for anneal temperature below 600°C. An annealing temperature higher than 700°C gave 3 order improvement in field effect mobility. The inverter switching characteristics were strongly influenced by gate transfer characteristics (V_T), drain resistance (R_d), anneal temperature, and rehydrogenation treatment.

Table 2. A Summary of Anneal Temperature Effects for TFT.

	Temp (°C)	W/L (μm)	C/A (×10^{-8} F/cm)	V_{ds} (V)	g_m (moh)	μ_{FE} (cm²/V.s)
RTA	No heat	500 /114	1.2	25	1.6x10^{-9}	1.6x10^{-3}
	400	500 /200	1.3	15	18.3x10^{-9}	39.0x10^{-3}
	600	500 /200	1.2	6	7.0x10^{-9}	22.7x10^{-3}
	850	500 /200	1.9	6	2.0x10^{-6}	3.6
	H^+300	500 /200	1.9	5	4.5x10^{-6}	19.4
VAC	200	500 /200	1.6	12	7.0x10^{-10}	2.2x10^{-3}
	400	500 /200	1.9	8	1.1x10^{-9}	2.9x10^{-3}
	600	500 /200	1.9	4	3.0x10^{-10}	8.1x10^{-3}
	700	500 /200	1.9	5	9.0x10^{-6}	24.3

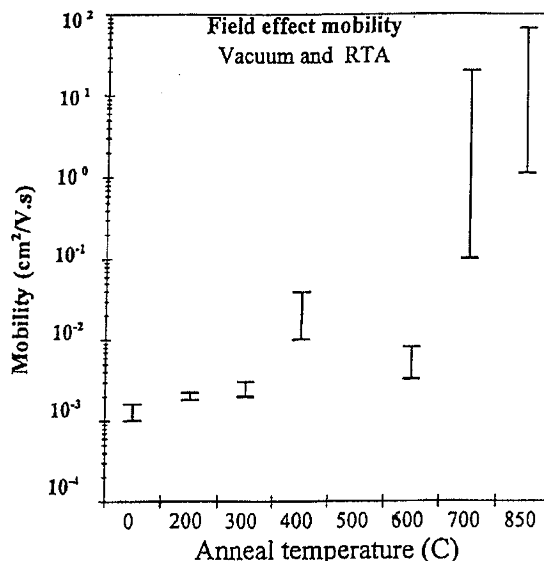

Fig. 7. The summary of field effect mobility as a function anneal temperature.

Inverter switching voltage was increased as oxide thickness increased. The poly-Si TFTs with oxide thickness below 250 nm can be readily operated for gate bias less than 5 V. Drain resistance R_d must be chosen less than TFT OFF resistance and larger than TFT ON resistance. Generally inverter's switching characteristics exhibited very sharp ON and OFF transitions for a high R_d and broad transition characteristics for a low R_d value. Rehydrogenation treatment reduced inverter switching voltage with the following conditions: high temperature annealing, reduced insulator thickness, and reduced gate

length.

4. CONCLUSIONS

A novel method of TFT fabrication was developed using the Mo substrate as drain and source contact, while removing other portion of the Mo. The Mo substrate was stable for high temperature processing and removable for TFT fabrication. We have shown TFT improvement after high temperature annealing treatments. The thermally grown oxide capacitor exhibited the lowest leakage current and the highest breakdown voltage. The second best was with double layer SiO_2 and the evaporated SiO in oxygen gas. The gate threshold voltage was increased as insulator thickness increased. The best working Si film thickness was 0.3 μm thick. As anneal temperature increased the TFT exhibited increased g_m and reduced V_{ds}, V_T. The high temperature annealed poly-Si TFT output characteristics were very stable against external light illumination. The field effect mobility was improved by three orders after high temperature anneal. The poly-Si grain boundary passivation with hydrogen increased the field effect mobility to as high as 67 $cm^2/V.s$. We showed grain boundary trap type and activation energy with anneal temperature. Hole type traps were the major defect type after 850°C anneal treatment and activation energy was given as 0.49 eV. The optimized conditions of the RF plasma rehydrogenation require a substrate temperature of 300℃, exposure time of 6 h and electrode distance of 1/2 inch spacing from the substrate holder.

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