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A Study of Jitter Reduction for SDH Transmission System using Sigma-Delta Modulation

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Abstract

The SDH (Synchronous Digital Hierarchy) has been rapidly acknowledged as a world wide transmission standard replacing the existing PDH infrastructure. A bit stuffing is used for synchronization between a PDH signal and a SDH node, and a pointer justification is used for synchronization between one SDH node and the other SDH node. During above processes - a bit stuffing and a pointer processing -, a stuffing jitter and a pointer jitter are produced and the generated jitter can cause transmission error.

In this study, a stuffing jitter and a pointer jitter are modeled and analyzed. A Sigma-Delta modulation is described and an advanced jitter reduction technique using a Sigma-Delta modulation technique in the Synchronizer, Pointer Processor and Desynchronizer is provided.

I. Introduction

The SDH offers an improvement in network flexibility supported by network management facilities. The intentionally synchronous operation simplifies the access to individual channels within the multiplexed signal. The synchronization of a PDH signals into SDH network is made by bit stuffing mechanism and these synchronized signals are multiplexed together in byte according to pre-defined procedure, which form STM (Synchronous Transfer Module) signal having a basic frequency 155.520 MHz and a frame rate 8 KHz.[1] The frequency offset and long-term phase deviation between one node and the other node in SDH network is absorbed by pointer justification in byte meaning. These digitized versions of the frequency offset are transmitted to the desynchronizer and distort the phase of a output PDH signal (jitter or wander) from the SDH gating node, while desynchronizing process. For the compatibility with the PDH network, the jitter generated in SDH network must be smoothed. So the output jitter at SDH gating node is limited and recommended by ITU-T.[2]

The bit stuffing jitter (mapping jitter) had analyzed by Duttweiler in 1972, and it has been proven that the bit stuffing jitter is mainly caused by a frame structure, called waiting time jitter.[3] From the nature of stuffing jitter, various reduction techniques have been proposed. The most prevailing one is, called a forced stuffing, making a stuffing ratio q/p , where p and q are mutually independent positive integer, instead of 0 or 1.[4]. A pointer justification results in large pointer jitter due to its low frequency and byte based stuffing structure. A bit leaking method - slicing the multi-bit phase jump into a single bit phase jump - has mainly discussed for pointer jitter reduction. Nowadays before deriving the phase lock loop (PLL) in the desynchronizer, phase modulation with dither signal is used .[5]

The existing jitter reduction methods need narrow

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bandwidth smoothing PLL in desynchronizer to meet the ITU-T jitter specification. Therefore the residual jitter in pass band of a PLL increases and is accumulated. [5] In this paper, well propose the new jitter reduction algorithm using a Sigma-Delta modulation technique and show the effectiveness of the proposed algorithm by simulation.

First, in section 2, the modeling and characterizing of a jitter (stuffing jitter and pointer jitter) generated in SDH network is presented. And In section 3, the Sigma-Delta modulation technique is reviewed and applied to synchronizer, pointer processor and desynchronizer for jitter reduction. The improved jitter performance by using a proposed algorithm is demonstrated by computer simulation in section 4. A conclusion is summarized in section 5.

Ⅱ. Jitter generation and its characterization in SDH equipment

2.1 Jitter generation

When a tributary signal , a PDH signal, with frequency fIN enters one node of SDH network with frequency fS1 , the difference of bit rates between PDH & SDH signal (fS1 - fIN) is accommodated by a bit stuffing process resulting in 1 bit phase jump.[5]

$$f_{NODE-1} \Rightarrow f_{S1} + (f_{IN} - f_{S1}) \Rightarrow f_{S1} + f_{STF} \quad (2.1)$$

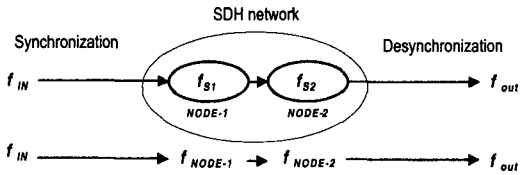

Fig. 2.1 frequency variation in the SDH network

SDH nodes are driven by local clock oscillators and these local clocks operate tracking mode (tracing to a reference source or STM-N input signals), holdover mode (tracing with a tracking history) or free running mode. According to the mode of operation, local clocks cause phase deviation in the holdover mode, and frequency deviation in the free running mode between the input and output signal of a SDH node. These phase and frequency offsets are accommodated by pointer processing (pointer adjustment) resulting in 8 bits or 24 bits phase jump.[5]

$$f_{NODE-1} \Rightarrow f_{S2} + (f_{S1} - f_{S2}) + (f_{IN} - f_{S1}) \Rightarrow f_{S2} + f_{PTR} + f_{STF} \quad (2.2)$$

These 1 bit or multi-bit phase jumps encoded in dedicated bits of STM frame are transported transparently within the SDH network and effect on the justification jitter at the SDH output interface port at the desynchronizer. For the reconstruction of a PDH signal from a terminating node of a SDH network, the desynchronizer uses phase locked loop (PLL) for smoothing the phase jumps due to bit stuffing and pointer processing.

$$f_{OUT} \Rightarrow LPF(f_{S2} + f_{PTR} + f_{STF}) \Rightarrow f_{IN} + f_{FLUCTUATION} \quad (2.3)$$

While smoothing a phase jump, the PLL in the desynchronizer inherently adds low frequency fluctuation, short-term or long-term phase variation, to the original PDH signal this fluctuation of a output PDH signal is called a payload jitter in SDH transmission system.

2.2 Jitter characterization

Figure 2.2 shows the block diagram of a conventional phase or frequency adaptation scheme (stuffing scheme) of a SDH equipment.

The stuff decision determines whether the justification opportunity bit in synchronizer (byte in

pointer processor) is to be occupied by a data bit(byte) or stuff bit(byte), and is derived from the buffer fill. Due to the integrating characteristic of an address counter, the buffer fill represents the phase difference between the input and output. The justification decisions are transmitted to the desynchronizer.

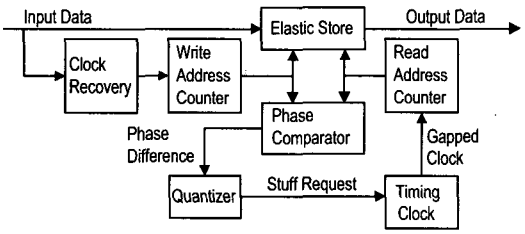

Fig. 2.2 Conventional stuffing scheme

For the analysis of a stuffing jitter, Fig. 2.2 can be modeled such as Fig. 2.3. The stuffing model shown in Fig. 2.3 operates at a sampling frequency equal to the frame repetition rate, and address counters are modeled by an integrator. The phase difference is obtained by subtracting the read phase from the write phase. The quantizer makes a stuffing request when phase difference exceeds a certain threshold.

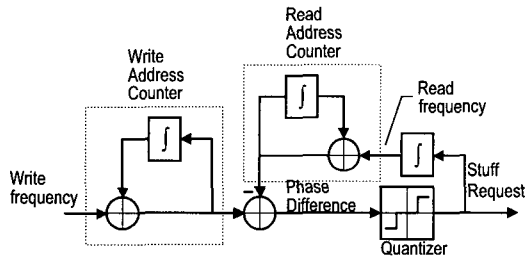

Fig. 2.3 Two input model of a stuffing scheme

After applying some trivial technique, Fig. 2.3 can be converted Fig. 2.4 shown as below.

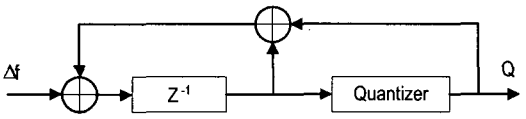

Fig. 2.4 Single input Model of a stuffing scheme

From the above model, we can say that the stuffing mechanism is a analogy of a 1 bit (byte) A/D converter with 1st order Sigma-Delta modulation - presented in section 3 - absorbing the frequency difference (f) between the input and output with a coarse quantizing step size. The phase smoothing PLL in the desynchronizer is simply modeled by a low-pass filter (LPF) performing a D/A conversion. So, the jitter generated in SDH transmission system can be characterized to a A/D-D/A conversion error of a frequency difference.

Ⅲ. Jitter reduction in SDH equipment

3.1 Sigma-Delta modulation

The 1 bit A/D conversion (Analog to Digital conversion) is a special version of the A/D conversion. It implies that the quantizing step size is not enough precise to describe the analog signal. So, many methods to reduce the quantization error in a 1 bit A/D conversion have been made and a Sigma-Delta modulation is one of those using a over-sampling technique.

The Fig. 3.1 shows a normal 1 bit A/D converter. And the Fig. 3.2 and the Fig. 3.3 show the 1st order and the 2nd order Sigma-Delta modulated converter, respectively.

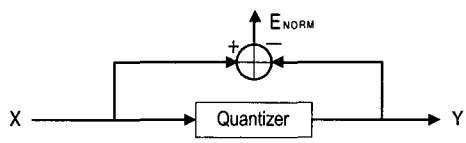

Fig. 3.1 Normal 1 bit A/D converter

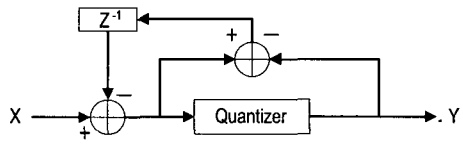

Fig. 3.2 1st order Sigma-Delta modulated converter

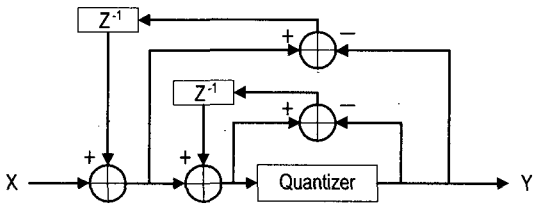

Fig. 3.3 2nd order Sigma-Delta modulated converter

Putting a ENORM is a quantization error, quantization error of the 1st order and the 2nd order Sigma-Delta modulated converter are given as below.

$$E_{NORM} = X - Y \tag{3.1}$$

$$E_{1ST} = (1 - Z\text{-}1)\, E_{NORM} \tag{3.2}$$

$$E_{2ND} = (1 - Z^{1})^{2}\, E_{NORM} \tag{3.3}$$

From the above equations, we can see that the quantization error of Sigma-Delta modulated converter has a high pass filtered form of that of a normal converter. For finding a realistic effect of a Sigma-Delta modulation, lets discuss the noise power spectral density letting a E_{NORM} be a white noise.

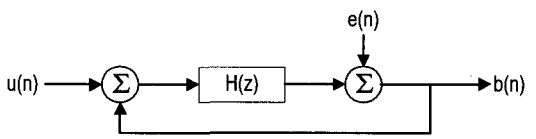

Fig. 3.4 Noise model of Sigma-Delta modulation

Fig. 3.4 is a linear model of a Fig 3.2 and 3.3, where u(n) is an input signal and e(n) is a noise signal. In Fig. 3.4, the signal transfer function (STF) is

$$W(z) = H(z) / 1 + H(z) \tag{3.4}$$

and the noise transfer function (NTF) is

$$T(z) = 1 / 1 + H(z) \tag{3.5}$$

Under the assumption that a u(n) and e(n) are mutually independent - uncorrelate -, the noise power spectral densities of the 1st order and the 2nd order Sigma-Delta modulated converter are given as below.[6]

$$R_{1ST\eta\eta}(z) = T_{1ST}(z) \cdot T_{1ST}(z^{-1}) \tag{3.6}$$

$$R_{2ND\eta\eta}(z) = T_{2ND}(z) \cdot T_{2ND}(z^{-1}) \tag{3.7}$$

Fig. 3.5 shows graphical feature of above equations where 1ST order noise transfer function, $T_{1ST}(z) = 1 - z^{-1}$ and 2ND order noise transfer function, $T_{2ND}(z) = (1 - z^{-1})^{2}$.

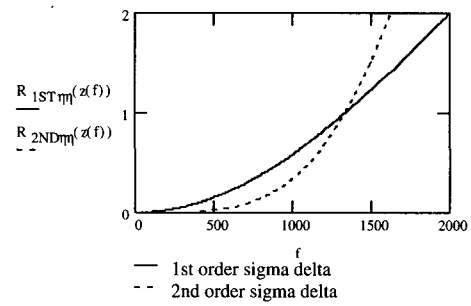

Fig. 3.5 Noise spectra of 1STand 2ND order Sigma-Delta modulation

We can see that the low frequency portion of a noise spectral density decreases and the high frequency portion of that increases. And it can be easily inferred that the quantization error of Sigma-Delta modulated converter is less than that of normal converter after D/A conversion (low pass filtering).

3.2 Jitter reduction using a Sigma-Delta modulation

A bit stuffing and a pointer processing are exactly same structures except step size (bit or byte). So, we can reduce the jitter replacing a normal quantizer by a Sigma-Delta modulated quantizer as shown Fig. 3.6 in

bit stuffing and pointer processing.

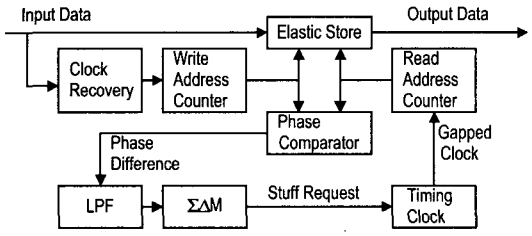

Fig. 3.6 Improved stuffing scheme with Sigma-Delta modulation

In the desynchronizer, a LPF is used for bit leaking to slice the multi-bit (byte base) phase jump for deriving a smoothing PLL. At this time, the output of a smoothing LPF is a sub bit resolution but we cannot derive a PLL of a sub bit resolution. So like stuffing process, it is needed to quantize the output of LPF. Of course, to reduce the quantization error, the Sigma-Delta modulated quantizer is also applied to this structure.

Ⅳ. Simulation

4.1 Bit stuffing jitter reduction

For the bit stuffing jitter (mapping jitter) reduction, the 2nd order Sigma-Delta modulated quantizer is applied to the synchronizer. E1 signal is selected for the testing PDH signal because the C12 (a container of E1) has stuffing ratio 0 or 1 which is the worst case resulting a large stuffing jitter. The simulation input and test condition are shown in Table 4.1.1.

For the jitter measurement, we simulate desynchronizer with a 2nd order PLL and test set with a high pass filter as below equation (4.1),(4.2).[2]

$$H_{PLL}(s)=\frac{\gamma\cdot s+\delta}{s^2+\gamma\cdot s+\delta} \quad \text{where} \quad \gamma=64,\ \delta=256 \qquad (4.1)$$

$$H_{HPF}(s)=\frac{s}{s+\omega_M} \quad \text{where} \quad \omega_M=2\cdot\pi\cdot 200 \qquad (4.2)$$

Table 4.1.1 Simulation input and test condition of a synchronizer

Nominal frequency of E1	$f_c=2048\cdot 10^3$
Sampling frequency for bit-stuffing	$f_s=2\cdot 10^3$
Tributary clock offset	$TO=1\cdot 10^{-6}$
Normalized frequency of tributary clock	$f_N=(1+TO)f_c/f_s$
Normalized frequency of path clock	$f_P=f_c/f_s$
Amplitude of jitter	$A=1$
Frequency of jitter	$f_j=0.25$
Input jitter	$\phi_J(t)=A\cdot\sin(2\cdot\pi\cdot f_J\cdot t)/2$

Fig 4.1.1 shows the simulation result of a proposed scheme comparing to conventional one.

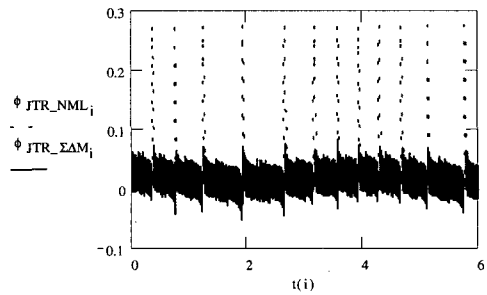

Fig. 4.1.1 Comparison of a bit stuffing jitter (peak-to-peak jitter)

4.2 Pointer jitter reduction

For the pointer jitter reduction, the 2nd order Sigma-Delta modulated quantizer is applied to not only the pointer processor but also LPF for bit leaking. E4 signal is selected for the testing PDH signal because the AU4 (administrative unit of VC4) stuffs 3 bytes (24 bits) at one time, which is the worst case resulting a

large pointer jitter. The simulation input and test condition are shown in Table 4.2.1.

Table 4.2.1 Simulation input and test condition of a pointer processor

Nominal frequency of VC4	$f_C = 150336\times10^3$
Sampling frequency for pointer-processing	$f_S = 8\times10^3$
Node-1 relative clock offset	$NO1 = 1\times10^{-6}$
Normalized frequency of node-1 clock	$f_{N1} = (1+NO1)\cdot f_C / f_S$
Normalized frequency of node-2 clock	$f_{N2} = f_C / f_S$

Fig.4.2.1 and Fig.4.2.2 show quantizing error waveform of pointer processor which means a phase difference between read clock and write clock phase in the 3 byte elastic store.

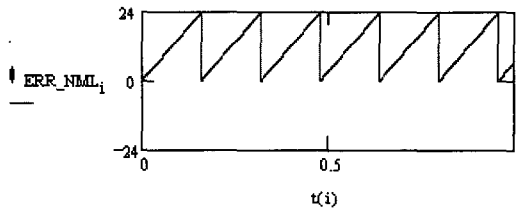

Fig. 4.2.1 Quantizing error of a conventional pointer processor

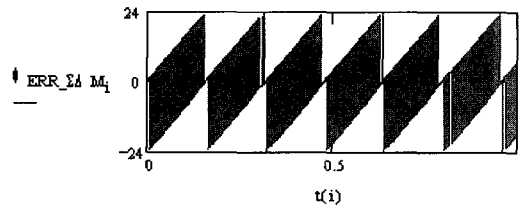

Fig. 4.2.2 Quantizing error of a proposed pointer processor

In the Fig.4.2.1, 24-bit phase difference occurred in the synchronizer and even if we use bit leaking method in the desynchronizer, a large amount of low frequency jitter remains. On the contrary, the phase difference on the proposed scheme can be eliminated by the low pass filter at the desynchronizer easily because its power spectra move to high frequency band.

Fig.4.2.3 shows the simulation result of proposed pointer processor compared to conventional one.

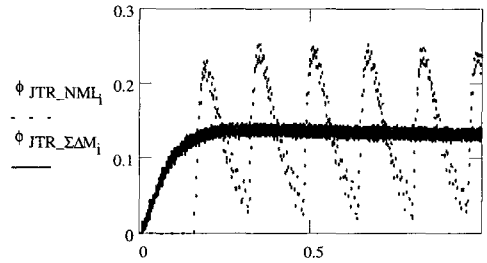

Fig. 4.2.3 Comparison of a pointer jitter (peak-to-peak jitter)

V. Conclusion

In this paper, the stuffing mechanism is modeled and its jitter generated in SDH equipment characterized to A/D-D/A conversion error. And also the advanced jitter reduction algorithm using a 2nd order Sigma Delta modulation is presented. The proposed algorithm can be applied to a synchronizer, a pointer processor and a LPF for bit leaking in the desynchronizer. As we see the simulation results, 0.2 UIp-p jitter can be reduced in the synchronizer and 0.1 UIp-p in the desynchronizer using Sigma-Delta modulation respectively.

For the best jitter reduction performance, of course, it is recommended that all parts of the SDH equipment adopt the proposed algorithm. The simulation results show the improved performance in jitter analysis during a SDH transmission of a PDH signal.

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