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VOID DEFECTS IN COBALT-DISILICIDE FOR LOGIC DEVICES

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Abstract

We employed cobalt-disilicide for high-speed logic devices. We prepared stable and low resistant $CoSi_2$ through typical fabrication process including wet cleaning and rapid thermal process (RTP). We sputtered 15nm thick cobalt on the wafer and performed RTP annealing 2 times to obtain 60nm thick $CoSi_2$. We observed spherical shape voids with diameter of 40nm in the surface and inside $CoSi_2$ layers. The voids resulted in taking over abnormal junction leakage current and contact resistance values. We report that the voids in $CoSi_2$ layers are resulted from surface pits during the ion implantation previous to deposit cobalt layer. Silicide reaction rate around pits was enhanced due to Gibbs-Thompson effects and the volume expansion of the silicidation of the flat active regime trapped dimples. We confirmed that keeping the buffer oxide layer during ion implantation and annealing the silicon surface after ion implantation were required to prevent void defects in $CoSi_2$ layers.

Key words : *$CoSi_2$, surface damage, void defects, salicide, ion implantation*

1. Introduction

We need to low resistive silicide for the interconnection and the gate to enhance the speed of the logic devices. Self-aligned silicide (salicide) process that forms the silicide only to gate, source and drain selectively has been employed in semiconductor device fabrication processes. Titanium disilicide ($TiSi_2$) and cobalt disilicide ($CoSi_2$) have been used as appropriate silicide materials for semiconductor devices. $TiSi_2$ has been employed frequently as the silicide materials of which sheet resistance is 12～14£ohm-cm. $TiSi_2$ has been reported that it shows abnormal sheet resistance values of 100 ohm/sq. below 0.3μm gate lengths. As the Si atoms are the major moving material during the $TiSi_2$ silicidation, it leads to agglomerate silicide at the edges of the gate and source/drain. The agglomeration of the silicide sometimes causes to short the gate and source or drain electrically, known as GSD short[1)~3)].

The $CoSi_2$ is promising to substitute $TiSi_2$ as it shows stable sheet resistance of 16～18 £ohm-cm even below gate length of 0.1um. Usually, the Co atoms move during silicidation, $CoSi_2$ is

more favorable to prevent GSD short in MOSFET devices. Employing $CoSi_2$ for the devices which have design rule of the minimum gate length sub-0.3㎛ is of importance to speed up the device performance by reducing the interconnect resistance. We fabricate $CoSi_2$ with typical logic device process and observed 40nm void defects. These defects worsen the contact resistance by 20% than that expected. We confirmed that those defects are from source and drain ion implantation damages. We suggest that defects may be removed by employing 5 nm-thick SiO_2 buffer layer on top of the active in ion implantation.

2. Experimental Procedure

Dual-gate CMOS transistors were fabricated 200㎜ epitaxial wafers as a starting material. After completing the PSLOCOS (poly spacer local oxidation of silicon) isolation, a high-energy phosphorous implant was performed to define N-well. Then, the threshold adjustment implants were performed. After the removal of sacrificial oxide layer, gate dielectric films with various thicknesses were fabricated in vertical furnaces. The 6nm-thick SiO_2 gate oxides were grown in dry oxygen with small addition of HCl. Then, the wafers with gate dielectrics were processed through poly silicon deposition in LPCVD. After poly silicon gate pattering followed by deposition of poly silicon gate, the shallow source and drain extensions (MDD) were implanted. After the sidewall spacers patterning, the poly silicon gate and source and drain regimes were heavily doped. The ion-implanted dopants were activated by RTA (rapid thermal annealing). The cobalt disilicide process was performed for the reduction of gate electrode and source and drain resistance. Cross-sectional and top views of silicide topography were observed with scanning electron microscope (SEM). $CoSi_2$ is confirmed with XRD rocking curves. After the deposition of insulating layer, metal contact photolithography and dry etching, tungsten plugging, and chemi-mechanical planarization (CMP), interconnection process with Al was performed. We measured contact resistance and junction leakage current[4].

3. Experimental results

We observed void defects at the surface and inside of $CoSi_2$ layer especially in the active area after salicide process. The SEM micro-images of cross sectional and top-view of the void defects are shown in Fig. 2. The density of the voids in active was 0.5 each/㎛^{2}. We also measured the junction leakage current in several wafers and showed the results in Fig. 3. The wafers with voids show more junction leakage current by 20% than that without defects. In addition, the junction leakage current distribution is broad in wafers with defects.

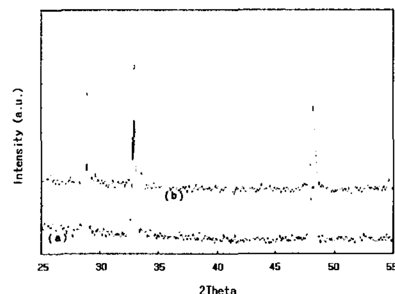

Fig. 1 XRD confirmation for $CoSi_2$ with (a) RTP 700 ℃ and (b) RTP 750 ℃

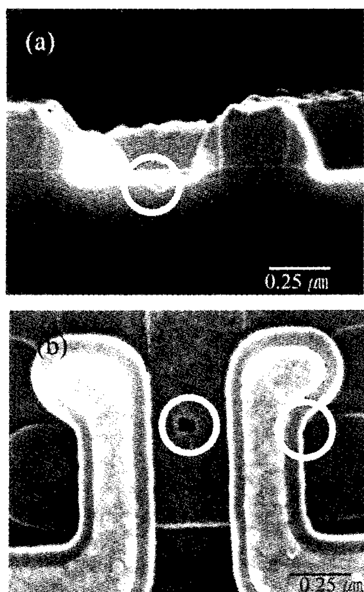

Fig. 2 The void defects in $CoSi_2$ (a) cross sectional view (b) top view

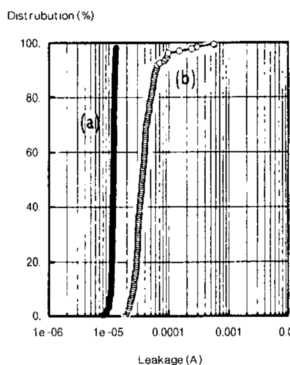

Fig. 3 Junction leakage current distribution plots for the $CoSi_2$
(a) without voids, (b) with voids

4. Discussion

We propose a model to explain the void defects as shown in Fig. 4.

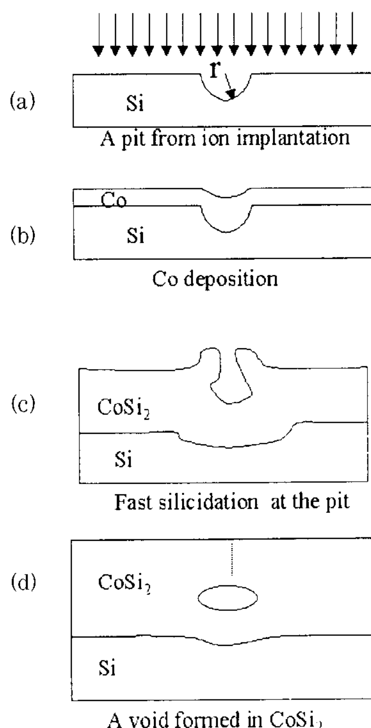

Fig. 4 A model for the void formation during silicidation

Active area of silicon is damaged during source-drain implantation and has a local pit (Fig. 4(a)). However, the silicidation flux around pits is fast due to the Gibbs-Thompson capillary effect[5]. As the Co is moving species during silicidation, it leads to enlarge the pits as shown in (b). After stable silicidation, 3.4 times volume expansion occurs, pits are surrounded by neighbor silicide as shown in (c). Finally trapped pits become void defects as in (d).

Based on above proposed model, we suggest to avoid void defects by removing surface damage during ion implantation process. We employed 5 nm-thick SiO_2 buffer layers during ion implantation and confirmed that no void defects are observed in active area.

5. Summary

It was possible to form void defects during the Co salicide process. Once void defects appears in active area of silicon devices, contact resistance and junction leakage current become large. The void defects are from surface damage in ion implantation process. We suggest that we avoid defects by protecting the active area surface using 5 nm-thick SiO_2 buffer layers.

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