Journal of Korean Institute of surface Engineering
Vol. 32, No. 3, Jun., 1999

THE RECENT TREND OF BUILD-UP PRINTED CIRCUIT BOARD TECHNOLOGIES

Kiyoshi Takagi

(TAKAGI Associates)

Abstract

The integration of the LSI has been greatly improved and the circuit patters on the LSI are becoming finer line and pitch. The high-density electronic packaging technology is improved. In order to realize the high-density packaging technology, the density of the circuit wiring of the printed circuit boards have also been more dense. The build-up process multilayer printed circuit board technology have a lot of vias, possibilities of the finer conductor wirings and have a freedom of capabilities of wiring design. The build-up process printed circuit boards have the wiring rules which are the pattern width: 100-20㎛, the via hole diameter: 100-50㎛. There three kinds of build-up processes as far materials and hole drilling. In this paper, the recent technology trends of the build-up printed circuit board technologies are described.

Key words : *Multilayer printed circuit board, Build-up process, Laser drilling, Semi-additive plating, Full-additive plating*

1. Introduction

Electronic products have been required to be more high functionality and highly processing speed. The integration of the LSI has been improved and the circuit patterns on the LSI are becoming finer line and pitch. In order to realize the high-density packaging technology, the density of the circuit wiring of the printed circuit boards, on which the electronics devices are mounted, have also been more dense. In this article, I would like to briefly explain the recent technology trend of the build-up printed circuit board technologies.

The build-up printed circuit board technology have a lot of vias, possibilities of the finer conductor wiring, and have a freedom of capabilities of wiring design.

With using the electroplating method, the plated-up method is one of the earliest one as the build-up process in 1967. After about 1990, the process called "copper polyimide", had been developed, which constructed by thin film technology using organic polyimide film on the ceramic substrate. The IBM's "SLC" board[1], which used the photosensitive dielectric materials, has

become for practical use of the build-up multi-layer printed circuit boards. The build-up multi-layer printed circuit boards have been rapidly developed since then in this industry.

The multi-chip modules have been developed by using these boards, on which the bare LSI chips have been mounted. The performances of the electronic products have become rapidly advanced, and now, it is developing to apply for LSI packages. The printede circuit boards by this technology will be more expanded hereafter.

2. The needs for the boards with finer pattern density [2]

The market needs of the electronic products with high performances has been unlimited today. The progress of the integration of SLI have brought the increasing of the number of the I/O pins of devices and increasing of the wiring density per unit area on the printed circuit boards. The mounted devices become small and are not only the QFP, TCP, but also the PGA, BGA, CSP with a lot of I/O pins.

Furthermore, the electric characteristics are important. The short distance wiring, the parallel wiring limitation, characteristic impedance control is required for these boards.

The build-up process multilayer printed circuit boards are highly suitable for the fine line and fine pitch technology. The wiring rules are,

The pattern width : 100-20μm,

The via hole diameter/the land diameter : 100-50μm/200-100μm,

The distance between the layers : 80-30μm,

The freedom of the via location.

On the build-up process technology can make small via holes, and also realize the finer patterns widths and finer pattern pitches.

3. The build-up process technology [2]

The build-up process is the following; a conductor layer and an insulated layer are built-up on the base substrates or on the layer that is already built-up. In the build-up process printed circuit boards, the functions about the device supporting part and the conductor wiring part are separate and this function is one of the features of the board.

In the blind-via technology, following dielectric materials and drilling methods are used;

1) using the photosensitive resin, and drilling holes photo lithographically

2) using the thermosetting resin, and drilling holes by laser

3) using the resin coated copper foil, and drilling holes by the laser using conformal mask of copper foil.

The comparison of these techniques is shown in the Fig. 1 In this figure, the relationship with the plating process is also shown.

3. 1 The photo lithographical method with photosensitive resin

The liquid or film type photosensitive dielectric materials are coated or laminated on the core boards, or on the layer already built-up. The process is shown in the Fig. 2. After the formation of the insulated materials, the boards are exposed by the UV rays through the mask

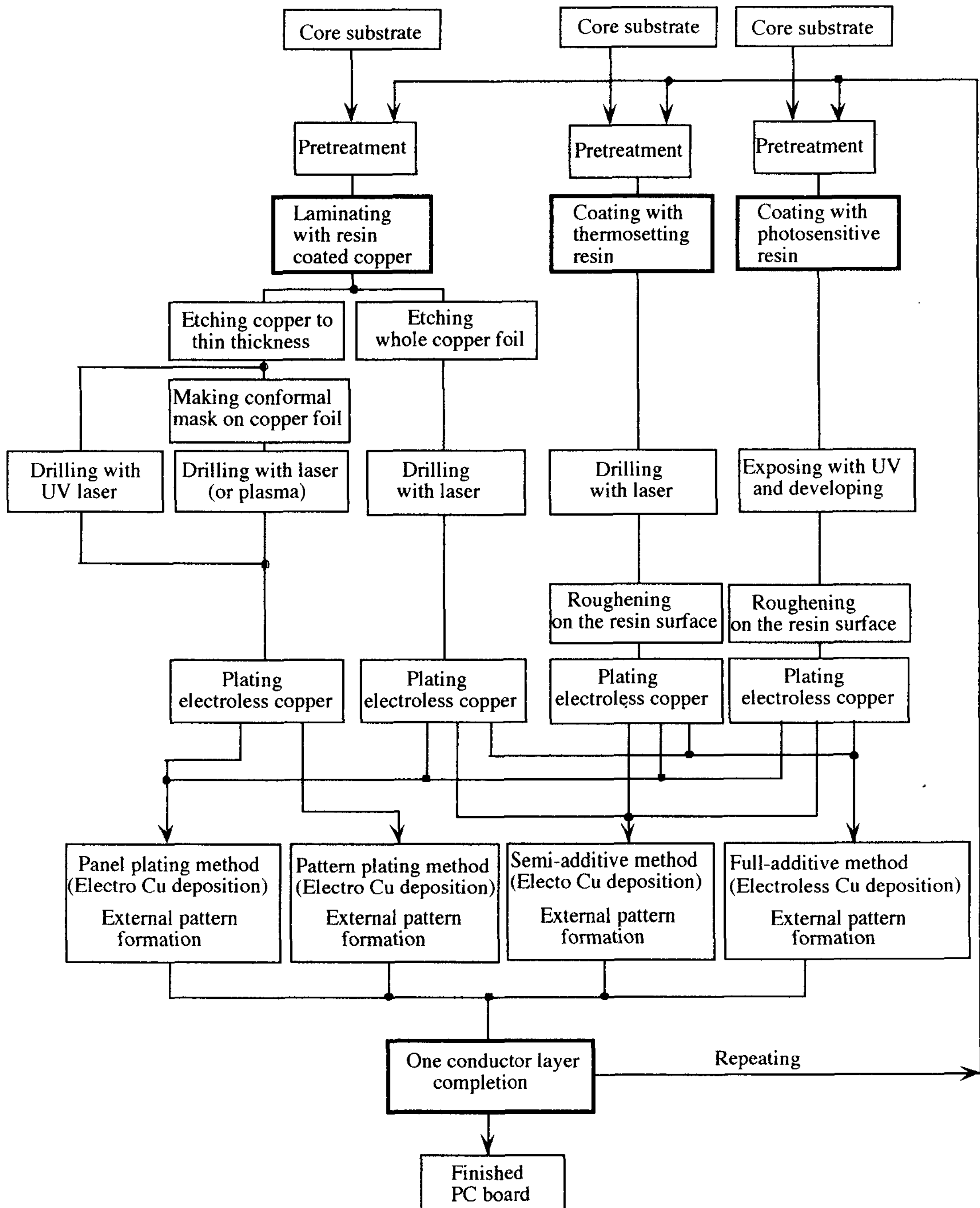

Fig. 1 Comparison on materials and microvia formation in sequential build-up process

and developed, then the via holes are formed in the dielectric layer. In order to promote adhesion of the electrodeposition, the surface of the dielectric materials is roughened, then the conduc-

tive layers formed by the electroless copper plating, followed the copper electrodeposition to required thickness sown in Fig. 2.

After the plating, the surface conductive patterns are formed by photo-etching technique. After that, the second dielectric layer is formed on the surface, and this process is repeated to build-up the conductive layers as shown in this figure. In the case of the photosensitive resin, the resin itself has unsatisfied property because the resin must be photosensitive. yet, the conventional manufacturing process can be applied to make the boards.

3. 2 The laser drilling method using thermosetting resin

In the case of using the thermosetting resin, the liquid or film type materials can be applied. After the formation of the dielectric layers, laser beam is scanned to make via holes. This process is corresponding to the UV exposure and developing in the Fig. 3. The other processes after drilling are the same in the Fig. 2.

When the thermosetting resin is used, the choices of the materials are basically widen,.

These two techniques (3-1 and 3-2) are the techniques that do not need the copper foils, and

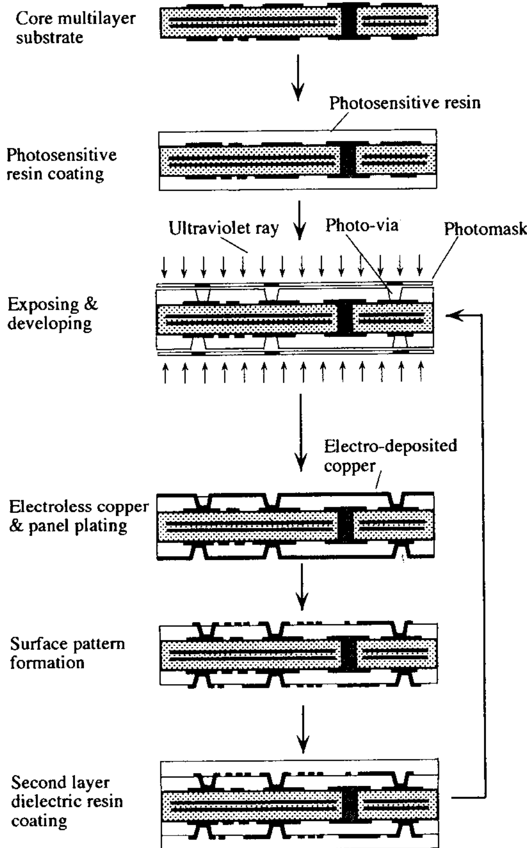

Fig. 2 Build-up process of photo-via and panel plating

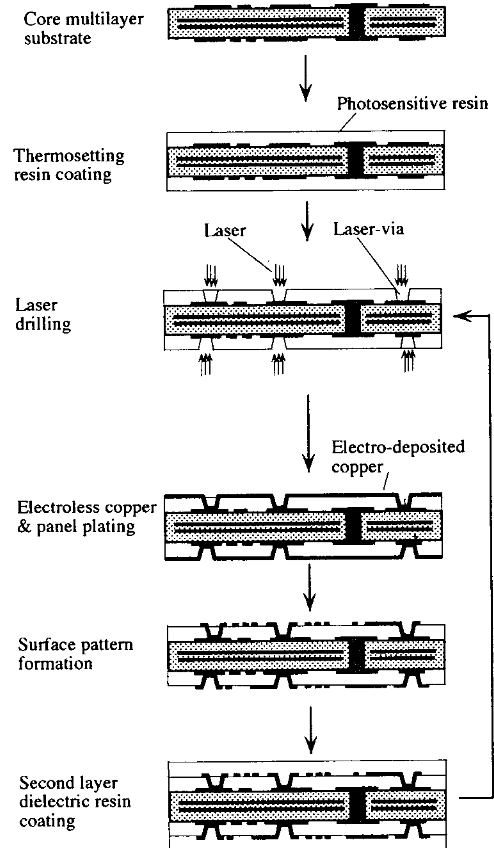

Fig. 3 Build-up process of laser-via and panel plating

use the electroless copper plating directly on the resin, following electro-depositing copper.

3. 3 The laser drilling method with resin coated copper foil

In these two cases above (3-1, 3-2), there are some limitations in terms of the plating adhesion. In order to improve the adhesion, the resin coated copper foil is applied. The process is shown in the Fig. 4.

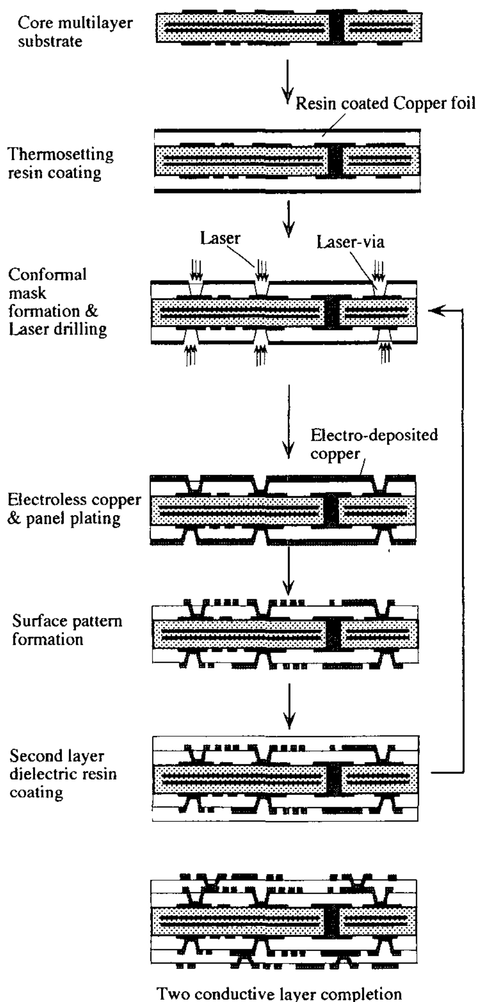

Fig. 4 Build-up process of laser-via and panel plating with coated copper foil

The resin coated copper foils is laminated by multilayer hot press or roll laminator, then, the conformal masks are formed on the copper foil by the photo etching for the laser drilling. After the plating process, it becomes difficult to form the conductive pattern with the etching process because the thickness of the conductive layer is the copper foil plus plating thickness. Before forming the conformal masks, making more thin copper foils is the first issue.

After the cleaning of the inside of the holes, the electroless copper plating and the electro-plating are processed. The patterning of the surface is the same above (3-1).

3. 4 The new pattern transfer technique.

The conductive patterns plated on the stainless steel made by the pattern plating method is transferred by the laminating press, and the holes are drilled by the laser, then, the interconnection is done with the plating method. By using this technique, it is possible to achieve more fine patterns by the pattern plating technique. Because the patterns are adhered with resin from three directions of the patterns, the peel strength becomes strong enough, and roughening process of resin is no longer needed. In addition, the flat surface can be obtained. Repetition of this process makes possible to increase the number of the layers.

4. The materials for the build-up printed circuit boards

The dielectric materials for build-up processes in the market are classified in three categories : the photosensitive resin, the thermosetting

resin, and the resin coated copper foils. The most of the dielectrics are epoxy resin, and the others are polyimide, PPE, BT, and so on. Almost all the resins have the properties of the heat-resistance and low dielectric constant. These materials may be adopted for the electronic equipment where requiring these properties. The materials are supplied with the liquid or the film type, and the copper foils coated with B stage of thermosetting resin. For the roughening on the resin surface, potassium permanganate is applied.

The features of the resin are the following : the peel strength of plated copper on theresin is about 0.8-1.5kN/m and glass transition temperature us 100-170℃. The dielectric constant of the resins is relatively low because they do not have the glass cloths. The resin coated copper foils shows high peel strength.

5. The plating process and the fine pattern formation

Having the fine lines and spaces are necessary for the build-up printed circuit board. To realize this, the relationship between the pattern formation and the plating technology is very important.

At present, the panel plating method has been the most major one in the plating techniques. The plating thickness with the panel plating process should be thin to achieve the fine line and space. The resistance to the stress on the corner of the via holes with thin plating thickness becomes low.

In the case of the resin coated copper foils, to achieve the sufficient thickness of the plating inside of the via holes, the thickness on the surface is the sum of the copper foil and the plating. It is difficult to make fine patterns by etching process, so the foil etching technique is usually applied, by etching out the copper foil to be very thin. For soldering the packaging with fine -pitched lead pins, accurate upper widths of patterns must be needed.

The pattern plating method which use the copper foil, the semi-additive technique after the making rough on the resin surface in the Fig. 5, and the full additive technique in the Fig. 6, can correspond to this subject. And the pattern transfer technique also meets this su

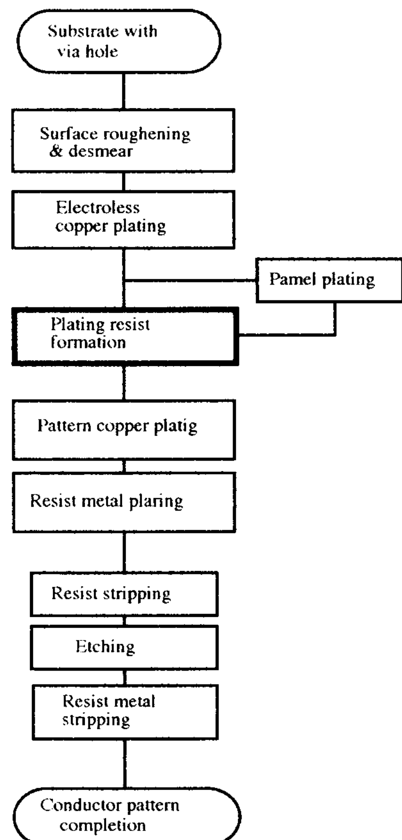

Fig. 5 Pattern formation with semi-additive plating

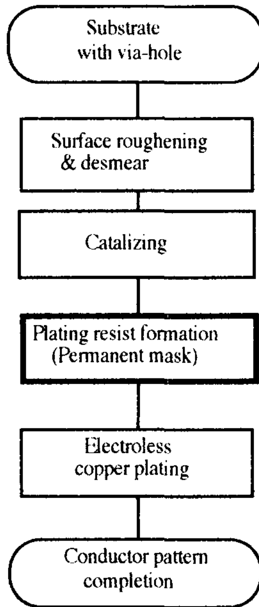

Fig. 6 Pattern formation full semi-additive plating

bject.

In the future, fine line patterns with less than 50㎛ are required for the build-up printed circuit boards. To make this, the clean manufacturing environment should be one of the most important factors. As the same as the pattern formation process is usually only cleaned, the other process shops, like plating process, are to be cleaned.

6. The reliability of the boards

The reliability of the build-up printed circuit boards are very important. There are basically two kinds of way of reliability test : thermal-shock test to check the interconnection, and the humidity test to check the dielectric insulation. Many kinds of the examinatiions for the build-up printed circuit boards are experienced, and show the boards highly reliable. The test results of microvias show also high reliability, which have already reported, for example, shown in the Table 1[3].

7. Application for packaging and MCM

The substrate of build-up printed circuit boards with fine line and fine pitch technology

Table. 1 Reliability of build-up multilayer PCB

Spesification of build up multiyayer board

Items	Specification
Materials	Build-up part : Photosensitive epoxy resin Core part : FR-4
Layer count	Build-up part:2+2=4 layer Core part:4 layer
Board thickness	0.75㎜
Dilectric thickness of build-up part	
Plating thickness	Build-up part:12㎛ Core part:35㎛
Line and space	50㎛/50㎛ Partially 40㎛/45㎛
Hole and land diameter of core part	ϕ200㎛/ϕ420㎛
Hole and land diameter of build-up part	ϕ100㎛/ϕ150㎛
Hole pitch	780㎛, 210㎛
Board size	50×50㎜

Result of reliability test

Items		Condition	Results
Continuity	Photo via	-65～125℃	1000cy OK
	Plated Through hole	-65～125℃	1000cy OK
Resistivity	Intralayer	60℃ 85% RH DC20V	1000cy OK
		120℃ 85% RH DC20V	50hrs OK
	Interlayer	60℃ 85% RH DC20V	1000cy OK
		120℃ 85% RH DC20V	50hrs OK
Peel strength		Peel angle 90°	700g/㎝

are widely applied for high-density packages such as ULSI mounting.

Multi-chip module is attractive for improving the functionality of electronic circuits. The substrate of the MCM is constructed of build-up multilayer printed circuit boards with fine line and fine pitch technology made from organic materials.

8. Summaries

In this article, I have described the recent technology trends of the sequential build-up multilayer printed circuit boards with the plating techniques, including process selection, status of material development, selection of via formation method, relationship between fine line productioin and plating, and reliability issues.

I believe that the requirement for higher density will inevitably expand the application of build-up process for printed circuit boards in future. These printed circuit boards are very valuable, and contribute to the high-dense packaging technology.

References

1. Y. Tsukada, S. Tsuchida, Y. Mashimoto : Proc. 7th IMC, p.252, June 3-5, 1992
2. K. Takagi : Electronic Technologies (Nikkan Kogyo Shimbun Ltd.), vol40, No.8, p.2, 1998
3. Y. Maeno, T. Kusagaya : Proc. 11th JIPC Annual Meeting, 17A-02, March, 1997