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Efficient Approach to Thermal Modeling for IC Packages

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효율적 수치해석기법을 이용한 반도체 패키지의 열방출 해석

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Abstract : An efficient method for thermal modeling of QFP is proposed. Thermal measurement data are given to verify the method. In parallel with the experiment, an exact full 3-D model calculation is also provided. One finds that there is an excellent agreement between validation data and the efficient model data.

1. Introduction

A rapid change has been seen in the power dissipation of electronic components for the last few years. In case of microprocessor, power dissipation ranges from a low end Pentium of 10W in 1995 to a high end Pentium of 40 W in 1999. Even memory devices have faced much more challenges to meet thermal requirements. A typical SRAM die for a PC in 1998 produces heat of 0.3 to 1 W max. Rambus memory die with operating speeds of more than 600 MHz, however, is expected to dissipate in excess of 2W. The higher the clock frequency becomes, the higher the power dissipation gets. However, the more heat that must be dissipated, the This cost will be manifested as more expensive thermally enhanced packages higherthe cost will be to the system. with larger fans, heatsinks and baffling, microchannels embedded in wafer itself optional.

In this context it becomes important to grasp and seek to enhance thermal performance of the packages in the packaging and assembly industry. In this study we propose a simplified model technique with which one could investigate thermal performance of MQFP(Metric Quad Flat Package) in a reasonably short time through simulation. Also the comparison with both experimental and exact 3-D model data will be given for validation.

2. Modeling Analysis

A typical type of package, MQFP, is chosen as a model example for convenience. The information on the package

geometry is given below in Table 1. Table 2 provides thermal conductivity of the materials used in the model.

Table 1. Package geometry

Lead count	208
Body size (LxWxT)	28 x 28 x 3.37 mm
Die size(LxWxT)	7.8 x 7.8 x 0.63 mm
Pad size(L x W)	9.5 x 9.5 mm
Board size(LxWxT)	100 x 100 x 1.59 mm
Board type	Multi-layer (1S2P)

Table 2. Thermal conductivities(℃/W)of the materials used.

EMC	0.83
D/A	2.5
L/F(pad)	170
L/F(lead)	85
Die	150
Test board(in-plane)	24.4
Test board(thickness)	0.38
Air	0.03

3. Simplified approach to the modeling

3.1. Lead

In reality, the leads are separated to each other as it should be. It would take a lot of time to model so many leads one by one in this case, 208 leads. This can be much simplified in such a way that the leads are modeled as a plane and its thermal conductivity is reduced by half the actual, instead. This is reasonable because the covered metal area is approximately half the total area.

3.2. Wire

There are 208 gold wires in this package through which heat conduction takes place. However, the effective cross sectional area of all wires is equivalent to less than 5 % of all leads, which means a very small contribution to heat dissipation. Also each wire's cross section area is of order of $10^{-3}mm^2$ of which effective thermal conductivity is so low that wires can be excluded in the model.

3.3. Pad to Lead Gap

Actually most contribution to heat dissipation in lead frame packages is made through the pad-to-lead path. So the pad-to-lead gap is the major factor in thermal modeling. In the lead frame design, inner leads are angled ("lead tip angle") considering bonding condition and mold flow. All the leads, however, are modeled to run in parallel with the pad edge for which compensation should be made up in terms of an effective gap length. The effective gap length can be determined by the harmonic average over the gaps between the pad and the leads. Or the algebraic average will work fine.

3.4. Heat Source

It is assumed that heat is uniformly generated on the die top surface. A GaAs chip has a highly localized hot point so that a caution should be needed in that case. The magnitude of input power is calculated by the formulae, power divided by die surface area. For example, if 1W power is applied to 10×10 mm die, then 1/100 = 0.01 W/mm^2.

3.5. Package to Board Heat Transfer

There is some clearance between the p ackage bottom and the board. This clearance filled with the air is meshed specifically and given the effective conductivity of k = 0.03 W/mK. The

contribution due to conduction only is considered.

3.6. Test Board

Test board used in this model consists of 3 metal layers : top signal, 2 copper planes embedded between FR4 layers. In most thermal calculations, it is convenient to treat such a layered structure as a homogenous material.

$$k_{through-thickness} = \frac{\sum_{i=1}^{N} t_i}{\sum_{i=1}^{N} \frac{t_i}{k_i}}$$

This means the board has orthotropic thermal properties, i.e., two different-thermal conductivities in the in-plane and through-thickness directions. These thermal conductivities are calculated by the following equations:

3.7. Heat Transfer Coefficient

It is well known that it is very difficult to define the exact value of the heat transfer coefficient in convection heat transfer problem because the value is quite dependant on the geometrical configuration, temperature of surface and fluid, and so on. In this study, the following equations are used to apply the averaged value of heat transfer coefficient to the all exposed top and bottom surface. These equations can be applied to the industry-standard wind tunnel environment. The radiation term is included in the total heat transfer coefficient (h_T).

h_{NC}[1] and h_{FC}[2] are area averages and h_{NC} assumes horizontal board orientation. The approximate value of h_T for natural convection is 15 W/m^2-K. At forced air velocities of 1.0 and 2.5 m/s h_T for forced convection will be about 35 and 55 W/m^2-K, respectively.

$$h_T = (h_{NC}^3 + h_{FC}^3)^{1/3} + h_{RAD}$$

$$h_{NC} = 1.31 \left(\frac{\Delta T}{W}\right)^{0.25}$$

$$h_{RAD} = \varepsilon\sigma \left(\frac{T_s^4 - T_a^4}{\Delta T}\right)$$

$$h_{FC} = 6.3 \left(\frac{V_{air}}{W}\right)^{0.62}$$

4. Thermal Test Procedure[3]

Thermal test die and calibration procedure[4,5]

Specially designed silicon die, called thermal test die, was used for the junction temperature measurement. There are resistors and diodes on the die top surface for heating and temperature sensing, respectively.

The diode is located on the center position of the die. Actually, the voltage difference of both sides of the diode is measured for T_j measurement. The die temperature is calculated by measuring the voltage of the diode, using an inverse relationship between the temperature and diode voltage.

Each package with thermal die

$$k_{in-plane} = \frac{\sum_{i=1}^{N} k_i t_i}{\sum_{i=1}^{N} t_i}$$

mounted is calibrated before testing. The packages are placed in a convection oven and connected to a 1.0 mA current

source. The oven was set to six temperatures ranging from 30℃ to 130℃ with 20℃ interval. The packages in

Table 3. Test board description

Substrate material	FR-4
Size (overall)	114 x 102 (mm)
Size (metallization)	99 x 99 (mm)
Thickness	1.6 (mm)
Signal layer	1
Internal Cu layer	2
Cu coverage (signal layer)	40%
Cu coverage (internal layer)	100%
Trace width	254+/-25 (μm)
Signal trace thickness	70+/-14 (μm)
Internal Cu layer thickness	35+/-3.5 (μm)

the oven are allowed to reach equilibrium at each temperature. Once equilibrium is reached, a four-wire measurement method is used to determine the diode forward voltage. Then the data are fitted by the following equation.

$$T_j = a \cdot V_{die} + b$$

where a is the slope and b the Y intercept.

Thermal test board

The test samples were mounted to the test board after bake process (24 hours at 125℃) using standard IR reflow procedure with a maximum ramp of 1.5℃/sec, at a maximum dwell preheat of 140 to 175℃ of 2 minutes, and a maximum dwell of 10 seconds at 210℃. The proposed specification of test board is described in Table3. The dimension of test board, especially the amount of copper, is very important because Θ-ja is largely influenced by the characteristics of the board. This is due to the fact that the board plays a role of external heat-fin for thermal dissipation.

Natural and forced convection test[6]

The natural and forced convection test was conducted in a closed loop wind tunnel with 12×12×24 inch (W×H×L) test section. The packages were placed in the middle part of test section in a horizontal orientation during the test. The ambient temperature was measured using a type-K thermocouple

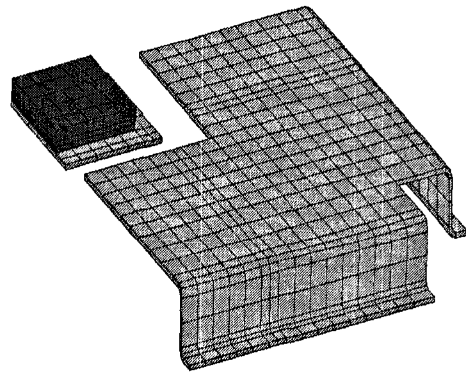

Fig. 1 Simplified model package inside

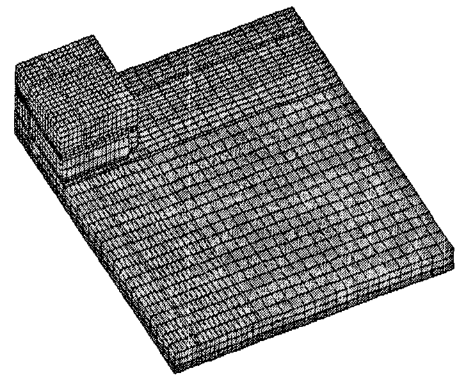

Fig. 2 Simplified model package test board

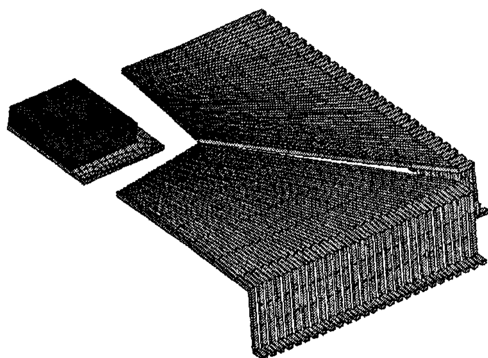

Fig. 3 Full 3-D model package inside

positioned apart from the test board with 1 inch distance from the side edge and the bottom wall, respectively. Three power levels (1, 2, and 3 watts) were positioned apart from the test board with 1 inch distance from the side edge and the bottom wall, respectively. Three power levels (1, 2, and 3 watts) were applied to the die for heating each at three air velocities (0, 1, and 2.5 m/s). The steady-state time was fixed as 15 minutes for the each power level and air velocity.

5. Results and Discussions

A finite element method (FEM) was applied to calculate the θ-ja. For this analysis a commercial software, ABA-QUS, was used. The boundary condition was assumed to be natural convection, and the power of 1 W was applied to the die. Fig. 1 shows a quarter of the model including lead, pad and die. A quarter model as a whole can be seen in Fig. 2. A quarter of the exact 3-D model is illustrated in Fig. 3.

Table 4 shows the comparison of the efficient model result with both experiment and full 3-D model.

Comparing test results with the present model data, one can see that the agreement lies within the error of 1 % max. In the case of the full 3-D model, the maximum error of 2.2 % can be obtained. One may raise a suspicion

Table 4. Comparisons of date from test pre sent model, and full 3-D model.

Air velocity (m/s)	θ-ja(℃/W)		
	Test	Model	
		Present	Full 3-D
0	30.9	31.22	31.53
1	27.4	27.46	27.79
2.5	25.3	25.52	25.86

that the exact model gives higher error than the simplified. Our proposed model already includes several approximations as mentioned in the above sections so that it would not be surprising to have the above result because the approximations may produce inherent error cancellation. In order to confirm this, we applied our model approach to other several packages of different size and lead count. And it turns out that the error ranges over 3 % to 9 %.

In summary, based on thermal measurement database, an efficient and universal model tool of MQFP is proposed. It can be applied to all kinds of MQFP packages. One can see good output within the error of 10 % max.

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