

FLIP CHIP ON ORGANIC BOARD TECHNOLOGY USING MODIFIED ANISOTROPIC CONDUCTIVE FILMS AND ELECTROLESS NICKEL/GOLD BUMP

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Abstract : Flip chip assembly directly on organic boards offers miniaturization of package size as well as reduction in interconnection distances resulting in a high performance and cost-competitive packaging method. This paper describes the investigation of alternative low cost flip-chip mounting processes using electroless Ni/Au bump and anisotropic conductive adhesives/films as an interconnection material on organic boards such as FR-4.

As bumps for flip chip, electroless Ni/Au plating was performed and characterized in mechanical and metallurgical point of view. Effect of annealing on Ni bump characteristics informed that the formation of crystalline nickel with Ni₃P precipitation above 300 °C causes an increase of hardness and an increase of the intrinsic stress resulting in a reliability limitation.

As an interconnection material, modified ACFs composed of nickel conductive fillers for electrical conductor and non-conductive inorganic fillers for modification of film properties such as coefficient of thermal expansion(CTE) and tensile strength were formulated for improved electrical and mechanical properties of ACF interconnection.

The thermal fatigue life of ACA/F flip chip on organic board limited by the thermal expansion mismatch between the chip and the board could be increased by a modified ACA/F. Three ACF materials with different CTE values were prepared and bonded between Si chip and FR-4 board for the thermal strain measurement using moire interferometry. The thermal strain of ACF interconnection layer induced by temperature excursion of 80 °C was decreased with decreasing CTEs of ACF materials.

1. INTRODUCTION

Flip chip assembly directly on organic boards offers miniaturization of package size as well as reduction of weight and interconnection distances resulting in high performance of electrical and thermal properties particularly in high frequency applications¹⁾. Therefore flip chip on organic board technology becomes a cost-competitive packaging method in the various industries, such as automobile, telecommunication, computers, appliances, and display. Especially flip chip technology becomes very important in mobile electronic products

such as cellular phones, pagers, PDA (personal digital assistant), video cameras, etc.

In case of non-solder flip chip interconnection technology, integrated circuit chips with bumps are faced down onto metallized substrate pads, and then anisotropic conductive adhesive/film is cured to interconnect chips to substrates.

For flip chip bump formation, electroless Ni plating is a potential candidate for cost reduction in bump formation because of selective autocatalytic metal deposition directly on the aluminum pads. Electroless Ni/Au bump process serves as one of

reliable, electrically stable interconnect between chips and substrates. General features of electroless Ni plated bumps are: (1) potential to be lowest cost bumping process because of easy process steps, however, (2) least consistent of all bumping processes because of electroless bumping uniformity, and (3) for high volume consumer & consumable markets. Electroless plated Ni bumps can be interconnected as bump itself by combining anisotropic conductive films (ACFs). ACFs are generally used for fine pitch interconnection methods for LCD applications^{2)~4)}. Connecting with ACF forms electrical and mechanical contact in which the connection resistance is higher than that of soldering and bonding temperature lower than those that result from soldering and much finer pitch conduction pads can be interconnected simultaneously using ACFs than solders. Conventional ACFs composed of an adhesive polymer matrix and fine conductive fillers using metallic particles or metal-coated polymer balls become important as a high density interconnection material. However, flip chip interconnection with conventional ACF has thermo-mechanical reliability limit induced by high CTE mismatch due to high CTE value of ACFs⁵⁾. Modified ACF composed of conductive fillers for electrical conductor and non-conductive fillers for modification of film properties such as CTE (Coefficient of thermal expansion) and tensile strength is necessary for improved reliability of ACF interconnection.

As the estimation for the reliability of flip chip interconnection, fatigue life of ACF interconnection which is limited by the thermal expansion mismatch between chip and substrate could be increased by modification of interconnection material. In general, the interconnection material between chip

and substrate should have close CTE value to those of chip and substrate for the reduction of thermally induced strain and stress.

Intensive research and development works have been carried out in the field of flip chip on board technology using ACF as an alternative of soldering^{6)~7)}. Few studies have been performed on the flip chip assembly on organic board by combination of ACF and Ni/Au bump as low cost alternatives. Understanding the effect of modification of ACFs on thermo-mechanical properties will impact on the better performance and reliability of flip chip packages by choosing right ACF materials and ACF materials development in the future.

This paper describes the mounting processes, material characterization and thermo-mechanical properties of flip-chip assembly using electroless Ni/Au bump and anisotropic conductive adhesives/films on organic board such as FR-4.

2. EXPERIMENT

2.1. Flip Chip Bumping

The electroless bumping process is wet-chemical and maskless⁸⁾. Test chips with 5 mm × 5 mm size and peripheral 48 I/Os were processed with an Al layer thickness of 1 μm and a passivation layer of 0.5 μm silicon nitride. The passivation openings of the bond pads are 75 μm and pad pitch is 150 μm. The processing steps are: (1) zincate treatment on Al I/O pad surface. Al surface should be activated to plate Ni because Ni is not electroless plated on Al surface. However, in this process Al is dissolved by the zincate solution. (2) Electroless Ni plating mushroom shape electroless Ni bumps with 20 μm height were formed in sodium hypophosphite

plating bath at 90 °C for 1 hour. (3)
Final gold flash with 0.05 μm thickness

resin in which conductive nickel particles with 5 μm in diameter and non-conductive inorganic particles with

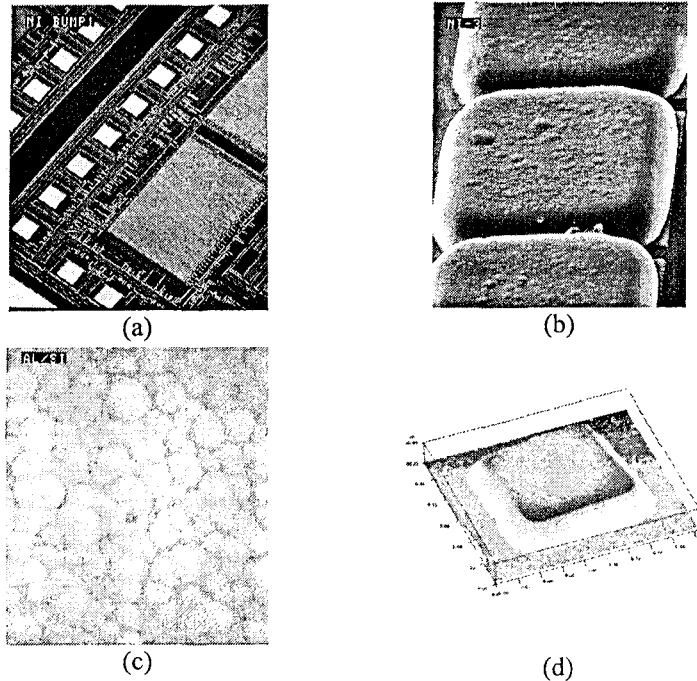


Fig. 1. Electroless Ni Bumps (a) unbumped Si chip, (b) Ni bumps, (c) surface morphology, and (d) configuration of Ni/Au bump.

was applied to the electroplated Ni surface for preventing oxidation. Fig. 1 shows Al pad in the test chip, electroless plated Ni bumps and surface morphology.

For the investigation of heat treatment effect, electroless plated Ni bumps were heat treated at 300°C in vacuum oven for 60 minutes.

Hardness measurement by nano-indenter and phase characterization by X-ray Reflection Diffractometry (XRD) were performed before and after heat treatment.

2.2. Modified ACF Material

ACF used in this study is 20~30 μm in thickness and made of insulative

less than 5 μm in diameter dispersed. Surface modification of particles is necessary before particles mixing with base resin. In a typical procedure⁹⁾, silica (40g) were mixed with a solution containing *g*-glycidoxy propyltri methoxy silane (2.0g), ethanol (95 mL), and distilled water (5 mL). The white suspension was ultrasonicated for 5 min and then stirred at 70 °C for 1 hour. The surface modified powders were collected by centrifugation followed by washing with ethanol (120 mL) and then dried under vacuum. Adhesive resins prepared by mixing epoxy resin, curing agents, silylated silica powders and Ni powders were converted to a dry film format for easy handling. The

Table 1. The Bonding Parameters for ACF Flip Chip Assembly

| Pre-bonding | |
|---|-----|
| Temperature(°C) | 80 |
| Pressure(kgf/cm ²) | 0.5 |
| Time (s) | 5 |
| Final bonding of FPC to glass substrate | |
| Temperature | 150 |
| Pressure(kgf/cm ²) | 3 |
| Time (s) | 300 |

content of non-conductive inorganic particles was varied from 0 to 50 wt% ACF.

The CTE values of the cured modified ACFs were measured by TMA (Thermo

Mechanical Analyzer). The specimen for TMA test was cured and cut into strips mm. After placing a specimen in the with dimensions of about 0.1×5×40 TMA instrument, heat was applied from room temperature to about 250 °C at a rate of 5 °C/min.

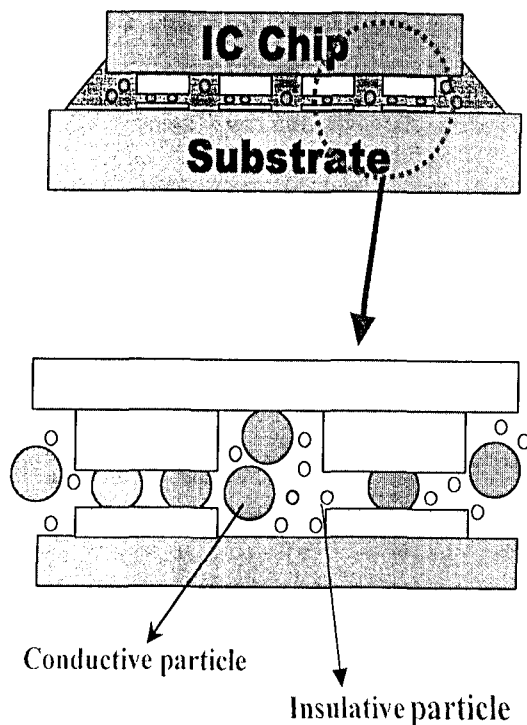


Fig. 2. Schematic of cross-section of flip chip interconnection with Ni/Au bump and modified ACF.

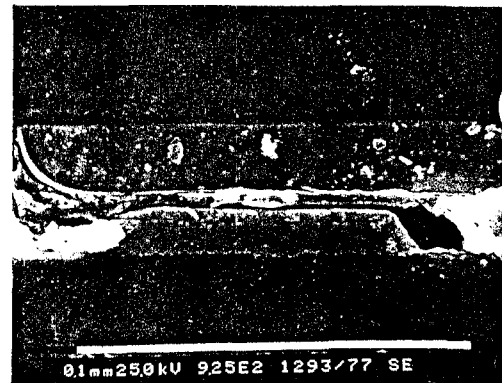


Fig. 3. SEM cross-section of the ACF flip chip interconnection with Ni/Au bump.

2.3. Flip Chip Assembly

Modified ACFs were cut into a correct size to cover the bonding area and were first pre-bonded to organic FR-4 board using light pressure and at the same time applying heat (80 °C, 0.5 kgf/cm² for 5 seconds). After the pre-bonding the carrier film was removed. Then chip was aligned and final bonded to the organic FR-4 board substrate using Fineplacer. The bonding parameters of pre-bonding and final bonding are shown in Table 1.

The schematics of cross-section of flip chip assembly using modified ACF shown in figure 2 indicate that electrical conduction paths are constructed by mechanical contacts between conductive particles, bump and pad, and non-conductive particles do

not contribute to electrical conduction and affect the adhesive property such as CTE and tensile strength. For electrical evaluation of ACF flip chip interconnection, connection resistances were measured by four-point probe method. After bonding, the cross-section of bonded area was observed by a scanning electron microscopy (SEM).

2.4. Thermal Strain Measurement

Thermal deformations that result from mismatches of coefficient of thermal expansion (CTE) in the ACF flip chip assembly were investigated by moire interferometry. The thermal loading that caused the measured deformation was applied by cooling the specimen from an elevated temperature T_1 to room temperature T_2 . The grating was placed on the specimen while the specimen was

held at T_1 , and the measurements were conducted at T_2 . Thus, the deformations of the specimen grating reflect the deformations experienced by the specimen under thermal loading ΔT ($\Delta T = T_2 - T_1$) = 80 °C.

The moire interferometry system was designed to obtain U (x-direction) and V (y-direction) displacement fields of the specimen. Thermal strains in the ACF flip chip assembly were determined from both the displacement fields.

Table 2 shows the CTE values of components in the ACF flip chip assemblies.

3. RESULTS AND DISCUSSION

3.1. Effect of Heat Treatment on Ni Bump

For the Ni/Au bumps, average of bump height is 20 mm and bump height uniformity is 1 mm for 48 bumps per test chip. The hardness of 2.56 GPa measured by nano-indenter was achieved. Thereafter hardness was increased to 4.55 GPa after heat treatment without structural deformation. It is the result of phase transformation in the electroless deposited Ni bump that can be explained by X-ray diffraction analysis. The amorphous structure of as-deposited Ni bump is shown in the figure 4 (a), and crystallization of amorphous Ni and precipitation Ni_3P

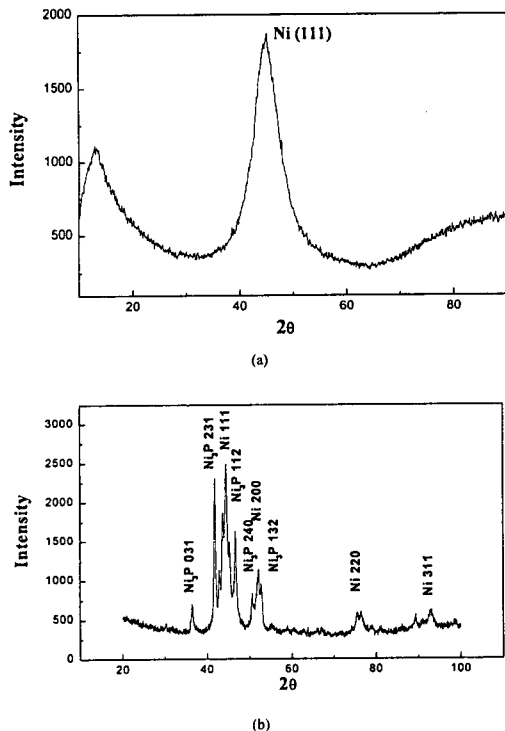


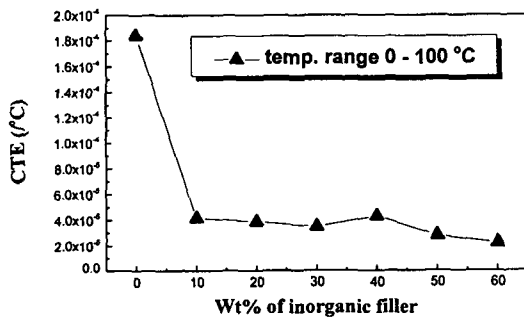
Fig. 4. X-ray diffraction pattern of the electroless Ni bump (a) before and (b) after heat treatment.

Table 2. The Bonding Parameter for ACF Flip Chip Assembly

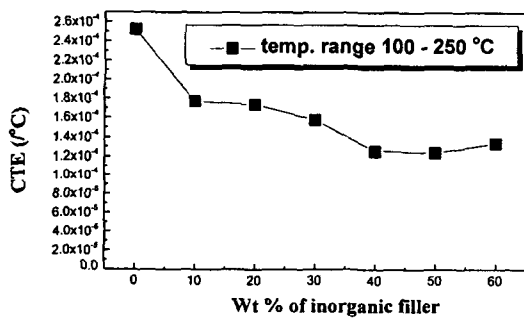
| Component | CTE(ppm/°C) |
|---------------------------|-------------|
| Si chip | 3.5 |
| FR-4 board | 18 |
| ACF of 10 wt% filler cont | 42.9 |
| ACF of 30 wt% filler cont | 35.2 |
| ACF of 50 wt% filler cont | 28.0 |

phase after heat treatment are shown in the figure 4 (b). It is believed that the formation of crystalline nickel with Ni₃P precipitation causes an intrinsic stress increase resulting in the hardness increase, which can be a source of reliability limitation.

Effect of heat treatment on the Effect of heat treatment on the electroless deposited Ni film characteristics indicated that, although the Ni₃P precipitates formation above 300°C caused an increase of hardness, there was no tremendous change of bump characteristics.



(a)



(b)

Fig. 5. CTE of cured ACF materials done on a TMA (Thermo-Mechanical Analyzer) as a function of wt% inorganic filler content (a) below T_g and (b) above T_g which is 109.5°C measured by DSC (Dynamic Scanning Calorimeter).

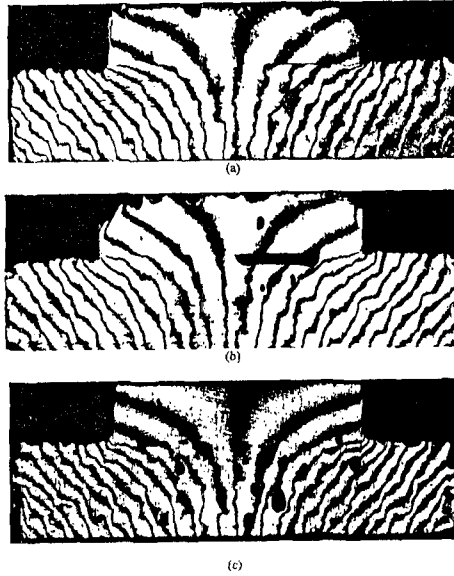


Fig. 6. Moire fringe patterns of horizontal x direction displacement (U displacement field) for flip chip assembly specimens with adhesive layer of (a) 10wt%, (b) 30wt%, and (c) 50wt% filler content under an isothermal loading DT=80°C (Reference temperature = 102°C)

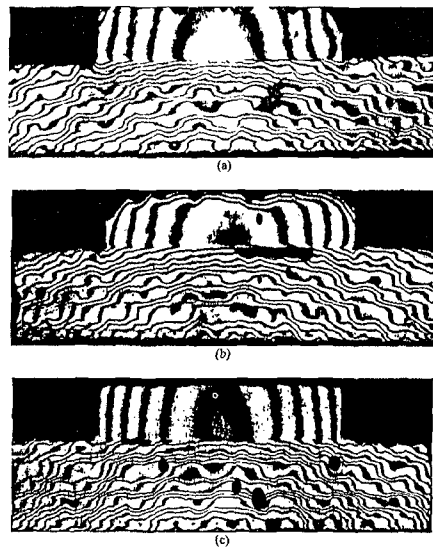


Fig. 7. Moire fringe patterns of vertical y direction displacement (V displacement field) for flip chip assembly specimens with adhesive layer of (a) 10 wt%, (b) 30 wt%, and (c) 50 wt% filler content under an isothermal loading dt = 80°C (Reference temperature = 102°C)

3.2. Effect of Filler Content on CTE of ACF Material

varied with filler content. It is desirable that the CTE of the interconnection material should be as closely matched as possible with those of the components to be bonded. Fig. 5 shows with increasing amount of inorganic particles for the below and above glass transition temperature of epoxy resin.

It is recommended that the adhesive layer should have CTE value of 22~27 ppm/°C range for the acceptable thermal fatigue property due to thermal mismatches of flip chip assembly¹⁰⁾. Below T_g, filler content of 50~60 wt% is necessary for the recommended requirement. The addition of conductive filler over certain limit in conventional ACF materials makes their electrical property from anisotropic to isotropic.

Therefore, non-conductive particles up to certain amount are added to adjust CTE value of adhesive layer for the reliability concerns.

Above T_g, CTE value of matrix epoxy resin is high and decreases slightly with addition of inorganic fillers.

3.3. Effect of CTE of Adhesive Layer on Thermal Strain of Adhesive Flip Chip Assembly

In this section, we discuss the thermal deformations of the ACF flip chip assembly structure and the resulting thermal strains in the adhesive layers as a function of CTE value of the adhesive layer. The thermal fatigue life of ACF flip chip on organic boards limited by the thermal expansion mismatch between the chip and the board could be increased by the incorporation of modified ACF.

Figure 6 and 7 show fringe patterns of U and V displacement fields from ACF flip chip assembly specimen with

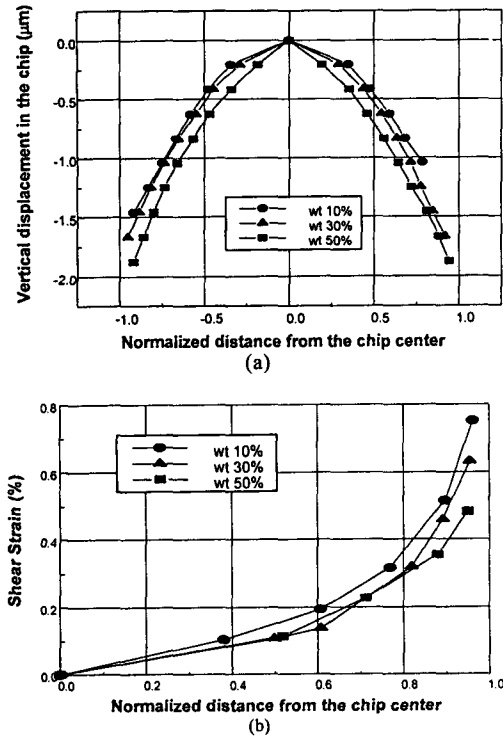


Fig. 8. (a) Chip warpage and (b) Thermal shear strain of ACF interconnection layer.

different CTE values of adhesive layer. After the assembly was cooled by 80 °C, all of the components contracted in both the x and y directions. The deformations in the Si chip are very small as indicated by the low fringe density, because the material has low CTE and high Young's modulus. In the FR-4 board, the y direction contraction is much greater than the x-direction shown by the higher fringe gradient in the V field fringe pattern.

In the x-direction, the CTE mismatch resulted in different displacements in the chip and the board. Their relative displacements at any point are a function of the distance from the center of the flip chip assembly to that point, and CTE of adhesive layer. At the ends of the assembly, the relative

displacement reaches its maximum value which shows the highest strain and stress. The increase in fringe density in the adhesive layer between the chip and the board with distance from the center is observed in the figure 6 for three adhesive of different CTE value.

The strains of adhesive layer induced by thermal loading can be determined from the discontinuities of fringe pattern between the chip and the board¹¹⁾. Through the use of the U field fringe pattern as shown in figure 6, the relative displacement in the x direction between the chip and the board was determined. The resulting shear strains in the adhesive layers were also calculated as shown in figure 8(b).

The difference in the three shear strain curves is the result of the CTE difference of adhesive layers that exist between the chip and the board. Thermal strain of ACF interconnection layer induced by temperature excursion of 80 °C is decreased with decreasing CTE of ACF layer. It is obvious that if the CTE value of the adhesive layer is relatively low resulting in high Young's modulus, the strain of the adhesive layer is low due to the more rigid mechanical constraints between the chip and the board.

Figure 7 shows fringe patterns of V displacement field in the chip and the board showing vertical displacement in the chip increase as a function of distance from the chip center as shown in figure 8 (a). Regardless of CTE value of adhesive layer, vertical displacements are almost same.

5. CONCLUSION

We have discussed the flip chip assembly on organic board using ACF and electroless Ni/Au bump. As a low

cost bumping process, electroless Ni bumps were formed and characterized. A very good uniformity of bumps has been obtained and the electrical property from connection resistance measurement of flip chip assembly was excellent. In the case of using Ni/Au bumps for cost effect flip chip assembly, heat treatment above 300 °C for longer than 1 hour should be avoid because hardness and internal stress increase in the bumps due to Ni₃P precipitation may be a potential of interconnection failure.

For the improvement of reliability of ACF flip chip assembly, conventional ACF was modified by incorporating non-conductive particles. As the content of non-conductive particles increases, CTE value of cured adhesive film decreases without variation of electrical conductivity as an interconnection material in the flip chip assembly.

Modified ACFs of different CTE value have been interconnected between Si chip and FR-4 board. The modified ACFs with incorporation of nonconductive particles can be successful interconnection materials without degradation of electrical conductivity. Moire interferometry was used to evaluate the thermal strain induced by CTE mismatches as a function of CTE value of adhesive layer. The results show that low CTE adhesive layer with high filler content has low shear strain induced by CTE mismatch between the chip and the board under temperature difference. Further investigation on the thermo-mechanical property of adhesive jointed flip chip assembly as a function of CTE value of adhesive layer is necessary to find out the optimal design for higher reliability. In summary, flip chip assembly techniques using the combination of chemical Ni/Au bumping and modified ACFs are successfully demonstrated and very cost effective.

References

1. Dernevik, M. et al., Electrically Conductive Adhesives at Microwave Frequencies, Proc. 48th Electronic Components and Technology Conference, 1026-1030 (1998)
2. Asai, S. et al., Development of an Anisotropic Conductive Adhesive Film (ACAF) from Epoxy Resins. Journal of Applied Polymer Science, 56, 769-777 (1995)
3. Date, H. et al., Anisotropic Conductive Adhesive for Fine Pitch Interconnections. Proc., International Symposiums on Microelectronics '94, 570-575 (1994)
4. Torri, A., Takizawa, M., and Sasahara, K., Development of Flip Chip Bonding Technology using Anisotropic Conductive Film. Proc., 9th International Microelectronics Conference, 324-327 (1996)
5. Yim, M. J., and Paik, K. W., The Contact Resistance and Reliability of Anisotropic Conductive Film (ACF). IEEE Transaction on Component, Packaging, Manufacturing and Technology, to be published, May, (1999)
6. Kulojarvi, K., Savolainen, P., and Kivilahti, J., Bonding Flexible Circuits and Bare Chips with Anisotropic Electrically Conductive and Non-conductive Adhesives. 10th European Microelectronics Conference, 28-34 (1995)
7. Williams, D. J. et al, Anisotropic Conductive Adhesives for Electronic Interconnection. Soldering & Surface Mount Technology, 4~8 (1993)
8. Kloeser, J. et al., Fine Pitch Stencil Printing of Sn/Pb and Lead Free Solders for Flip Chip Technology. IEEE Transaction on Component, Packaging, Manufacturing and Technology, C 21, 41-50 (1998)
9. Liang, S., Chong, S. R., and Giannelis, E.P., Barium Titanate/Epoxy Composite Dielectric Materials for Integrated Thin Film Capacitors. Proc. 48th Electronic Components and Technology Conference. 171-175 (1998)
10. Suryanarayana, D., Wu, T. Y., and Varcoe, J. A., Encapsulants used in Flip Chip Packages. Proc. 43th Electronic Components and Technology Conference, 193-198 (1993)
11. Guo, Y. et al., Solder Ball Connect Assemblies under Thermal Loading: I. Deformation Measurement via Moire Interferometry, and Its Interpretation. IBM Journal of Research and Development, 37(5), 635-647 (1993)