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대용량 IGBT를 위한 새로운 능동 게이트 구동회로

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A New Active Gate Drive Circuit for High Power IGBTs

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요 약

대용량 IGBT를 위한 새로운 능동 게이트 구동회로를 제안한다. IGBT의 우수한 스위칭 성능을 성취하기 위해 필요한 여러 구동 조건들을 최적으로 조합시킨 게이트 구동 회로이다. 스위칭 노이즈와 스트레스를 감소시키기 위해 필요한 느린 구동 조건과 스위칭 속도를 증가시키고 손실을 저감시키기 위해 요구되는 고속 구동 조건들을 동시에 만족시키고 있다. 또한 작은 전류의 턴-온시 발생되는 진동현상을 효과적으로 감쇠시킬 수 있는 특성을 지니고 있다.

ABSTRACT

This paper deals with an active gate drive (AGD) technology for high power IGBTs. It is based on an optimal combination of several requirements necessary for good switching performance under hard switching conditions. The scheme specifically combines together the slow drive requirements for low noise and switching stress and the fast drive requirements for high speed switching and low switching energy loss. The gate drive can also effectively dampen oscillations during low current turn-on transient in the IGBT. This paper looks at the conflicting requirements of the conventional gate drive circuit design and the experimental results show that the proposed three-stage active gate drive technique can be an effective solution.

Key Words: Gate resistor, active gate drive, gate drive circuit, IGBT switching transient

1. Introduction

Recently the applications of IGBTs has expanded widely, particularly in the area of high power converters. The gate drive circuit in the power converter is the interface between the IGBT power switches and the logic level signals in the modulator. The gate drive circuit design can be optimized to achieve the best performance that can be obtained from the power semiconductor device. The gate drive should switch the IGBT at a high speed while limiting di/dt and dv/dt and associated noise generated during the switching transient. The simultaneous requirement to minimize switching losses, the peak reverse recovery current stress during turn-on and the peak over-voltage stress at turn-off makes gate drive design a challenging task. The IGBT gate drive circuits have conventionally employed fixed gate resistors. The resistor is selected so as to obtain acceptable level of switching electro-magnetic interference (EMI), and to limit the reverse recovery current at turn-on, and the over-voltage at turn-off with minimal energy loss. These conflicting requirements results in sub-optimal performance of such a conventional gate drive (CGD) unit. To satisfy the switching stress constraint and the EMI standard, the value of the gate resistor required would have to be

large. This compromise leads to long switching delays and higher switching losses while merely being able to achieve acceptable noise levels and switching stresses.

The values of the turn-on and turn-off gate resistors have, in the past, been optimized and their effects studied in [1] and [2] with an aim to limit the turn-on di/dt and the turn-off over-voltage and dv/dt. Also, [3] has investigated methods that utilize multiple gate resistors to control the over-voltage during turn-off switching transient at over-current levels. This study, however, is only for turn-off operation and it is difficult to obtain optimized switching characteristics between the over-voltage and the turn-off energy loss at nominal current levels. The IGBT has been used in the active region at turn-off by using a closed loop high speed operational amplifier in the gate circuit.[4] In this case, the turn-off dv/dt can be precisely controlled according to the reference voltage command. The problem with this method is the large switching loss at turn-off, and the circuit cannot be easily extended to turn-on operation under inductive load switching transient. A technique for reducing the power loss at turn-on by injecting additional current into the gate has been investigated in.[5] This method used a phase-locked-loop to determine the instant of current injection into the gate of the device, which can result in poor operation under transient load current conditions. Also, the update of the control information occurs with one switching period delay and the total turn-on delay time is still quite large because a fixed gate resistor has been used to limit the di/dt during turn-on. Reference[6] has described a high performance current source gate drive used in a modular traction converter. Also,[7] has reported on the use of a high performance gate drive for high power IGBT converter applications. It is based on open loop methods for reduced turn-on di/dt operation, with pre-determined control points. Turn-off is controlled by using closed loop measurement of the collector voltage. This information is used to limit the over-voltages for the series-connected IGBTs.

In this paper, a three-stage AGD technique is presented for driving high power IGBTs. The purpose of the proposed AGD is to obtain optimized switching performance for both turn-on and turn-off operation and for all operating conditions, which has the following characteristics:

- Reduced delay time at both turn-on and turn-off;
- Reduced turn-on di/dt and the associated reverse recovery effects;
- Lower tail voltage and the resultant energy loss at turn-on;
- Controlled over-voltage at turn-off;
- Reduced energy loss due to improved dv/dt characteristics at turn-off;
- Reduced total switching time at both turn-on and turn-off.

2. The Proposed Three-Stage AGD

The typical collector and gate voltages and current waveforms at turn-on and turn-off with a CGD are sketched in Fig. 1. The turn-on characteristics show the delay time before the rising of the collector current, the reverse recovery transient at the end of the current rise, and the tail voltage at the end of the voltage fall. During turn-off, Fig. 1(b) shows the delay time before the collector voltage rise, the over-voltage during the collector current fall, and the tail phenomena at the end of the collector current fall. Detailed explanation of the switching transient in the IGBT is available in.[2],[8~10] This paper divides the typical switching waveform into three regions in order to obtain different control purposes based on the successive stages of the switching transient as shown in Fig. 1(a) and (b) respectively. So we call it a three-stage AGD technique.

The timing requirement for the three-stage control is illustrated in Fig. 2. The power circuit topology considered is the hard-switched voltage source inverter leg shown in Fig. 3. At turn-on, stage-I immediately follows the main command. This stage is designed to minimize the delay time by rapidly charging the IGBT gate with a large gate current. Once the gate voltage has reached the threshold voltage level of the device, the second stage of operation is initiated. During this stage, control of the turn-on di/dt is achieved by a reduced rate of charging of the IGBT gate. This can be achieved because the turn-on behavior of the IGBT is similar to a MOSFET, which allows the collector current to be controlled based on the gate voltage. Stage-II continues until the collector current reaches the

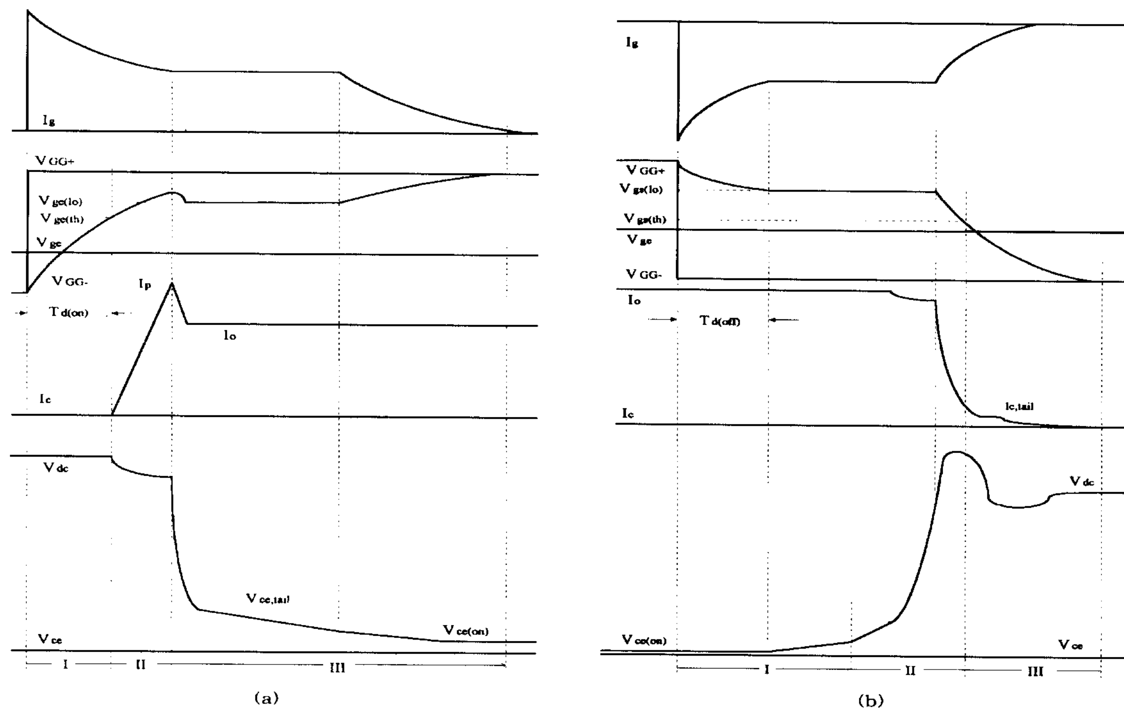

Fig. 1 Sketches of (a) turn-on and (b) turn-off waveforms of an IGBT under inductive load switching with a CGD circuit

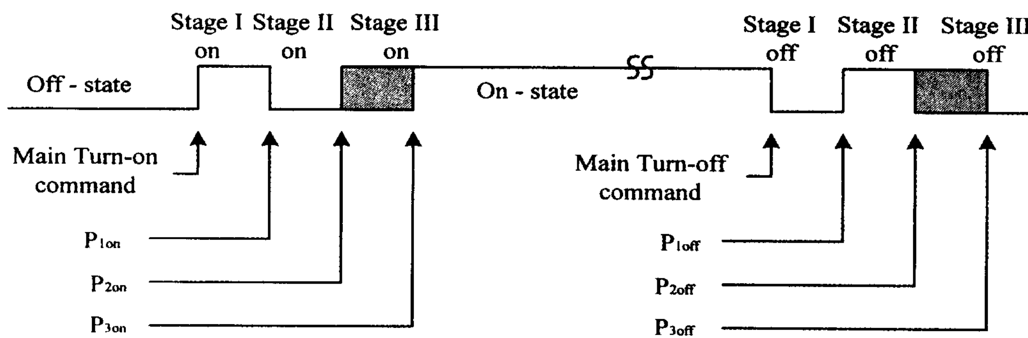

Fig. 2 Timing diagram corresponding to the three-stage active turn-on and turn-off switching

load current plus the peak reverse recovery current. The reverse recovery current can be effectively controlled due to the lower turn-on di/dt. The current injected into the gate during this stage is reduced so as to minimize the effects of the reverse recovery current on the converter system. These effects include the over-voltage across the complementary switch caused by free-wheeling diode snap-off and the EMI generated by the ringing during the reverse recovery transient. The circuit shifts to stage-III of turn-on at this point, and the gate is now rapidly charged to reduce the tail voltage thus decreasing the power loss during turn-on. Also, the Miller plateau duration and the total switching time are reduced by stage-III.

The main objective of the active turn-off circuit is to control the over-voltage at turn-off with minimal switching delay and switching loss. Stage-I of the three-stage active turn-off control starts at the main turn-off command. The first stage consists of rapid discharging of the gate-emitter capacitor until the rising

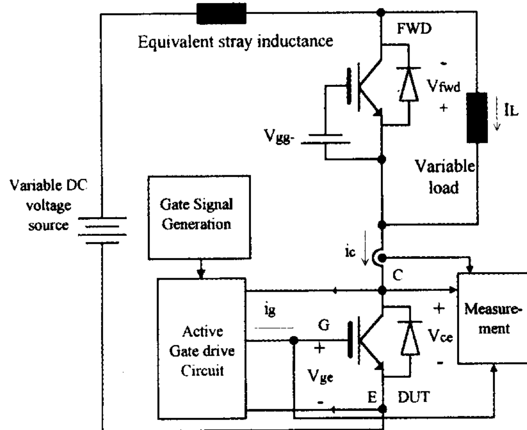

Fig. 3 The experimental setup used for investigating the gate drive circuits

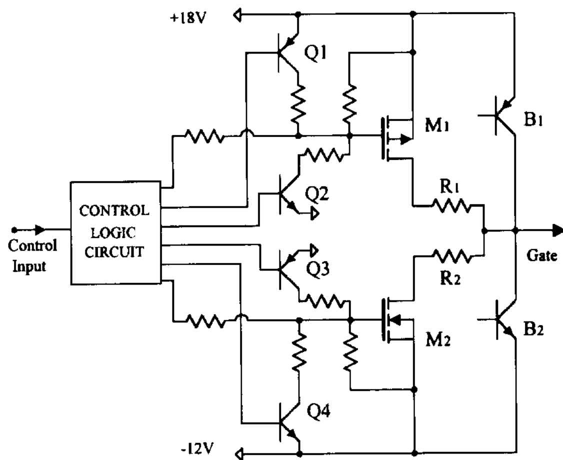

Fig. 4 Schematic of the proposed AGD circuit

instant of the collector voltage. This considerably reduces both the turn-off delay time and the power loss caused by the slow initial rise of the collector voltage. The large gate current during stage-I causes the gate voltage to go below the threshold voltage resulting in a higher dv/dt and a lower power loss. At this point stage-II is initiated and the gate current is reduced. The collector voltage rise during turn-off of the IGBT causes the gate voltage to charge up because of the displacement current through the gate-collector capacitor. The gate voltage goes above the threshold voltage, which results in excess carriers being injected into the IGBTs buffer region through the gate channel. This results in a lower turn-off di/dt and a reduced over-voltage during turn-off. The gate is discharged slowly during stage-II of turn-off operation. This stage continues through the rising period of the collector voltage and the falling period of the collector current. Stage-III is initiated at the end of the rapid falling of the collector current. This stage makes the gate voltage rapidly attain its final value. The gate voltage reaches its final negative value by the end of stage-III. This provides improved noise immunity during the off-state of the IGBT.[11] The total switching time is also reduced. Any re-turn-on of the IGBT is prevented in the three-stage method because the gate current remains negative in all three active turn-off stages, thus ensuring stable operation.

3. Implementation of the Three-Stage AGD

The schematic diagram of the gate drive circuit is shown in Fig. 4. A MOSFET and a BJT are used in parallel in the circuit for both turn-on and turn-off operation. The use of MOSFETs, M_1 and M_2, in the gate drive allows one to effectively obtain higher gate current required during stage-I and stage-III operation for high power IGBTs. Also, one can fully utilize the supply voltage in the gate drive and operate rail-to-rail by using a MOSFET. The BJTs, B_1 and B_2 in parallel with the MOSFETs allow precise gate current control during stage-II of the active switching transient. Additional BJTs, Q_1 to Q_4 are shown in Fig. 4, which are to control the MOSFETs, during stage-II and stage-III. Resistors R_1 and R_2 are used to limit the peak gate current and to obtain damped switching transients in the AGD circuit.

3.1 Active turn-on

At the main command to turn the IGBT on, stage-I is initiated by turning MOSFET M_2 off and turning M_1 on in Fig. 4. The use of an extremely low value of the gate resistor, R_1, results in rapid charging of the IGBT gate. The turn-off of M1 occurs at time P_{1on} shown in Fig. 2, which corresponds to the rising instant of the collector current in the IGBT. However, due to propagation time in the turn-off of M_1, one has to initiate the turn-off of M_1 at a prior instant. This can be selected as a fixed parameter for an IGBT of given ratings. P1on can also be triggered by measuring the gate voltage. The gate

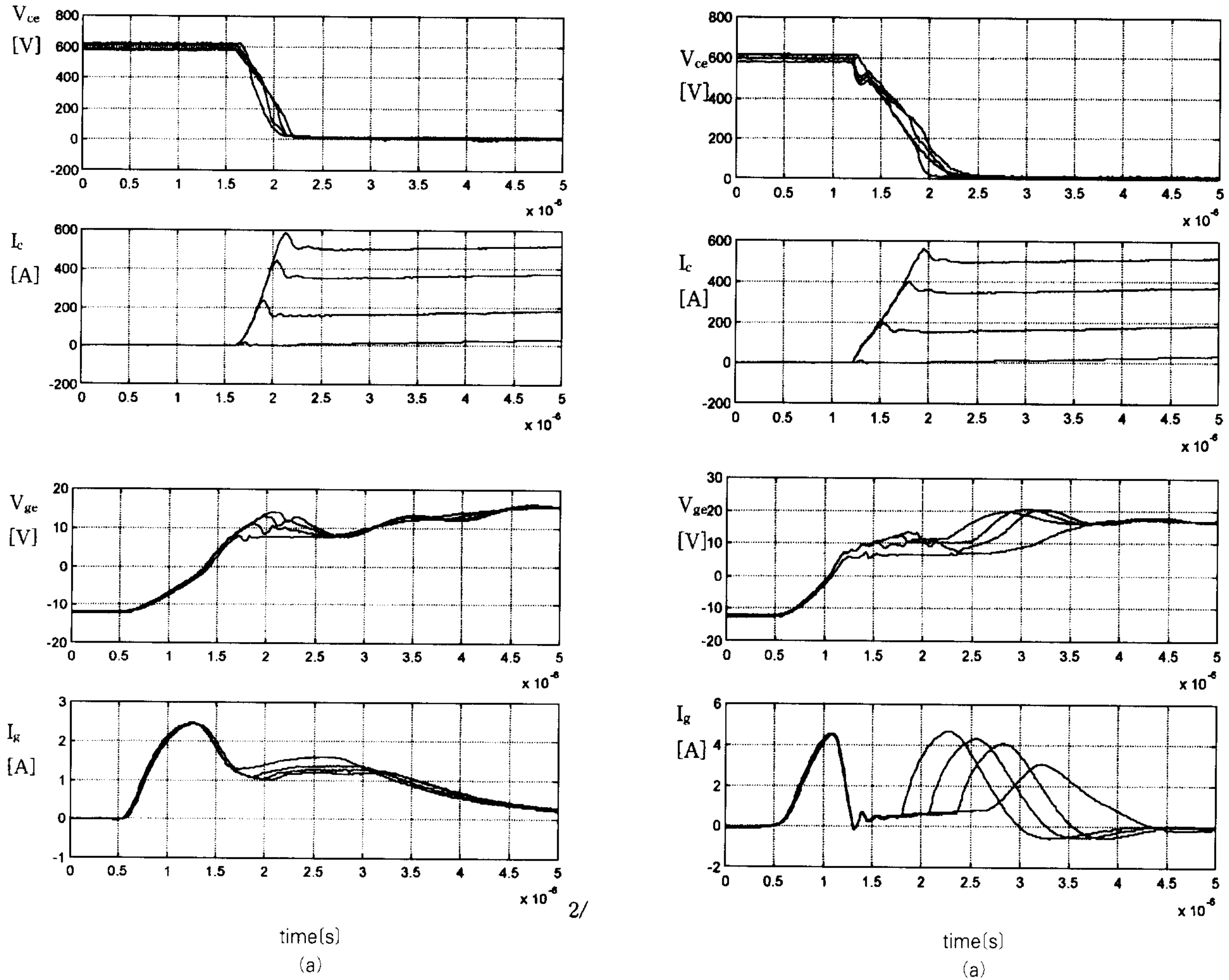

Fig. 5 Measured turn-on switching waveforms (v_{ce}, i_c, v_{ge}, i_g) with (a) the CGD and (b) the AGD at current levels of 0, 150, 350, 500A. Turn-on resistor of 5.6Ω is used in the CGD. Other conditions are as follows: V_{dc} = 600V, V_{gg+} = 18V, V_{gg}^- = -12V

now charges at a controlled current level determined by transistor B_1, which is used in the active region as a controlled current source during stage-II. P_{2on} is detected in the AGD by utilizing the di/dt information by measuring the voltage from the Kelvin emitter to the power emitter in the IGBT. This allows the gate of the IGBT to be controlled based on the instantaneous load current level. Once the collector current reaches the peak reverse recovery current, stage-III is initiated by turning M_1 on again. P_{3on} is a fixed parameter based on the ratings of the IGBT and it can be considered the minimum on-time for the device under consideration.

3.2 Active turn-off

This is also realized by the three-stage AGD turn-off technique. At the main command to turn off the IGBT, MOSFET M_1 is turned off and M_2 is turned on. The resistor R_2 is selected to be a very low value in comparison with the recommended value from the data sheets. Stage-I continues until the rising instant of the collector voltage. P_{1off} is detected using a collector voltage de-saturation circuit. Stage-II is initiated at this instant by turning M_2 off. Transistor B_2 drains a controlled current level out of the gate during this stage. Stage-III is initiated at P_{2off}, which corresponds to the falling edge of the collector current. The gate voltage reaches its final negative value by P_{3off}, which can be considered to be the total turn-off time for the given IGBT.

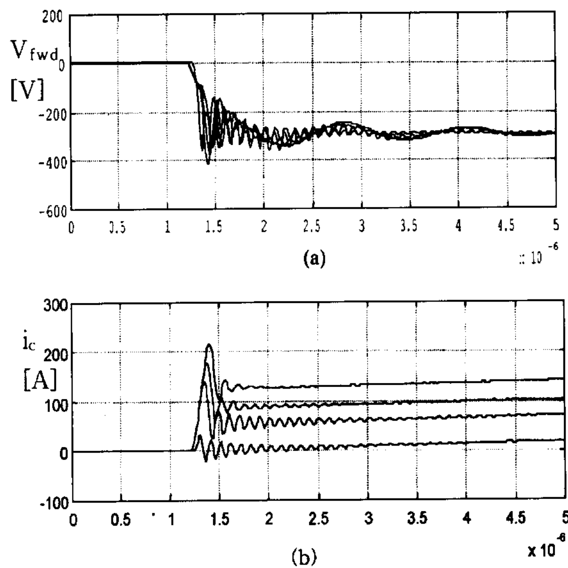

Fig. 6 Measured turn-on waveforms with the CGD at current levels of 0, 50, 80, 120A when the gate resistor of 0.5Ω is used
(a) The free-wheeling diode voltage
(b) The collector current.
Other conditions are as follows: V_{dc}= 300V, V_{gg+}= 18V, V_{gg-}= -12V

4. Performance of the Three-Stage AGD

Comparative results with the CGD are presented in order to investigate the operational performance of the three-stage AGD. The device used for the experimental test is a 1200V, 600A Powerex IGBT (CM600HA-24H). The switching waveforms for the CGD circuit were acquired using a gate resistance of 5.6Ω, which can be considered as a typical value for obtaining acceptable low noise switching for the IGBT. The value of the resistors R_1 and R_2 in the AGD shown in Fig. 3 is 0.5Ω. The trigger point for all measurements is the main command to the gate drive, which corresponds to zero in the time axis.

4.1 Investigation of turn-on characteristics

The turn-on switching waveforms of the CGD and the AGD at different load current levels are shown in Figs. 5(a) and (b) respectively. The waveforms plotted are the collector voltage, v_{ce}, the collector current, ic, the gate voltage, v_{ge}, and the gate current, i_g. It can be seen that the AGD circuit reduces the turn-on delay time as well as the total switching time, while limiting the reverse recovery current below that obtained using the CGD. The di/dt in the AGD is controlled by stage-II to a lower value and the collector voltage is held higher for a longer duration during the rising time of the collector current. The time required for the gate voltage to reach the given positive bias voltage, +18V, is reduced in the AGD. Therefore, the turn-on switching energy due to the tail voltage can be considerably reduced. The effect of variation of collector current level on the AGD can be seen from the gate current waveforms, which show the adaptation of the duration of stage-II based on the instantaneous load current level.

If one uses a small fixed gate resistor (0.5Ω) in the CGD circuit, the peak reverse recovery current and the peak voltage across the free-wheeling diode will be large. In particular, there are large oscillations at low current turn-on as can be seen in the free-wheeling diode voltage and the collector current waveforms in Figs. 6(a) and (b) respectively. This effect occurs because the rapid turn-on of the device can set up highly under-damped oscillations between the parasitic capacitance of the device and the inductance of the bus structure and interconnects. The snap-off process during the reverse recovery excites the oscillation. The reduction in oscillation at higher current levels is caused by the conductivity modulation lag effect during turn-on transient. This effect increases the effective resistance in the circuit at turn-on[12], and dampens out the turn-on oscillations. The AGD extends the duration of stage-II turn-on operation and damps out oscillations at low current turn-on as shown in Fig. 5(b). Increase in the turn-on power loss due to longer stage-II does not occur due to the very low load current level.

Fig. 7(a) and (b) show the effect of the control of the turn-on di/dt in the CGD and the AGD respectively. This can be achieved in the CGD by varying the gate resistor value. The whole gate current waveform is lowered when the gate resistor is increased, as shown in Fig. 7(a). This leads to the longer turn-on delay and the larger collector voltage tail. From the gate current waveform in Fig. 7(b), it can be seen that the turn-on di/dt in the AGD is effectively controlled by the variation of gate current during stage-II without affecting the delay time. Variation of the dc bus voltage does not lead to any significant difference in the

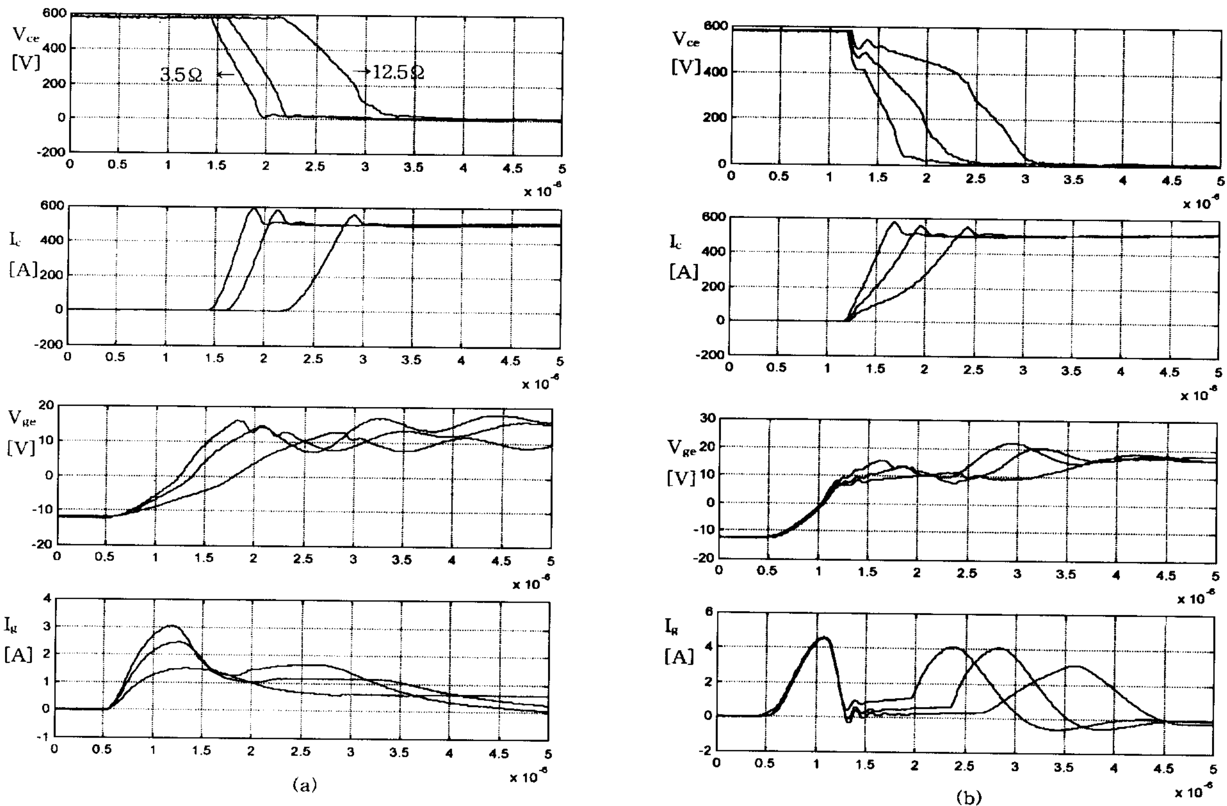

Fig. 7 Measured turn-on switching waveforms (vce, ic, vge, ig) with (a) the CGD and (b) the AGD when the turn-on di/dt is varied. Turn-on gate resistors used for varying di/dt in the CGD are 3.5, 5.6, 12.5Ω. Other conditions are as follows: V_{dc} = 600V, V_{gg+} = 18V, V_{gg-} = -12V

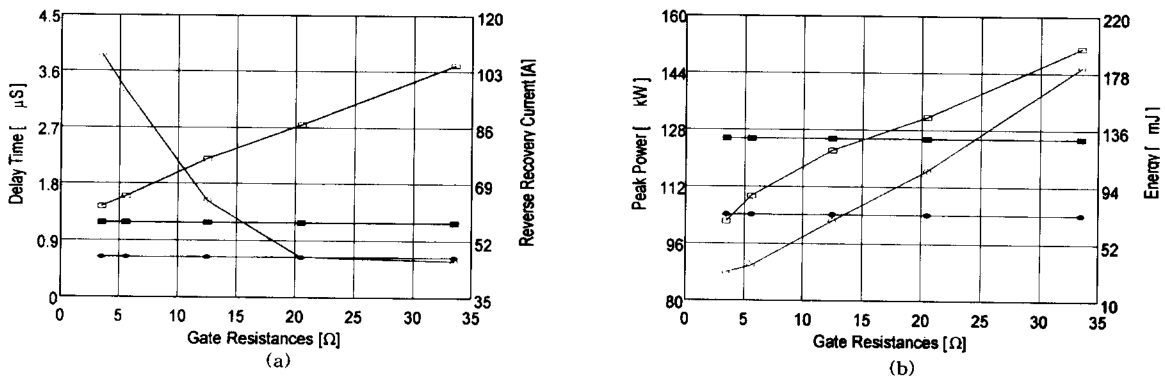

Fig. 8 Comparison of turn-on characteristics between the AGD and the CGD as gate resistance is varied. (a) Investigation of the turn-on delay time, Td (CGD) and Td (AGD), and the peak reverse recovery current, Irr (CGD) and Irr (AGD). (b) Investigation of the peak power, Pon(CGD) and Pon(AGD), and the turn-on energy loss, Eon(CGD) and Eon(AGD). Operating conditions are as follows: Vdc = 600V, IL= 350A, Vgg+ = 18V, Vgg- = -12V

performance of the CGD or the AGD. The turn-on di/dt is higher at the larger dc bus voltage.

Figs. 8(a) and (b) show the trade-off in turn-on characteristics of the delay time, the peak reverse recovery current, the peak power dissipation, and the energy loss in the case of the CGD. Different turn-on gate resistors are used under a constant load current of 350A. It is also compared with the results obtained with

the AGD circuit at the same power condition. As the turn-on gate resistor, R_{gon}, is increased, the delay time and the dissipated turn-on energy increase while the peak reverse recovery current decreases. The AGDs delay time is shorter than that of a CGD with R_{gon} of 3.6Ω and reverse recovery current lower than that of a CGD with 15Ω , and the switching energy less than a CGD with 12.5Ω. The improved performance of the AGD over the CGD holds good for a wide range of current levels and operating conditions.

4.2 Investigation of turn-off characteristics

The switching waveforms of the CGD and the AGD at turn-off for different load current levels are shown in Figs. 9(a) and (b) respectively. The turn-off dv/dt is higher in the AGD while the di/dt is lower. The AGD results in a lower over-shoot and ringing in the collector voltage waveform as shown in Fig. 9(b). This can lead to lower EMI generated during turn-off transient. The peak over-shoot in the collector voltage is limited to a lower level for a wide range of current levels in the AGD. As turn-off delay time is varied with load current, the transition from stage-I to stage-II is adapted by the AGD to further reduce the turn-off di/dt at higher current levels. The active turn-off reduces the switching losses by reducing the slow initial rising duration of the collector voltage, while at the same time achieving better control of the over-voltage compared to the case of utilizing a large gate resistor in the CGD circuit.

Figs. 10(a) and (b) show the control of the turn-off di/dt during turn-off switching transient. This is achieved in the CGD by controlling the gate resistor value. Increasing the gate resistor results in increased switching delay and a softer switching transient. The lower dv/dt that occurs with larger gate resistors increases the turn-off energy. The di/dt control in the

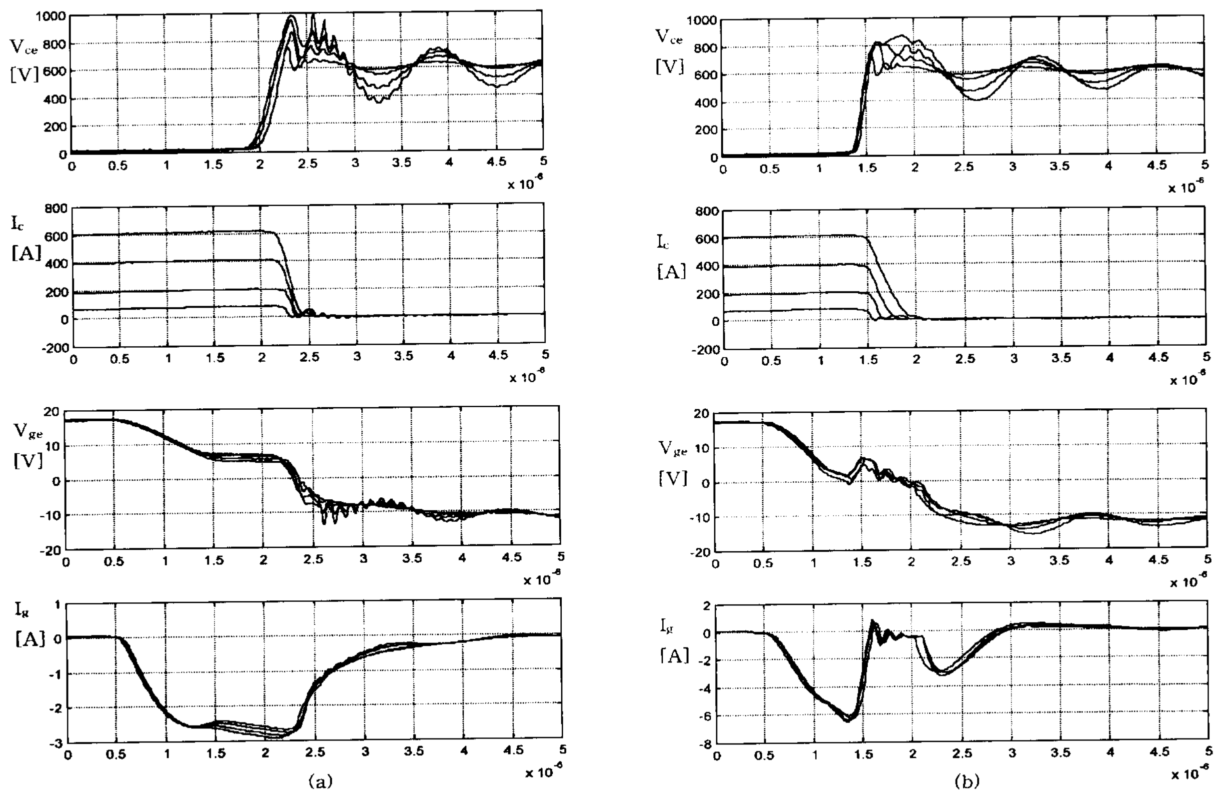

Fig. 9 Measured turn-off switching waveforms (vce, ic, vge, ig) with (a) the CGD and (b) the AGD at current levels of 80, 205, 405, 620A. Turn-off gate resistor used in the CGD is 5.6Ω. Other conditions are as follows: V_{dc} = 600V, V_{gg+} = 18V, V_{gg-} = -12V

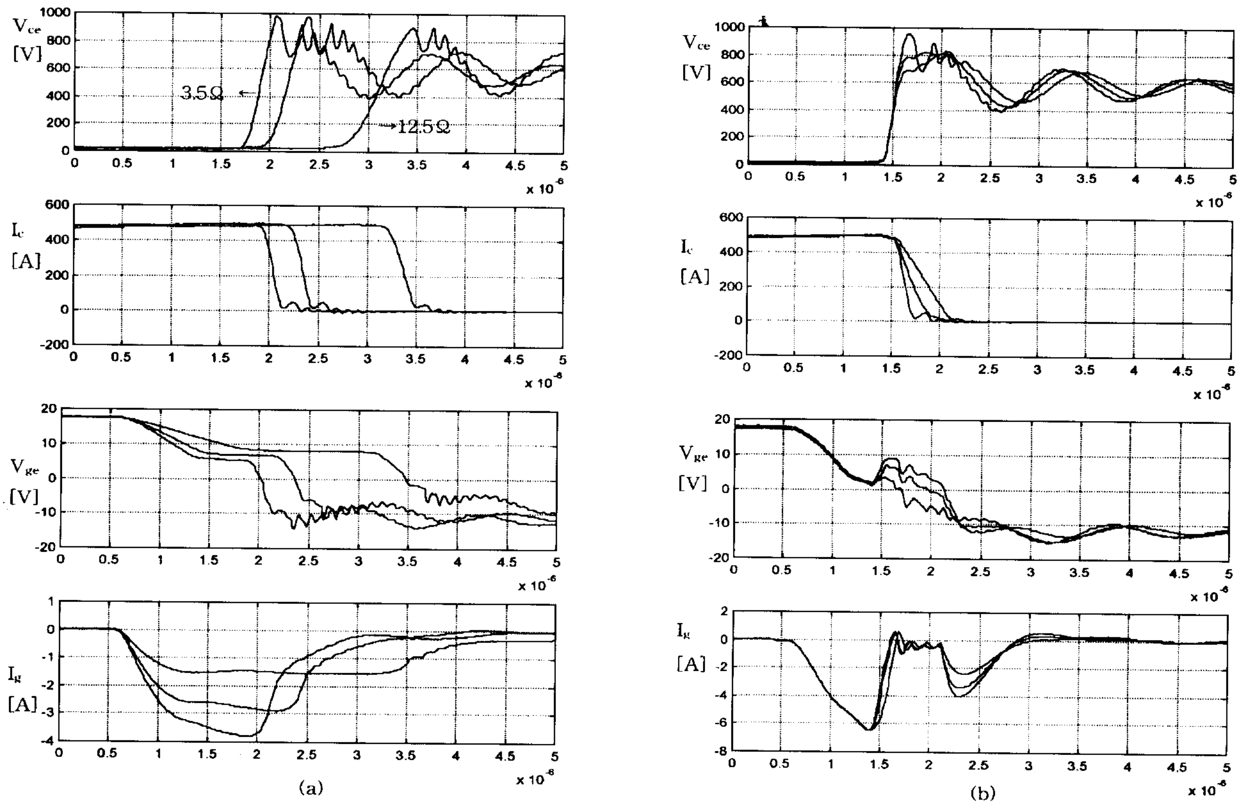

Fig. 10 Measured turn-off switching waveforms (v_{ce}, i_c, v_{ge}, i_g) with (a) the CGD and (b) the AGD when the turn-off di/dt is varied. Turn-off gate resistors used in the CGD for varying di/dt are 3.5, 5.6, 12.5Ω. Other conditions are as follows: V_{dc} = 600V, IL = 500A, V_{gg+} = 18V, V_{gg-} = -12V

AGD is achieved by advancing or delaying the P1off control point. This determines the gate voltage level during stage-II of active turn-off. From the collector current waveforms in Fig. 10(b), it can be seen that the switching delay time and the di/dt variation are de-coupled. The higher turn-off di/dt results in the higher collector over-voltage, but reduces the energy loss.

Figs. 11(a) and (b) show the effect of increasing the dc bus voltage on the performance of the CGD and the AGD respectively. The over-voltage level in case of the CGD is similar at higher dc bus voltages. In case of the AGD the over-voltage is reduced as the dc bus [A] voltage is increased, because the reverse transfer capacitance, the collector-gate capacitance of the IGBT, is more effective in increasing the gate voltage during stage-II. This can be seen from the gate voltage waveform of the AGD in Fig. 11(b). This leads to lower turn-off di/dt at higher dc bus voltages in the AGD.

The trade-off in the CGD performance according to variation of the turn-off gate resistance and the comparison with that of the AGD are illustrated in Fig. 12. Figs. 12(a) and (b) are for a load current level of 150A and Figs. 12(c) and (d) are for 620A. The turn-off performance is compared in terms of parameters such as the delay time, the peak collector voltage, the peak power dissipation, and the energy loss at turn-off. As the turn-off gate resistor, Rgoff, is increased, the delay time and the turn-off energy loss increase, while the peak collector voltage reduces. The AGD has the turn-off delay lower than that of a CGD with Rgoff of 3.6Ω and the over-voltage of the AGD is less than that of a CGD with 5.6Ω at a collector current level of 150A. The turn-off energy is lower than that of a CGD with 5.6Ω. At higher current level, the AGD is more effective in suppressing the over-voltage. Fig. 12(c) shows that the AGD has a lower over-voltage than that of a CGD with 33Ω at a turn-off current level of 620A.

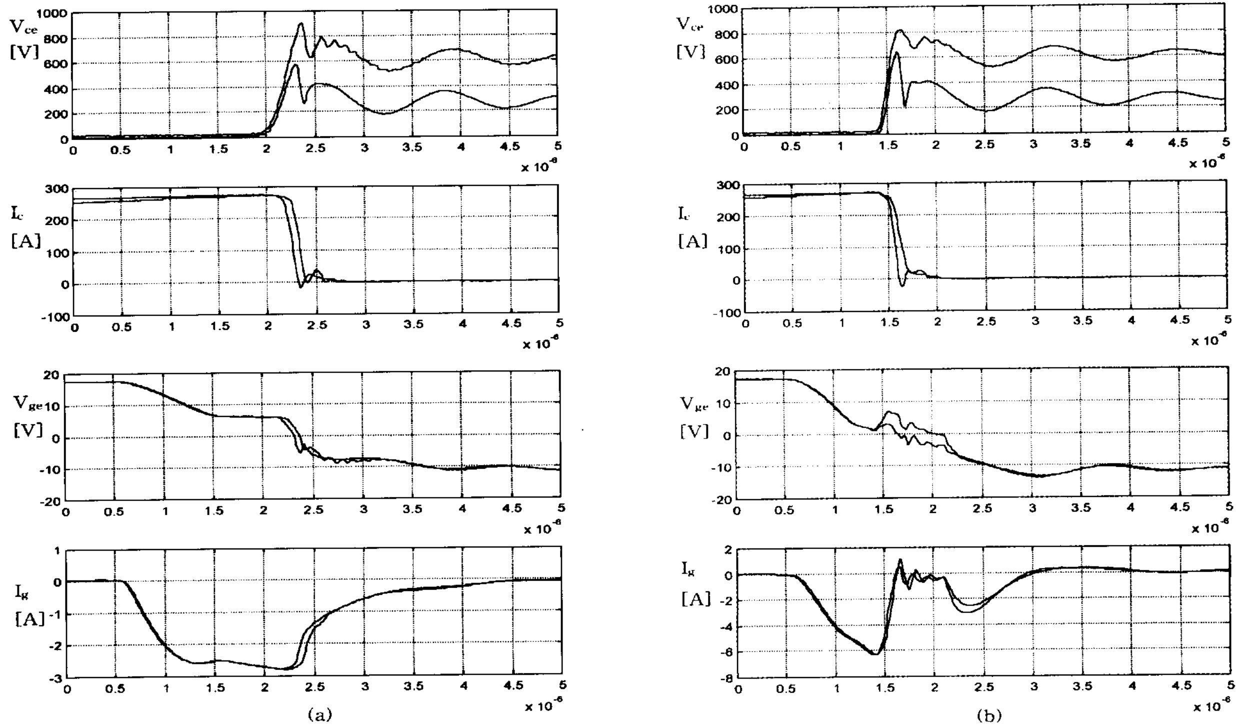

Fig. 11 Measured turn-off switching waveforms (v_{ce}, i_c, v_{ge}, i_g) with (a) the CGD and (b) the AGD when the dc bus voltage is varied. The dc bus voltages are 300, 600V. Turn-off gate resistor used in the CGD is 5.6Ω. Other conditions are as follows: IL = 270A, V_{gg+} = 18V, V_{gg-} = -12V

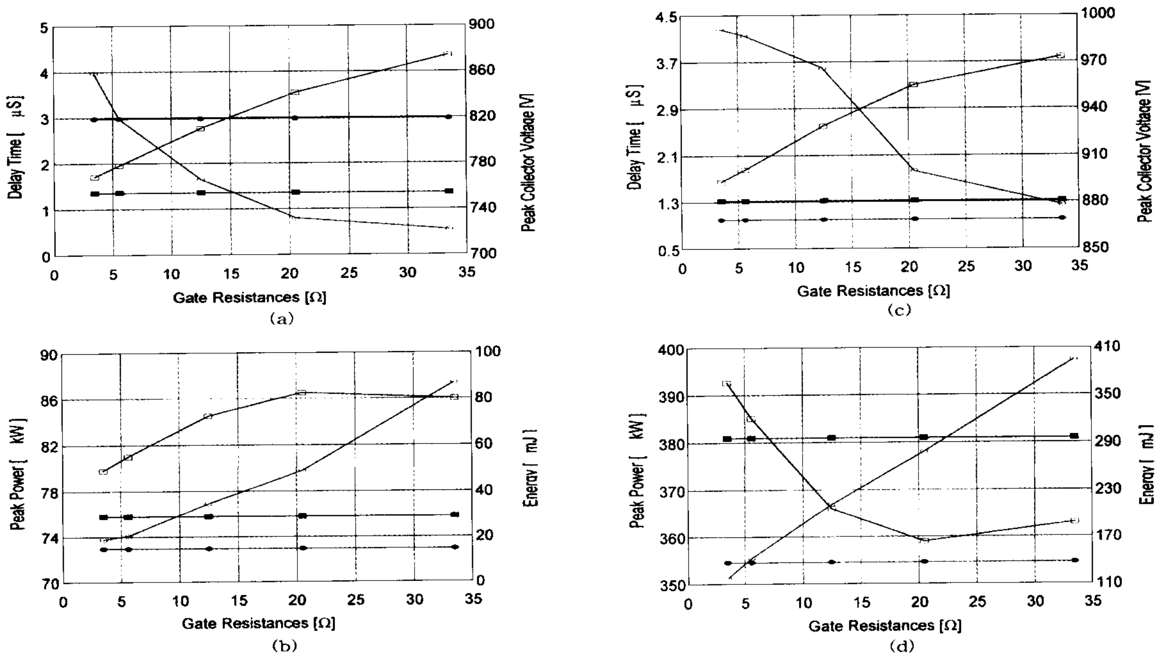

Fig. 12 Comparison of turn-off characteristics between the AGD and the CGD as the gate resistance is varied. IL = 150A in charts (a) and (b). IL = 620A in charts (c) and (d). (a) and (c) investigate the delay time, $T_{d\,(CGD)}$ and $T_{d\,(AGD)}$, and the peak collector voltage, $V_{ce\,(CGD)}$ and $V_{ce\,(AGD)}$. (b) and (d) investigate the peak power, $P_{off(CGD)}$ and $P_{off(AGD)}$, and the energy loss, $E_{off(CGD)}$ and $E_{off(AGD)}$. Operating conditions are as follows: V_{dc} = 600V, V_{gg+} = 18V, and V_{gg-} = -12V

5. Conclusions

The proposed AGD circuit is able to achieve shorter switching delay and total switching time. Thus it can be operated with lower blanking times leading to lower distortion in the output spectrum of the IGBT power converters. The lower peak reverse recovery current level at turn-on and the lower peak over-voltage at turn-off can reduce the switching stress and EMI problem. The switching energy in the AGD is lower than that of a CGD operating at the same peak device stress level. One drawback of the AGD is control complexity, and the AGD has to be tuned to operate with the individual device. However, most of the tuning can be implemented as software initialization of the gate drive unit. This would make the AGD compatible with a wide range of IGBT applications. Also, the same gate drive circuit can be used in both hard-switched and soft-switched applications. In a soft-switched power converter, stage-II of the AGD switching operation can be eliminated to obtain a high speed gate drive. Such a gate drive circuit would be appropriate for building standardized power converters like the Power Electronic Building Blocks.

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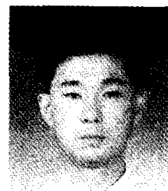

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