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부스트-플라이백 결합형 ZCS Quasi-Resonant 역률개선 컨버터

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Integrated Boost-Flyback ZCS Quasi-Resonant Power Factor Preregulator

Jun-Young Lee, Gun-Woo Moon, Hyun-Soo Kim, and Myung-Joong Youn

요 약

본 논문에서는 역률개선용 단일 스위치 부스트 플라이백 결합형 ZCS quasi-resonant converter(QRC)를 제안한다. 제안된 컨버터는 입력전류를 불연속 모드로 동작시켜 역률을 개선하며 입력전류의 zero-crossing-point에서의 왜곡을 개선함으로써 고조파를 감소시켜 역률을 향상시켰으며 좋은 출력전압의 regulation 성능을 가지고 있다. 그리고 체계적인 설계를 위하여 설계식을 제안하였으며 제안된 설계식을 통하여 프로토타입 컨버터를 설계하였다. 실험결과 효율은 약 86%, 역률은 약 0.985이상을 얻었다. 따라서 본 컨버터는 스위칭 주파수가 수백kHz이상이고 높은 regulation성능을 요구하는 낮은 전압의 소용량 컨버터에 적합하다.

ABSTRACT

An integrated ZCS quasi-resonant converter(QRC) for the power factor correction with a single switch is presented in this paper. The power factor correction can be achieved by the discontinuous conduction mode(DCM) operation of the input current. The proposed converter gives the good power factor, low line current harmonics, and tight output regulation. The input current waveform of the prototype designed using design equations shows about 15% of total harmonic distortion at rated condition. Also, the efficiency and power factor can be obtained about 86% and 0.985, respectively, at rated condition. The proposed converter is suitable for a low power level converter with a tightly regulated low output voltage and switching frequency of more than several hundreds kHz.

Key Words: Discontinuous Conduction Mode(DCM), Quasi-Resonant Converter(QRC), Power Factor Correction(PFC)

1. INTRODUCTION

Conventional off-line power supplies usually include the full-bridge rectifier and large input filter capacitor at input stages. They generate highly distorted input current waveforms with large amount of harmonics. Recently, standards such as IEEE 519 and IEC 61000 impose a limit on the harmonic current drawn by equipments connected to an AC line in order to prevent the distortion of an AC line voltage.[1],[2] Consequently, a power factor preregulator is an unavoidable choice. To meet the requirement, a number of power factor preregulators have been developed and these can be divided into two categories: the two stage approach and the single stage approach. In the two stage approach, it is customary to add a power factor corrector ahead of a DC/DC converter to provide a regulated and isolated DC output. This approach is widely used because of good characteristics of the continuous line current, small choke filter, high power factor, and fast output regulation, but the power factor preregulator increases the cost and size.[3],[4] Therefore, the two stage approach

is not desirable in low power level applications. To solve this problem, many single stage topologies have been suggested to achieve both power factor correction and power conversion from an AC line to the desired DC output. Most of them adopt the PWM control method for an output regulation but they are useful when the switching frequency is lower than 100kHz due to the heavy switching losses which affect the overall efficiency and size.[5] To overcome this disadvantage, a resonant power factor correction technique has been introduced. However, most of them have dealt with power factor preregulators with multiplier type input current controllers and only a small number of papers have suggested and analyzed DCM resonant topologies.[6],[7] Unfortunately, these topologies suffer from the input current distortion at zero-crossing-points and large output voltage ripple. Since the power factor correction is affected by the output voltage regulation in single stage DCM PFC converters with voltage follower control, the output voltage controller should have a low bandwidth. Thus, a large output voltage ripple is not good for the tight output voltage regulation and high quality input current waveform.

In this paper, an integrated ZCS QRC for the power factor correction based on a flyback converter is proposed. This converter operating in DCM has the low output voltage ripple and tight output regulation. In addition, this converter does not have the input current distortion at zero-crossing-points. Design equations which are obtained from a large signal model are derived for a systematic design procedure. Using design equations, a prototype is designed and experimented to show the advantages of the proposed converter by comparing with SEPIC QRC.

2. MODE ANALYSIS

Fig. 1 shows the circuit diagram of the proposed converter with a conventional single output voltage loop. The basic structure can be understood as a cascade connection of a boost converter followed by a flyback QRC. As shown in Fig. 2, each switching period is subdivided into six modes and their topological states are shown in Fig. 3. To illustrate the steady-state operation, the following assumptions are made:

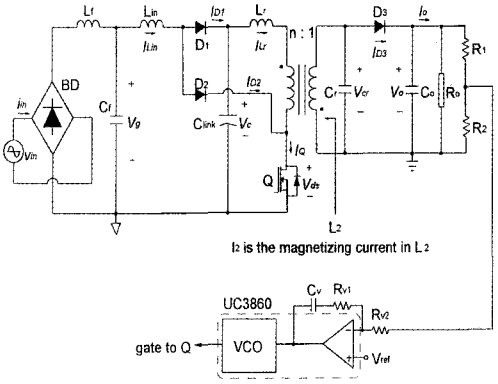

그림 1 제안된 컨버터
Fig. 1 Schematic of the proposed converter

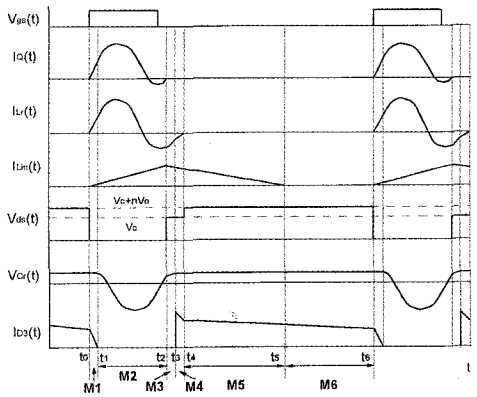

그림 2 모드해석을 위한 주요파형
Fig. 2 Key waveforms for mode analysis

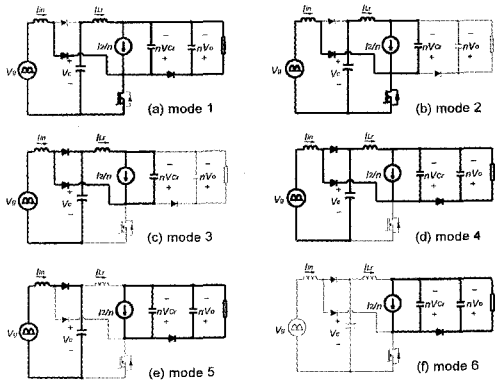

그림 3 동작 모드 다이아그램
Fig. 3 Operational mode diagrams

(a) The switch Q is ideal except for its internal diode
(b) The link capacitor voltage is assumed to be a constant DC voltage, V_C
(c) The output voltage is assumed to be a constant DC

voltage, V_o

(d) The magnetizing inductance of the transformer is so large that it is assumed to be a constant current source.

Mode 1 ($t_0 < t \le t_1$)

Mode 1 begins at t_0 when the switch Q is turned on. Since the resonant inductor current, $I_{Lr}(t)$, is smaller than the magnetizing current reflected to the transformer primary, I_2/n, the rectifying diode, D_3, is still turned on and the resonant capacitor voltage, $V_{Cr}(t)$, is clamped by the output voltage, V_o. Thus, $I_{Lr}(t)$ is linearly increased and can be expressed as

$$I_{Lr}(t) = \frac{V_C + nV_o}{L_r}(t - t_o) \tag{1}$$

Also the input inductor current is linearly increased with the slope of V_g/L_{in} as follows:

$$I_{Lin}(t) = \frac{V_g}{L_{in}}(t - t_o) \tag{2}$$

This mode stops when $I_{Lr}(t)$ reaches I_2/n where n is the transformer turns ratio. The duration of this mode can be expressed as

$$T_{d1} = \frac{L_r I_2}{nV_C + n^2 V_o} \tag{3}$$

Mode 2 ($t_1 < t \le t_2$)

The rectifying diode, D_3, is reverse biased as the resonant capacitor discharges its energy to the resonant inductor. From the equivalent circuit (b) in Fig. 3, the voltage across the resonant capacitor, $V_{Cr}(t)$, decreases sinusoidally as

$$\frac{dV_{Cr}(t)}{dt} = \frac{I_2}{C_r} - \frac{nI_{Lr}(t)}{C_r} \tag{4}$$

and the rate of increase of the resonant current becomes

$$\frac{dI_{Lr}(t)}{dt} = \frac{V_C}{L_r} - \frac{nV_{Cr}(t)}{L_r} \tag{5}$$

The solutions of eqs. (4) and (5) with the initial conditions of $I_{Lr}(t_1) = I_2/n$ and $V_{Cr}(t_1) = V_o$ are as follows:

$$I_{Lr}(t) = \frac{I_2}{n} + \frac{1}{Z_r}(V_C + nV_o)\sin\omega_r(t - t_1) \tag{6}$$

$$V_{Cr}(t) = \frac{I}{n}\left[(V_C + nV_o)\cos\omega_r(t - t_1) - V_C\right] \tag{7}$$

where $Z_r = n\sqrt{L_r/C_r}$, and $\omega_r = n\sqrt{L_r/C_r}$. In this mode, $I_{Lin}(t)$ is still increased linearly and expressed as

$$I_{Lin}(t) = \frac{V_g}{L_{in}}(t - t_1 + Td_1) \tag{8}$$

The switch current will continue to oscillate and feed energy back to the link capacitor. The duration of mode 2, T_{d2}, can be found by setting $I_Q(t_2) = I_{Lr}(t_2) + I_{Lin}(t_2) = 0$. The approximated expression of T_{d2} is

$$T_{d2} \approx \frac{4(V_C + nV_o)/Z_r - I_2/n - T_{d_1}V_g/L_{in}}{V_g/L_{in} + 2\omega_r(V_C + nV_o)/\pi Z_r} \tag{9}$$

Mode 3 ($t_2 < t \le t_3$)

Mode 3 begins after Q is turned off at t_2. Since the current flowing in the resonant inductor cannot change abruptly, the diode D_2 is still turned on to make the path for $I_{Lr}(t)$ and the diode D_1 also starts to conduct to transfer the energy charging in L_{in} to the link capacitor. Thus, the resonant capacitor, C_r, is able to be charged by $I_{Lr}(t)$ and I_2/n through D_1 and D_2. Fig. 3(c) is the diagram of this mode and the differential equations can be written from this mode diagram as follows:

$$\frac{dI_{Lr}(t)}{dt} = \frac{nV_{cr}(t)}{L_r} \tag{10}$$

$$\frac{dV_{cr}(t)}{dt} = \frac{I_2}{C_r} - \frac{nI_{Lr}(t)}{C_r} \tag{11}$$

Therefore, the solutions are

$$I_{Lr}(t) = \frac{V_{cr}(t_2)}{Z_r}\sin\omega_r(t - t_2) + \left(I_{Lr}(t_2) - \frac{I_2}{n}\right) \times \cos\omega_r(t - t_2) + \frac{I_2}{n} \tag{12}$$

$$V_{Cr}(t) = V_{Cr}(t_2)\cos\omega_r(t - t_2) - Z_r\left[\frac{I_{Lr}(t_2)}{n} - \frac{I_2}{n^2}\right] \times \sin\omega_r(t - t_2) \tag{13}$$

where $V_{Cr}(t_2)$ and $I_{Lr}(t_2)$ are initial conditions of this mode, which are found from eqs. (6), (7), and (9). Since the switch Q is turned off after mode 2, $I_{Lin}(t)$ begins to be linearly decreased as follows:

$$I_{Lin}(t)=\frac{V_g-V_C}{L_{in}}(t-t_2)+\frac{V_g}{L_{in}}(T_{d1}+T_{d2}) \quad (14)$$

This mode stops when $V_{Cr}(t)$ is equal to V_0 and the duration of this mode can be found from eq. (13) as follows:

$$T_{d3}=\frac{1}{\omega_r}\left[A-\sin^{-1}B\right] \quad (15)$$

where

$$A=\tan^{-1}\left(\frac{V_{cr}(t_2)}{Z_r\left[I_2/n^2-I_{Lr}(t_2)/n\right]}\right)$$

$$B=\frac{V_0}{\sqrt{V_{cr}(t_2)^2+\left[Z_r(I_2/n^2-I_{Lr}(t_2)/n)\right]^2}}$$

Mode 4 ($t_3<t\leq t_4$)

Since the output bulk capacitor is connected to the resonant capacitor, C_r, in parallel, $V_{Cr}(t)$ is clamped by V_0 and $I_{Lr}(t)$ is linearly increased as shown in eqs. (16) and (17):

$$I_{Lr}(t)=\frac{V_o}{L_r n}(t-t_3)+I_{Lr}(t_3) \quad (16)$$

$$V_{Cr}(t)=V_o \quad (17)$$

where $I_{Lr}(t_3)$ is the initial condition of mode 3 and it can be found from eqs. (12) and (15). Since $I_{Lr}(t)$ reflected to the transformer secondary flows to the load, the powering mode is initiated. This mode stops when $I_{Lr}(t)$ reaches zero and the duration of mode 4 is

$$T_{d4}=\frac{I_{Lr}(t_3)L_r n}{V_o} \quad (18)$$

Until the energy held in L_r is fully transferred to the resonant capacitor and the output bulk capacitor, both D_1 and D_2 keep conducting. Therefore, as can be seen in the mode diagram, the drain-source voltage of the switch Q is equal to the link voltage during modes 3 and 4.

Mode 5, 6 ($t_4<t\leq t_6$)

During modes 5 and 6, the input inductor current is reduced to zero and the energy charged in the transformer is transferred to the load which is the same as the conventional flyback operation. By setting eq.

$$T_{d5}=\frac{V_g}{V_C-V_g}(T_{d1}+T_{d2})-T_{d3}-T_{d4} \quad (19)$$

and that of mode 6 is

$$T_{d6}=T_s-\sum_{i=1}^{5}T_{di} \quad (20)$$

where T_s means a switching period. It is noted that since almost all of the 120Hz ripple energy of the input inductor current is absorbed by the link capacitor, the output voltage regulation is not seriously influenced by the input power factor correction. Furthermore, while achieving the ZCS of the switch, the proposed convertor has the good characteristic of low line current distortion at the line zero-crossing, since the input inductor current of the proposed convertor is not disturbed by the resonance and its slopes are determined only by the line and link voltages.

3. DESIGN

3.1 Selection of L_{in} and n

To determine L_{in}, a steady state analysis must be performed in advance. If the converter efficiency, η, is considered as a design parameter, the steady state solutions of V_0 and V_C becomes

$$V_c=\frac{V_{grms}}{\sqrt{2}}\left(1+\sqrt{1+\frac{0.852n^2\eta R_o(1-D_f)^2}{L_{in}D_f f_r}}\right) \quad (21)$$

$$V_o=\frac{D_f}{1-D_f}\frac{V_c}{n} \quad (22)$$

where $D_f\equiv f_s/f_r$, and f_s is the switching frequency and f_r is the resonant frequency.[1] To maintain a sinusoidal input current, the input inductor current must flow in DCM. This requirement is guaranteed by the following condition as

$$\frac{\sqrt{2}V_{grms}}{V_c-\sqrt{2}V_{grms}}(T_{d1}+T_{d2})f_s\leq 1-(T_{d1}+T_{d2})f_s \quad (23)$$

Since T_{d1} and T_{d2} are also the function of the link voltage V_C, the derivation of a design equation of L_{in} is difficult. However, by noting that the relationship between $T_{d1}+T_{d2}$ and the resonant period, T_r, over the entire cycle is

$$T_{d1}+T_{d2}\leq T_r \quad (24)$$

eq. (23) can be written as follows:

$$\frac{\sqrt{2}V_{grms}}{V_c-\sqrt{2}V_{grms}}D_f \le 1-D_f \quad (25)$$

With eqs. (21), (22), and (25), the maximum L_{in} to meet DCM can be calculated as follows:

$$L_{in} \le \frac{0.426D_f\eta R_o V_{grms}^2}{f_s V_o^2} \quad (26)$$

Once L_{in} is found by using eq. (26) and design specifications at the worst case, the transformer turns ratio, n, can be obtained using eqs. (21) and (22).

3.2 Selection of L_r and C_r

During mode 2, the switch current is written as

$$I_Q(t)=\frac{I_2}{n}+\frac{1}{Z_r}(V_C+nV_o)\sin\omega_r(t-t_1) + \frac{V_g}{L_{in}}(t-t_1+T_{d1}) \quad (27)$$

In order to achieve a ZCS condition over the entire line cycle, the switch current must be zero at the end of mode 2 when the line voltage has a peak value. This can be written as follows:

$$\frac{I_2}{n}+\frac{1}{Z_r}(V_C+nV_o)\sin\zeta+\frac{\sqrt{2}V_{grms}}{L_{in}}(\frac{\zeta}{\omega_r}+T_{d1})=0 \quad (28)$$

where ζ is defined as $\omega_r T_{d2}$. This condition may be satisfied when ζ has a value between π and 2π. Furthermore, due to the heavy current stress on the switch which is the general characteristic of a ZCS QRC, it is necessary to select a suitable value such that the current stress can be minimized. Eq. (27) clearly shows that a current stress of the switch becomes minimal when the characteristic impedance Z_r satisfying a given resonant frequency is selected as large as possible and this condition can be accomplished if has ζ the value of $3\pi/2$. With predetermined value of L_{in}, eq. (28) becomes

$$Z_r=\frac{V_C+nV_o}{\frac{I_2}{n}+\frac{\sqrt{2}V_{grms}}{L_{in}}\left(\frac{3\pi}{2\omega_r}+T_{d1}\right)} \quad (29)$$

Therefore, L_r and C_r are determined using eqs. (3), (21), (29), and a desired resonant frequency, ω_r.

3.3 Selection of Switch

The voltage stress of switch is expressed as following equation:

$$V_{ds}=V_C+nV_o \quad (30)$$

The worst case of voltage stress happens at a light load. Thus, the maximum voltage stress can be found using eqs. (21) and (30) with $R_o=R_{omax}$ and $f_s=f_{smin}$.
Also, the worst case of current stress happens at a full load and the peak line voltage. The peak current stress can be expressed as

$$I_{Qpk}=\frac{\sqrt{2}V_{grms}}{L_{in}}\left(\frac{\pi}{2\omega_r}+T_{d1}\right)+\frac{I_2}{n}+\frac{1}{Z_r}(V_C+nV_o). \quad (31)$$

4. EXPERIMENTAL RESULTS

The prototype converter has been implemented to show the operation of the proposed converter based on the design equations with following specifications:

Line voltage, Vg=110*Vrms*
Output voltage, Vo=15*V*
Output power, Po=20*W*-70*W*
Resonant frequency, fr=1.25*MHz*
Maximum switching frequency, fsmax=300*kHz*
Desired efficiency, =85%.

Using the design equations given in section III, the selected converter components are listed in Table 1. In addition, a simple PI controller has been designed using UC3860 from Unitrode Corporation. Figs. 4 and 5 show key waveforms of the proposed converter. From Fig. 4, it can be seen that there is the ringing of V_{ds} which

Table 1 Components list for the prototype

Switch	IRFP450	C_{link}	400μF
n:1	4.3:1	C_o	1000μF
L_{in}	49μH	C_r	37μF
L_r	8μH	C_f	0.1μF
L_f	80μH		

comes from the resonation of the output capacitance of the switch and the inductor connected in series with it when switch is turned off. Fig. 5 shows that the filtered input current follows the line voltage without any distortion at zero-crossing-points and the output voltage is tightly regulated. Figs. 6 and 7 show the normalized input current waveforms of SEPIC QRC in Fig. 8 and the proposed converter as a function of load for one half-cycle. The measured THDs of these two converters

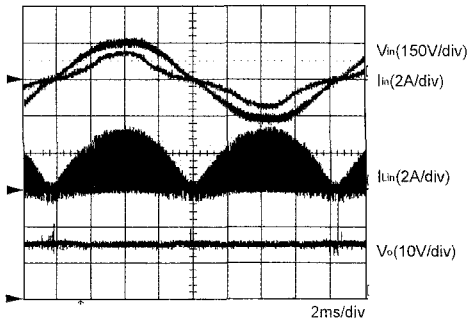

그림 4 V_{in}, I_{in}, I_{Lin}, V_o 의 실험파형동작
Fig. 4 Experimental waveforms of V_{in}, I_{in}, I_{Lin} and V_o

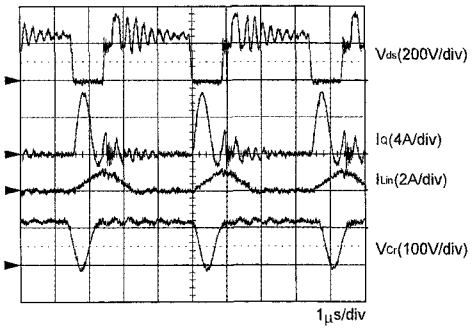

그림 5 V_{ds}, I_Q, I_{Lin}, V_{Cr} 의 실험파형동작
Fig. 5 Experimental waveforms of V_{ds}, I_Q, I_{Lin} and V_{Cr}

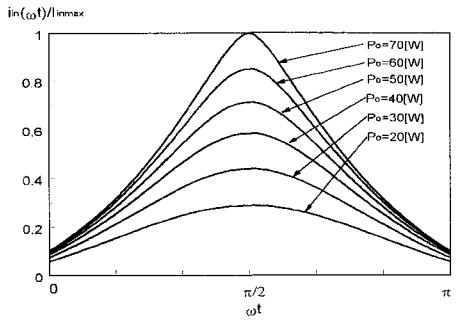

그림 6 부하변동에 따른 SEPIC QRC의 정규화된 입력전류파형
Fig. 6 Normalized input current waveforms of SEPIC QRC as a function of load

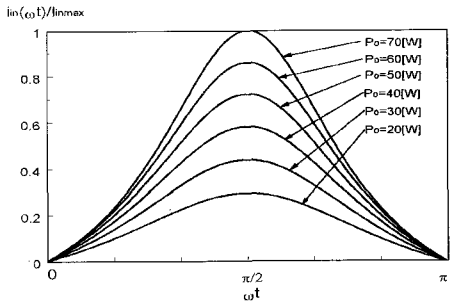

그림 7 부하변동에 따른 제안된 컨버터의 정규화된 입력전류파형
Fig. 7 Normalized input current waveforms of the proposed converter as a function of load

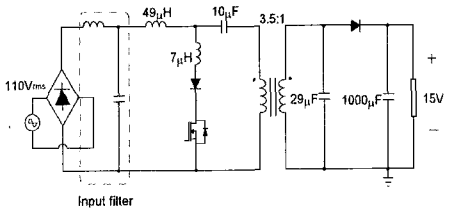

그림 8 SEPIC QRC의 회로도
Fig. 8 Schematic of conventional SEPIC QRC

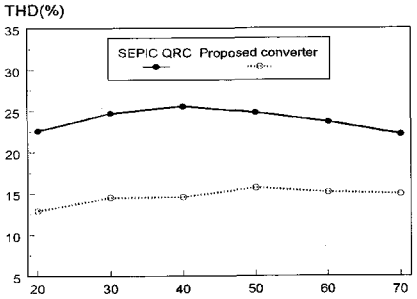

그림 9 SEPIC QRC와 제안된 컨버터의 THD
Fig. 9 The measured THDs of SEPIC QRC and the proposed converter

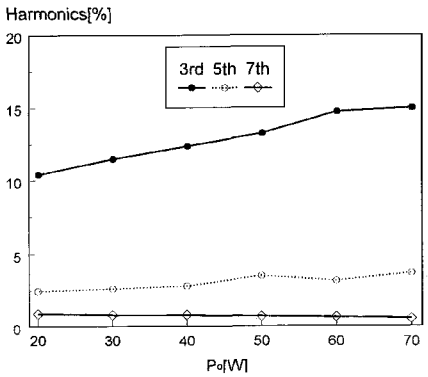

그림 10 부하변동시 제안된 컨버터의 주요 고조파 첨두치
Fig. 10 Peak value of the main harmonics of the proposed converter under load variation

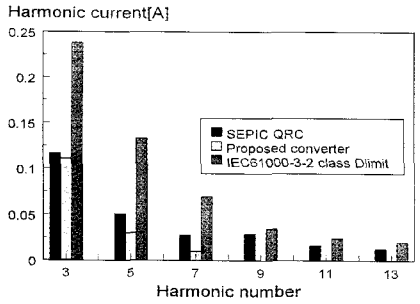

그림 11 P_o= 70W에서 SEPIC QRC와 제안된 컨버터의 고조파 전류

Fig. 11 Harmonic currents of SEPIC QRC and the proposed converter at P_o= 70W

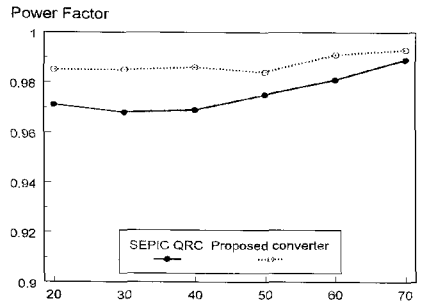

그림 12 SEPIC QRC와 제안된 컨버터의 역률

Fig. 12 Power Factor of SEPIC QRC and the proposed converter

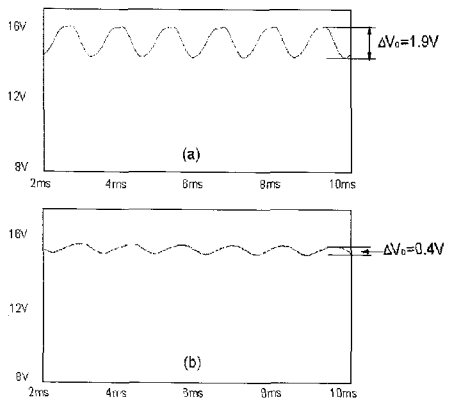

그림 13 P_o=70W에서 SEPIC QRC(a)과 제안된 컨버터(b)의 출력 전압 파형

Fig. 13 Output voltage waveforms of SEPIC QRC(a) and the proposed converter(b) at P_o=70W

under load variations are depicted in Fig. 9. It can be seen that THD of the proposed converter is lower than that of SEPIC QRC over entire load variations. The measured harmonic currents are shown in Figs. 10 and Fig. 11 shows that the 3rd harmonic current of the

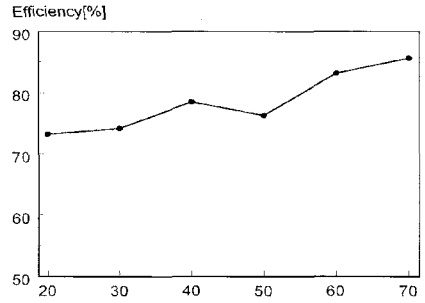

그림 14 제안된 컨버터의 효율

Fig. 14 Efficiency of the proposed converter

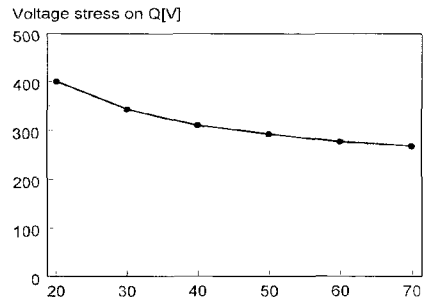

그림 15 부하변동시 주스위치 전압스트레스

Fig. 15 Voltage stress on the main switch under load variations

proposed converter is similar to that of SEPIC QRC, but the higher order harmonic currents are much lower or not even shown in the proposed converter. Fig. 12 shows the plot of the power factor as a function of output power in the two converters. As can be seen in this figure, due to the lower THD of the proposed converter compared with that of SEPIC QRC, the power factor of the proposed converter stays more higher. The computer simulations of the output voltage using the PSPICE are shown in Fig. 13. It shows that the output voltage ripple of SEPIC QRC is much larger than that of the proposed converter since the DCM current flowing in the input inductor is directly transferred to the output when the switch is turned off. This may result in a distortion of an input current waveform since the controller should have a high bandwidth to obtain a tight output regulation. Thus, a large output voltage ripple is not desirable characteristic in single-stage DCM PFC converters, especially at low voltage applications. Finally, the efficiency and the voltage stress on Q of the proposed converter under load variations are plotted in Figs. 14 and 15. These figures

show that this converter has the efficiency of about 86% at the rated condition and the maximum voltage stress is about 400V.

5. CONCLUSIONS

This paper has presented the analysis and experimental results of an integrated boost-flyback QRC for PFC operating in DCM. By eliminating the zero-point-distortion in the input current waveform, THD and power factor can be improved. Furthermore, the proposed converter is capable of producing the desired output voltage without a significant output voltage ripple. This is the desirable characteristic since the tight output regulation can be accomplished without the input current distortion using a high bandwidth output voltage controller. The designed prototype converter has a high power factor of above 0.985 and low THD compared with SEPIC QRC. Therefore, the proposed converter is suitable for a low power level converter with a tightly regulated low output voltage and a switching frequency of more than several hundreds kHz.

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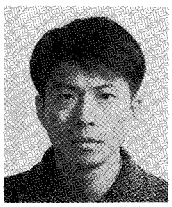

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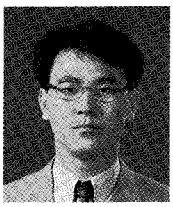

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