# Design of Real-Time Microvision for Edge Detection with Vertical Integration Structure of LSIs

## LSI 수직적층 구조를 가지는 윤곽검출용 실시간 마이크로 비젼의 설계

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**요 약** : 본 논문에서는, LSI 적층 기술을 이용한 실시간 처리 마이크로 비젼의 개발을 소개하고 있다. 새롭게 개발된 LSI 적층기술을 이용하여, 영상신호의 증폭, 변환, 연산처리등의 기본기능을 가지는 다수의 LSI 웨이퍼를 적층한다. 각 층간의 고밀도 수직배선을 통하여 대량의 영상정보를 동시에 전달하므로써, 대규모 동시 병렬처리를 가능하게 하며, 다수의 층에 걸쳐 파이프 라인 처리가 이루어진다. VLSI 설계시스템을 이용하여, 윤곽 검출기능을 가지는 테스트 칩을 설계(2 μm CMOS design rule)하고, 시뮬레이션을 통하여 양호한 동작(처리시간 10 μs)을 확인하고 있다. 시험제작을 위해서는, 새롭게 개발된 LSI 적층기술이 이용된다. 영상처리의 기본회로가 실려있는 웨이퍼의 기반을 30 μm의 두께까지 연마하고, 개발된 웨이퍼 aligner를 이용하여 수직배선이 형성된 상하 두 개의 웨이퍼를 미세조정하면서 접착한다. 이상의 제작과정을 반복하여 두께 1 mm이하의 인공망막과 같은 마이크로 비젼을 제작한다.

**Keywords** : real-time microvision, vertically integrated LSIs, circuit design, VLSI simulation

### I. Introduction

In intelligent robots which work in dynamic environment, it is desirable that the comprehension of dynamic task or environment and the generation of the appropriate action are carried out in real-time. For efficient visual servoing, it is known that the processing sampling rate of 100 $\mu s$ - 1 $ms$ is required in general. In addition, for tracking of ultra-high speed motion or analysis of ultra-high speed reaction, very fast real-time vision is needed.

However, in the conventional vision system, digital image processing and analysis have been performed using the conventional general-purpose computers in which programs and data are stored in the same memory unit and all operations are serially executed. As a result, the operations of two-dimensional (2D) image data arrays require a large amount of computing time which makes difficult to process and analyze image data in real time. A number of vision systems which tried to process and anlayze image information in real-time have been developed [1]. Some of them have partial parallel processing in software or hardware, but the sampling rate of the processing basically depends on the video rate of 33 $ms$ because of the systems using the conventional input devices. Trying to overcome these problems, some parallel architectures for image processing and the scale-up model of the massively parallel processing vision or one chip vision have been developed[1]-[4]. And some approaches in view of biology have been performed to realize the artificial eye[5]. However, it seems that the requirements of downsizing of the system and high speed operation of image data in real-time analysis of dynamic scene are not fully satisfied.

In this research, we design the microvision which has vertical integration structure and process the 2D image data arrays as the flow of 2D data arrays itself in parallel [6]. The basic concept of the real-time microvision is represented in Fig. 1. Each LSI layer has a basic function, such as, amplifying and converting image information signals and some arithmetic operations, etc. A number of LSI layers are fabricated vertically by the newly developed vertical integration technology. So, the data are transferred vertically using high density vertical interconnections. As a result, the microvision can be expected for dramatic improvement of the processing speed. The micro-vision is also expected for the vision system of mini or micro-robots because of its compactness. We design the test chip which plays edge detection using Laplacian operator. The circuit of photodetector, amplifiers and AD converters are designed in VLSI design system. Also the processor elements which provide simple arithmetic operations are designed by the method of wired logic control in VLSI design system. The circuits of the test chip are presented in the next section.

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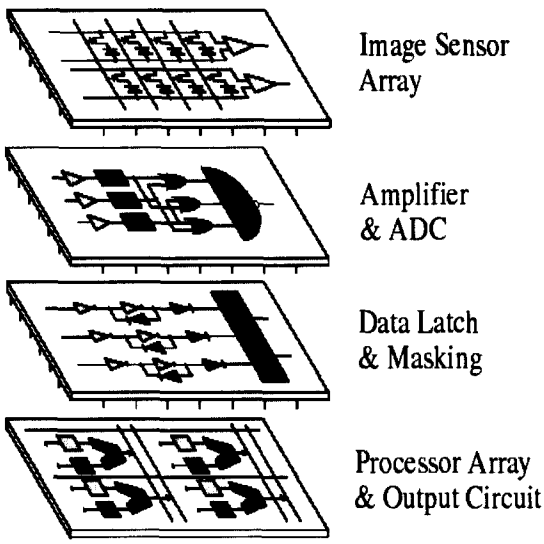


Fig. 1. Basic concept of real-time microvision with vertical integration structure of LSIs.

We have developed the new vertical integration technology of LSIs based on wafer bonding technique using micro-bumps to fabricate the microvision[7]. The Si substrate of the LSI which has the basic circuits is ground and polished to make a thin wafer. And the thinned wafer is aligned and bonded vertically onto a thick wafer by the vertical wafer aligner with the alignment tolerance of 1 $\mu m$. The microvision can be fabricated by repeating such sequence. The fabrication sequence of the microvision is introduced in a later section.

## II. System configuration and design

### 1. System configuration

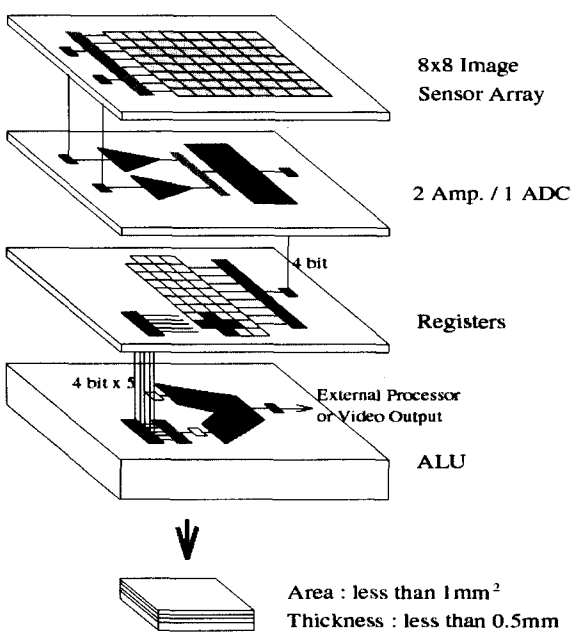


Fig. 2. Description of unit system.

The configuration of the unit system is represented in Fig. 2. The sixty-four (8 × 8) photodetectors are considered as a unit system. A number of unit systems are implemented depending on the scale of input image. Considering the device area of each LSI layer, we determine the corresponding ratio for devices between the respective layers as shown in Table 1.

Table 1. Configuration of unit system.

| Layer | No. of device |
|---|---|
| 1st layer | 8 x 8 photodetectors |
| 2nd layer | 2 amplifiers & 1 ADC |
| 3rd layer | 1 register |
| 4th layer | 1 ALU & output circuit |

The system consists of a number of LSIs vertically stacked using vertical integration technology introduced in section 4. Each LSI is connected vertically using the high density vertical interconnections. So, 2D image signals are transferred vertically at the same time and processed parallel in each LSI. The microvision has some processing parts. At first, the optical image signals are detected and converted to the electric signals. The electric signals are amplified, restored and modulated and so on. The manipulated electric signals are digitized, and some operations for the image informations are performed in the processor. Finally, the processed informations are transferred to a high level processors or some visual devices using 2D or 1D interconnections. The processing methods mentioned above are performed parallel in each LSI and in pipeline over all the LSI layers.

### 2. Design of test chip

We have designed the test chip using 2 $\mu m$ CMOS design rule which plays edge detection by Laplacian operator.

#### 2.1 Photodetectors

The 4 x 8 photodiodes are precharged and then charged by the acceptance of light. The charging rate is proportioned to the intensity of the light. The charged state of the photodiodes are stored in the capacitors. And then the stored electric charge in the capacitors are transferred sequentially to the amplifier.

#### 2.2 Amplifier and AD converter

The current mirror sense amplifier is adopted. The zero gain frequency is $3.35\times10^8$ *Hz*. The gain margin of the amplifier is about 2.6 *db* at the frequency of $4.06\times10^8$ *Hz*. It can be said that the amplifier is operated in stable. In the AD converter, the parallel conversion method is adopted. The four bit ADC with the conversion frequency of 25 *MHz* is implemented in the test chip.

#### 2.3 Registers

The block digram of the registers is represented in

Fig. 3. The registers have array of four bit D-flip flop in which the digitized value of input pixels with neighboring pixels of the verges are stored. The registers have two shift operation: the one shifts all the registers from the left to the right in turn (Shift H) and the other shifts right three columns of the registers from the bottom to the top in turn (Shift V). Combining the two shift operations, we shift the registers which are the candidate of the operation to the center of the gray regions with the neighboring registers in turn. The gray regions of the registers are transferred to the arithmetic logic unit (ALU) by the multiplexer.

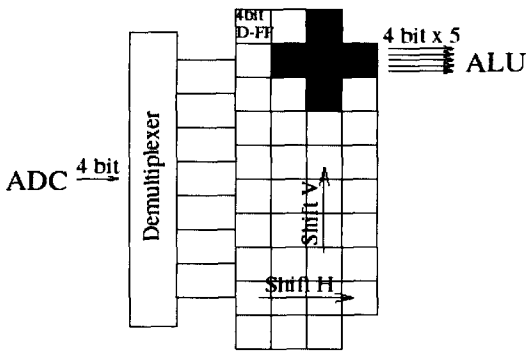


Fig. 3. Registers.

2.4 ALU

The ALU consists of carry lookahead adder, register, counter and multiplexer. The operation time of the carry lookahead adder is 13 *ns*. The ALU plays the edge detection using the Laplacian operator. The Laplacian operator based on the 2nd derivative detects the peak of the density change. For the pixels of 4-neighborhood, the Laplacian operator takes the following operation:

$$g(i,j) = f(i,j-1)+f(i-1,j)+f(i+1,j)+f(i,j+1)-4f(i,j)$$

where $g(i,j)$ is the operation result of the pixel $f(i,j)$. In the processor, the wired-logic control method is adopted for high speed operation. In practical application, Laplace of Gaussian (LoG) filter may be more effective for the edge detection. But in the test chip, Laplacian filter is used to simplify the circuit in the processor.

2.5 Parallel and pipeline processing

The configuration of the unit system is shown in the previous section. In application, a number of the unit systems are implemented in the vision system depending on the scale of input image. The interconnections of the multi-processor system which have four processor elements are shown in Fig. 4. The sixty four (4×16) line and eight (4×2) line buses are used for the interconnections of the multi-processor system to transfer the data each other. Using the interconnections, the neighboring pixels' data of the verges of each processor element are transferred for the 4-neighborhood Laplacian operation. In the unit system, two pipeline stages are performed as shown in Fig. 5. The first stage is the photo detection, the amplifying and the AD conversion. The second stage is the manipulation of the register and the operation in the ALU.

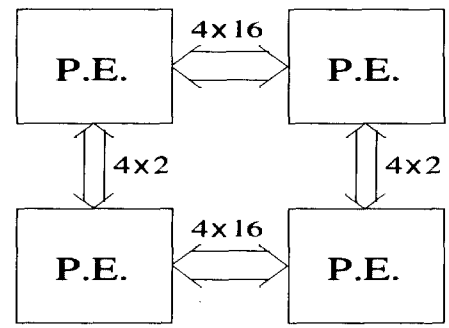


Fig. 4. Multi-processor system of test chip with four unit systems.

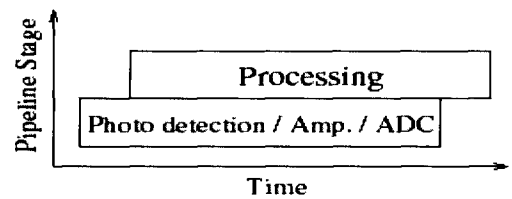


Fig. 5. Pipeline process.

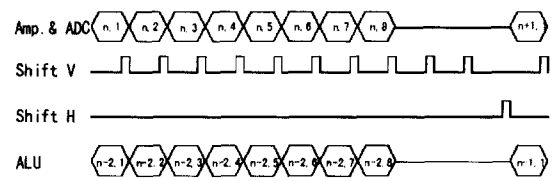


Fig. 6. Timing of operation.

## III. Simulation

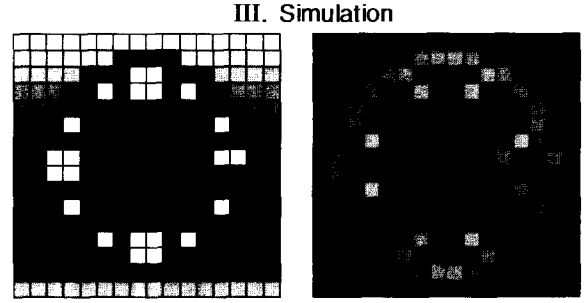


Fig. 7. Example of edge detection.

The timing of operation in the unit system is represented in Fig. 6. Considering the photodetector array as a matrix, the (n-2)th row data is operated in

the ALU when the n-th row data is processed in the amplifier and the ADC. The timing of operation shows the processing of the two pipeline stages. The simulation result of the edge detection for multi-processor system which has four unit systems is represented in Fig. 7.

By investigating the numerical results of the gray revel image, we can see that the operation of the edge detection is carried out successfully. The processing time of the edge detection takes about 10 $\mu s$. This result shows the significant improvement of the processing speed of the microvision comparing the conventional ones[1]-[4]. By using the advanced CMOS technology, we can reduce the processing time moreover.

## IV. Fabrication

In the past, the laser recrystallization technique is a leading candidate for 3D LSIs [8]. Also the 3D-LSI image processor which recognizes some letters had been developed using the method [9]. However, the 3D-LSI technology had not been employed in production because it was very complicated and expensive technology. In this paper, we propose more realistic vertical integration technology of LSIs based on wafer bonding technique using micro-bumps [7]. The process sequence to fabricate the microvision with vertical integration structure is shown in Fig. 8. At first, a LSI wafer with buried interconnections are prepared to

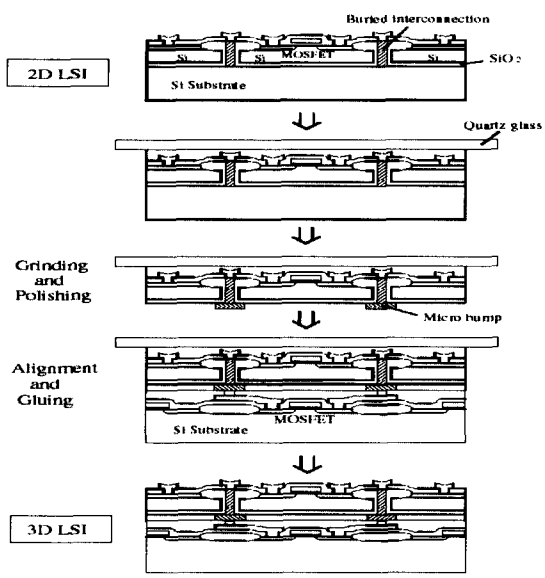


Fig. 8. Fabrication sequence of vertically integrated LSIs.

fabricate the microvision. The buried interconnections are used for vertical transfer of the data between the two LSIs. The buried interconnections are formed by depositing $n^+$ poly-Si into trenches which are formed through the field oxide. The LSI wafer with buried

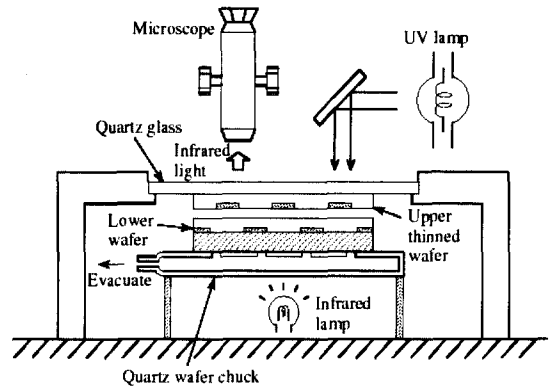


Fig. 9. Schematic diagram of wafer aligner for vertical integration.

interconnections is glued to a quartz glass and then thinned to around $30\mu m$ by grinding and chemical mechanical polishing. For a wafer alignment, we have developed a new wafer aligner as shown in Fig. 9. Wafer stage is precisely controlled with accuracy of 50 $nm$ in x,y,z directions by piezo actuators in the aligner. Six inch wafers can be aligned with the alignment tolerance of 1 $\mu m$. The thinned wafer is bonded to a thick wafer using In/Au micro-bumps with the minimum size of 5 $\mu m$ × 5 $\mu m$ and UV hardening adhesive layer with thickness of 1 $\mu m$ by forcing the z direction pressure after careful wafer alignment. We can monitor the wafer alignment through the ten layers using the infrared light equipped in the bottom of the aligner. The gap between two wafers are measured in-situ and precisely controlled during alignment. By repeating above sequence, the microvision with vertical integration structure can be fabricated. Good electrical contact was obtained between two micro-bumps after bonding by optimizing the micro-bump and bonding conditions. In the stacking of a number of LSI wafers, the problem of heat exhaust will be occur and may limit the number of wafers to be stacked. To overcome the problem, we consider the low power consumed circuit in the design of each LSI. In this chapter, the fabrication sequence was summarized. Some basic technologies, such as, thinning the wafer, burying the vertical interconnections and alignment were developed already. The fabrication of the test chip is planned using the developed basic technologies.

## V. Conclusion

The development of the real-time microvision with massively parallel processing structure was introduced. By stacking a number of LSIs vertically, we can process and transfer 2D image informations as it is through the high density vertical interconnections. In the microvision, the image informations are processed parallel in each layer and the processings are performed

in pipeline over all the layers. In CAD simulation of the edge detection using Laplacian filter, the good operation was obtained and the processing time takes about 10 $\mu s$ using 2 $\mu m$ CMOS design rule. The microvision is expected for the dramatic improvement of the processing speed comparing the conventional vision system using CCD sensor because the microvision has the massively parallel processing structure. Also the microvision is fabricated with the thickness of less than 1 $mm$ such as artificial retina using the newly developed vertical integration technology of LSIs.

In the practical application, such as, target tracking or pattern recognition, the additional image processing using external processors will be needed. Nevertheless, the improvement of the processing speed in pre-processing of image plays a significant role in realization of the real-time vision.

As a future work, we will design and fabricate the general purpose microvision which has the functions of local image processing, feature extracting and target tracking. By stacking a number of LSI wafers which have the various functions of image processing, we can make the general purpose microvision which have the input pixels of $640 \times 480$ for practical application.

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