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IGBT 인버터를 위한 향상된 단락회로 보호기법

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An Improved Short Circuit Protection Scheme for IGBT Inverters

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ABSTRACT

Identification of fault current during the operation of a power semiconductor switch and activation of suitable remedial actions are important for reliable operation of power converters. A short circuit is a basic and severe fault situation in a circuit structure such as voltage source converters. This paper presents a new active protection circuit for fast and precise clamping and safe shutdown of fault currents of the IGBTs. This circuit allows operation of the IGBTs with a higher on-state gate voltage, which can thereby reduce the conduction loss in the device without compromising the short circuit protection characteristics. The operation of the circuit is studied under various conditions, considering variation of temperature, rising rate of fault current, gate voltage value, and protection circuit parameters. An evaluation of the operation of the circuit is made using IGBTs from different manufacturers to confirm the effectiveness of the protection circuit.

Key Words: Fault current, fault under load, hard switched fault, IGBTs, protection, short circuit.

1. Introduction

Short circuit and over-current are severe fault conditions that can result in failure of the IGBT if appropriate remedial action is not taken within a short time of the order of a few microseconds. It is shown in [1] that the internal failure mechanism in IGBTs during short circuit is different from the case of hard switching inductive turn-off failure. Short circuit results in local heating closer to the gate oxide in the IGBT and can severely degrade the device. The excessive power dissipation in the IGBT during the fault leads to chip heating, which eventually destroys the device. Several methods for protection of the IGBT are available that are used in intelligent power modules and advanced gate driver chips [2]-[4]. However, there are no benchmarks for the performance of these circuits.

Various approaches to protect IGBTs have been proposed and studied in [5]-[12]. Different topologies for fault current limiting circuits (FCLCs) have been investigated in [5], [6]. The technique used in [5], which utilizes a capacitor to reduce the gate voltage after the fault, has the limitation that the device current may shut off and be turned back on again depending on the initial condition of the capacitor and its value. Also, a large value of capacitance is necessary to prevent the capacitor voltage from drifting back to the normal on-state gate voltage. Multiple stages of clamping are proposed in [5] to increase the endurance time and reduce the turn-off current level. A pure zener based clamp has the drawback that the clamping gate voltage can be much larger under the transient conditions of the fault. Reference [6] discusses a topology where the zener and capacitive method is used to limit fault currents. This circuit is effective in eventually clamping the fault current level but does not limit the large peak

current that flows immediately after the fault due to delay in its operation. References [7]-[12] discuss methods to softly turn off the IGBT after the fault and to reduce the over-voltage due to the turn-off di/dt. The purpose is to control the over-voltage caused by the parasitic inductance of the power circuit while turning off large currents.

This paper focuses on the following study issues for active protection of fault currents for IGBT modules:

· Use of a large on-state gate voltage to reduce conduction losses makes the fault situation more problematic and dangerous, because it leads to very high fault current. This results in large instantaneous power dissipation [13] and the possibility of latching in the device. Therefore, there is a trade-off between the short circuit current magnitude and the conduction loss;

· Precise detection of fault current levels is a challenging issue if current sensors are not used in series with the IGBTs. In particular, in case of large fault inductance (soft fault) it is difficult to precisely recognize the over-current condition using the de-saturation technique, which is a common method used to identify a fault situation. This is due to the reduced voltage drop in the IGBT under low di/dt conditions as well as the slow dynamics in the electronic components in the detection circuit;

· Fast detection and reliable handling of fault currents are important study issues. The initial value of short current is the highest due to the increased gate voltage caused by the Miller capacitance. It is not easy to reduce the initial peak current, because activation of protection circuit should be prevented during the turn-on transient conditions of the IGBT, and during noise phenomena caused by the IGBTs switching in the power converter;

· At shutdown, the falling rate of the current should be controlled to reduce the over-voltage stress. The over-voltage level across the device can become much larger than the rated voltage, if the large collector current is turned off without any treatment. While using a FCLC, soft turn-off requires to take into account possible changes in the operating modes of the protection circuit.

For the study mentioned above, experimental investigation on the fault situation is performed in detail for the cases of variation of temperature, rising rate of fault current, positive gate voltage level, and circuit parameters. A new active protection method is proposed to limit fault currents to a reasonable level while suppressing the initial peak current value and safely shut down the IGBT. Test results are given by using IGBTs from different manufacturers to study operation of the protection circuit under varying device parameters.

2. Operation Characteristics of The Proposed Active Protection Circuit

Fast detection of the occurrence of the fault, limiting of the initial peak current, clamping of the over-current, and safe shutdown are essential features of the protection circuit. The types of short circuit faults that can occur in an IGBT can be classified as hard switched fault (HSF) and fault under load (FUL) [14]. HSF occurs when the IGBT tries to turn-on into a short circuit. FUL is the case where the short circuit occurs when the IGBT is in the on-state conducting normal load current. Fig. 1 shows the schematic of the proposed circuit, which is composed of the basic drive circuit, the additional protective control circuit, and the three feedback lines, which are collector voltage detection,

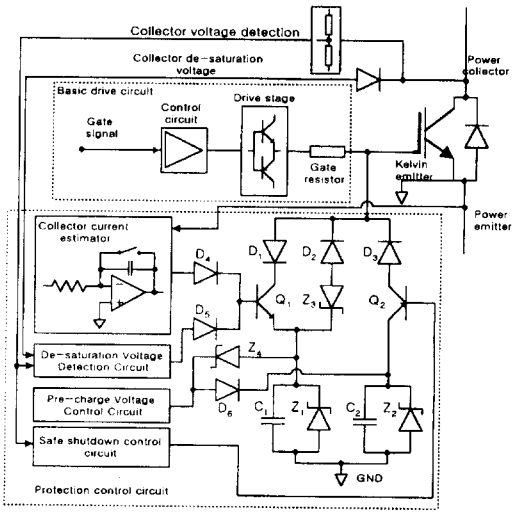


Fig. 1 Schematic diagram of the proposed protection circuit.

collector de-saturation voltage, and power emitter voltage. Functions and operational characteristics of the circuit are explained.

2.1 Detection

The detection of fault current is based on two inputsinto the protection control circuit. One is the collector to emitter voltage of the device of the IGBT, which is a function of the collector current in the device. A diode is used to clamp this voltage below the positive gate drive power supply voltage, and is called the collector de-saturation voltage. The other is the voltage drop between the power and the Kelvin emitter terminal of the device. In an IGBT module the Kelvin emitter terminal is available externally, because the gate signal is applied between the gate and Kelvin emitter terminals. If we look at the voltage between the power emitter and the Kelvin emitter, we can monitor the voltage drop in the connection inductance between the external power emitter terminal and its internal semiconductor contact, which is caused by the collector current. Here, the Kelvin emitter terminal can be considered as the semiconductor contact point. The inductance is of the order of a few nano-henries and becomes larger in higher power modules due to longer distances between the semiconductor and the power emitter terminal. This allows an estimate of the IGBT collector current level, which is obtained using a resetable integrator circuit shown in Fig. 1. The parameters of the integrator are based on the connection inductance between the two emitter terminals, the loading of the integrator circuit, and parasitic capacitance of the reset switch. The de-saturation voltage detection has a rapid response to low impedance (hard fault) FUL condition. The device current estimator is more effective in detecting soft fault situations. Direct measurement circuit of the collector voltage, which is added to collector feedback line in Fig. 1, is used to rapidly recognize HSF condition and to distinguish it from normal switching transients of the IGBT[12].

2.2 Limiting

Limiting of the current is obtained using the capacitor, C_1, and the zener diode, Z_1, for fast and stable protection. On detection of the fault the transistor, Q_1, is turned on, which causes C_1 to charge up to the voltage level of Z1, thus discharging the gate. The transistor is activated by the combination of the collector current estimate and the de-saturation voltage, which is obtained using diodes D_4 and D_5. A large C_1 results in initial oscillation in the device current and a slow ramp up to the clamp current level. A small value of C_1 results in an increased peak fault current due to insufficient gate discharge. The zener diodes, Z_3 and Z_4, make the voltage of C_1 be at the desired voltage level before turning on the IGBT. This pre-charge voltage compensates for the delay in operation of the protection circuit. A lower pre-charge voltage will result in the activation of the protection circuit at an earlier instant. The on-state voltage of the IGBT and the voltage drop along the de-saturation detection circuit limit the minimum value of the pre-charge voltage.

2.3 Clamping

The final gate voltage level is clamped by the zener Z_1. The value of the zener voltage is selected to be above the threshold voltage and depends on the transconductance gain of the driven IGBT. The voltage drops across the transistor, Q_1, and the diode, D_1, have to be considered while selecting the zener diode, Z_1. The clamped gate voltage decides the clamped level of fault current.

2.4 Shutdown

The capacitor C_2 is placed in parallel with the gate capacitance to turn off the IGBT at a reduced dVge/dt. The collector voltage detection signal provides information to the power converter control circuits about occurrence of the fault and initiates the safe shutdown. The current path changes from D_1-Q_1-Z_1 during clamping mode to C_2-Q_2-D_3 during shutdown. The pre-charge level of C_2 is higher than the gate voltage level used for clamping due to the voltage drop corresponding to the conducting paths of the shutdown circuit. This eliminates the small notch in gate voltage caused by the reversal of current from the clamping mode to the safe shutdown mode. The purpose of the diode, D_6, is to obtain decoupling between the pre-charge voltage levels for C_1 and C_2. The zener diode, Z_2, determines the pre-charge level of C_2.

2.5 Fault Monitoring

Nuisance faults signals can be rejected strongly because the main fault signal sent to the system controller occurs based on the measured Vce information. Also, a delay time of a few microseconds is used to report the fault information allowing for momentary transient in the current that could occur without damaging the device. These momentary transients are also held to the clamping current level.

3. Experimental Evaluation

A simple test circuit is set up to verify the validity of the proposed protection circuit, which is shown in Fig. 2. A two-pulse method has been used to drive the IGBT with an inductor as the load. The controlled time duration for the first pulse is required to obtain the desired load current, which would be the initial value at turn-on of the second pulse. In order to test FUL conditions, the short circuit control switch in Fig. 2 is turned on while the DUT is in on-state and is conducting load current during the second pulse. On the other hand, for HSF test, the short circuit control switch is already turned on before the second pulse activates the DUT. The test has been conducted with three different dual IGBT modules: IGBT1 - Toshiba MG100Q2YS40 (1200V, 100A), IGBT2 - Powerex CM75DY-12H (600V, 75A), and IGBT3 - Fuji 2MBI75-060 (600V, 75A). The measured collector current, collector voltage, and gate voltage waveforms for IGBT1, and graphs of the peak current and the clamped current levels for IGBTs 2 and 3 for the cases of with and without protection are shown.

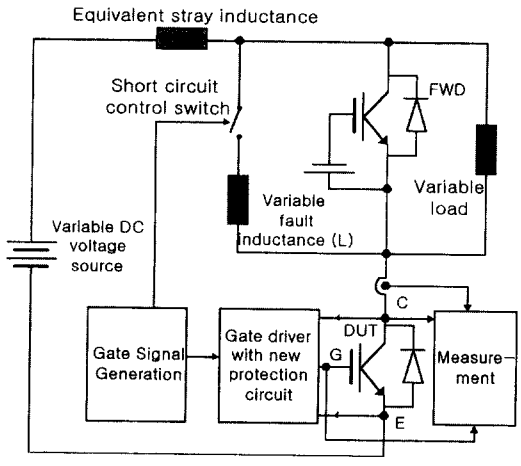


Fig. 2 Test setup.

3.1 On-State Gate Voltage Variation

Figs. 3(a) and (b) show the test results of FUL while varying the on-state gate voltage, which is the parameter studied during this test. In case of no protection shown in Fig. 3(a), the peak and the final current levels are strongly dependent on the gate voltages. When the on-state gate voltage is 19V, the peak current is more than fifteen times of the rated current. There is not much difference in the Vce waveform. From Fig. 3(b) it can be seen that fault currents are at controlled levels irrespective of the on-state gate voltage with the active protection circuit.

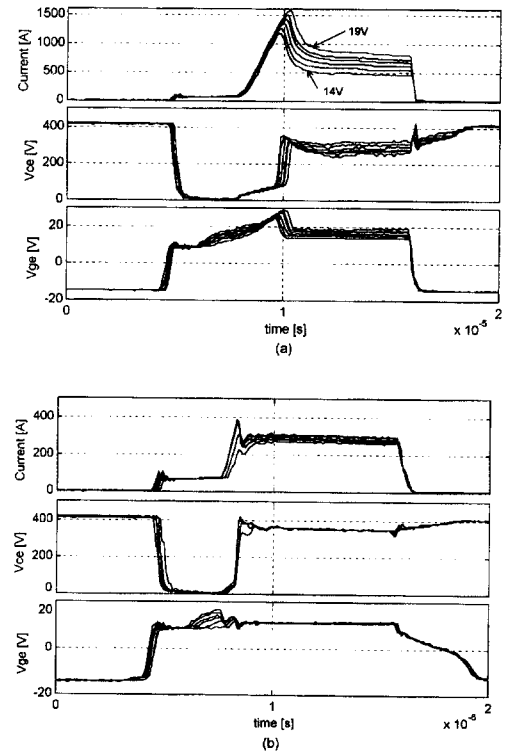


Fig. 3 FUL test results for IGBT1 under Vge variation. (a) Without protection. (b) With protection. Selected positive gate voltages are as follows: 14, 15, 16, 17, 18, 19V. Other conditions are as follows: C_1 = 30nF, Pre-charge voltage = 4.5V, V_{dc} = 405V, T = 24℃, L = 200nH.

Figs. 4(a) and (b) are for the case of HSF. Fig. 4(b) shows that the protection circuit keeps fault currents within a small envelope for a wide range of the on-state gate voltage levels as in the case of FUL. On the other hand, from Fig. 4(a), it is shown that the peak and the final current levels increased by a factor of two when the gate voltage was increased from 14V to 19V. The waveforms in Figs. 3(b) and 4(b) use the selected values of C1 and the pre-charge voltage that result in optimal characteristics of the protection circuit. Trade-off involved when these parameters are changed is explained in the following sections D and E. The graphs of the key parameters, while using IGBTs 2 and 3, are shown in Figs. 5(a) and (b), respectively. The use of the active protection shows that a significantly lower fault current level can be achieved irrespective of the gate voltage for all the IGBTs.

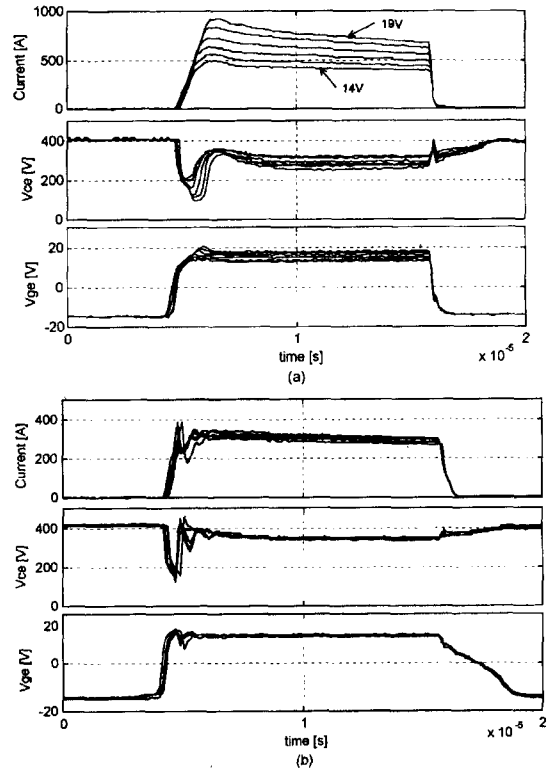
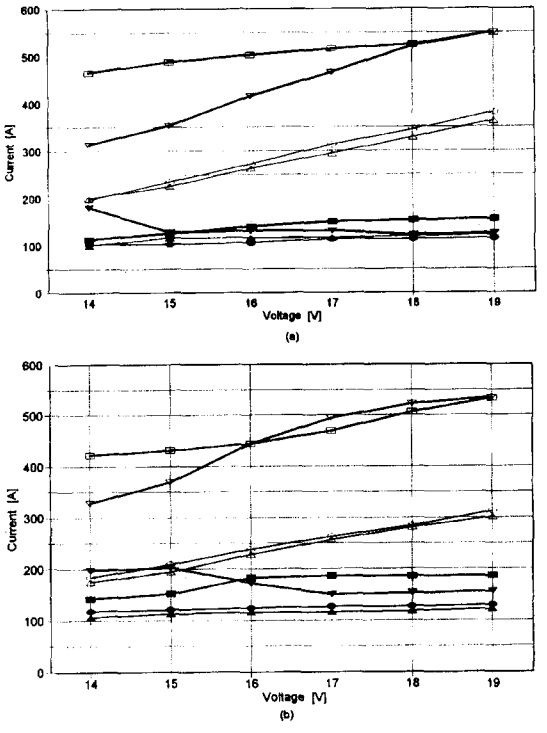


Fig. 4 HSF test results for IGBT1 under Vge variation. (a) Without protection. (b) With protection. Selected positive gate voltages are as follows: 14, 15, 16, 17, 18, 19V. Other conditions are as follows: C_1 = 60nF, Pre-charge voltage = 5V, V_{dc} = 405V, T = 24℃, L = 200nH.



Peak fault current under FUL without protection, peak fault current under HSF without protection, clamped current level under FUL without protection, clamped current level under HSF without protection, peak fault current under FUL with protection, peak fault current under HSF with protection, clamped current level under FUL with protection, clamped current level under HSF with protection.

Fig. 5 Effect of variation of on-state gate voltage on fault parameters. (a) Use of IGBT2 with the operating conditions - FUL: C_1 = 30nF, pre-charge = 5V; HSF: C_1 = 20nF, pre-charge = 3.45V; V_{dc} = 405V, T=24℃, L = 200nH. (b) Use of IGBT3 with the operating conditions - FUL: C_1 = 60nF, pre-charge = 5V; HSF: C_1 = 30nF, pre-charge = 6V; V_{dc} = 405V, T= 24℃, L = 200nH.

3.2 Temperature Variation

Figs. 6 and 7 show the effect of operating temperature on IGBT1 for FUL and HSF, respectively. The temperature is the measured at the baseplate of the IGBT. During the fault the chips in the module heat rapidly but the baseplate stays at approximately a constant temperature. The peak and the final fault

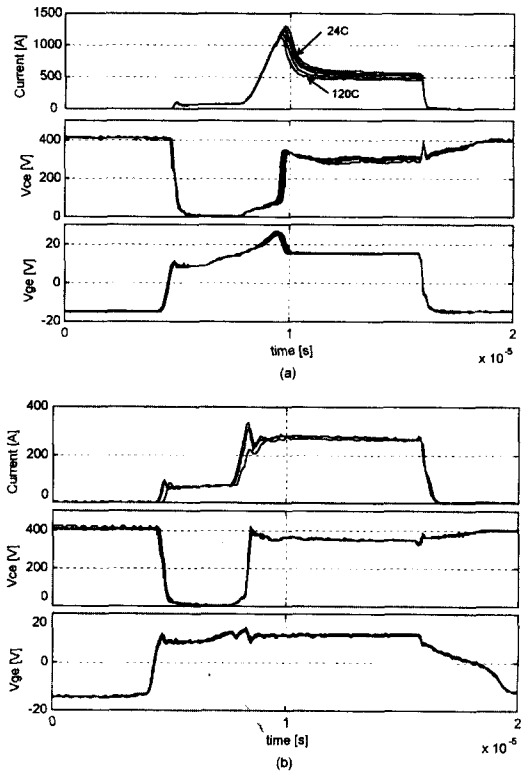


Fig. 6 FUL test results for IGBT1 under variation of temperature. (a) Without protection. (b) With protection. Selected temperatures are as follows: 24, 40, 60, 90, 120℃. Other conditions are as follows: C_1 = 60nF, Pre-charge voltage = 5V, V_{dc} = 405V, V_{ge} = 15V, L = 200nH.

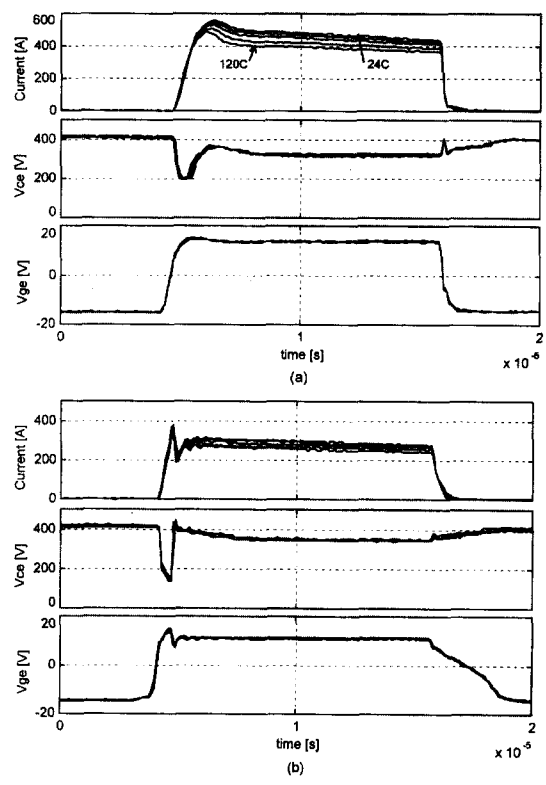
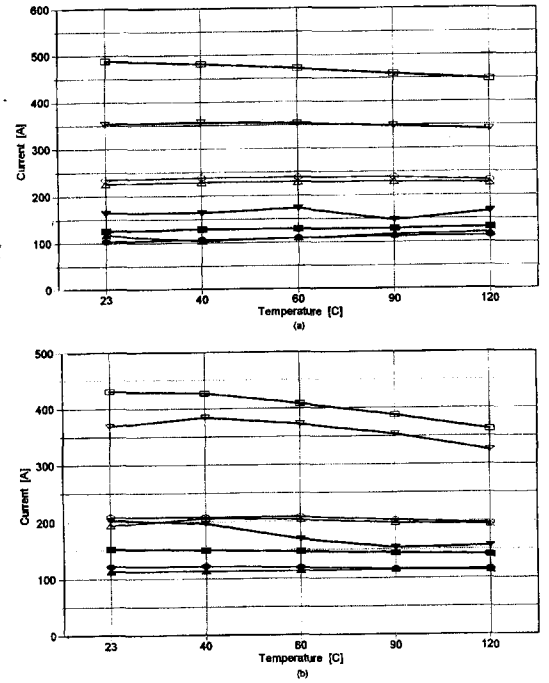


Fig. 7 HSF test results for IGBT1 under variation of temperature. (a) Without protection. (b) With protection. Selected temperatures are as follows: 24, 40, 60, 90, 120℃. Other conditions are as follows: C1 = 30nF, Pre-charge voltage = 4.5V, Vdc = 405V, Vge = 15V, L = 200nH.

current decrease as the temperature is increased due to the negative temperature coefficient at high current levels. This result indicates that within the normal operating temperature range, the fault current waveform does not vary significantly if the device is turned off in a short time. When the active protection circuit is applied, the effect of temperature is reduced. Thus the impact of fault on the device becomes much smaller. The graphs of the main fault current parameters for IGBTs 2 and 3 are shown in Figs. 8(a) and (b), respectively. The negative temperature coefficient is a desirable characteristic during the fault.

3.3 Fault Inductance Variation

For this test, the variable fault inductance (L), which is shown in Fig. 2, is used to obtain the inductance values of 0.2, 2.5 and 4.5uH. Fig. 9(a) shows that the peak fault current is largest for small fault inductance in case of FUL. As fault inductance decreases, it is necessary for the protection circuit to have a quick reaction to prevent the high peak current. As fault inductance increases, pure de-saturation based fault detection would have a large delay in operation. Therefore, it would not be possible to limit the peak fault current and to estimate the exact fault current level without using a current sensor. On the other hand, in the case of HSF shown in Fig. 10(a), the peak fault current increases as the fault inductance is increased. Therefore, it is difficult to exactly recognize fault conditions at similar current level for both cases.



Peak fault current under FUL without protection, peak fault current under HSF without protection, clamped current level under FUL without protection, clamped current level under HSF without protection, peak fault current under FUL with protection, peak fault current under HSF with protection, clamped current level under FUL with protection, clamped current level under HSF with protection.

Fig. 8 Effect of variation of temperature on fault parameters. (a) Use of IGBT2 with the operating conditions - FUL: C_1 = 30nF, pre-charge = 5V; HSF: C_1 = 20nF, pre-charge = 3.45V; Vdc = 405V, V_{ge} = 15V, L = 200nH. (b) Use of IGBT3 with the operating conditions - FUL: C_1 = 60nF, pre-charge = 5V; HSF: C_1 = 30nF, pre-charge = 6V; V_{dc} = 405V, V_{ge} = 15V, L = 200nH.

The proposed active protection circuit can detect and limit the fault current at the same level not only for a wide range of fault inductance but also for both FUL and HSF as shown in Figs. 9(b) and 10(b). The graphs of the fault current parameters for IGBTs 2 and 3 are shown in Figs. 11(a) and (b), respectively. The trend in all the cases without protection is similar, indicating a

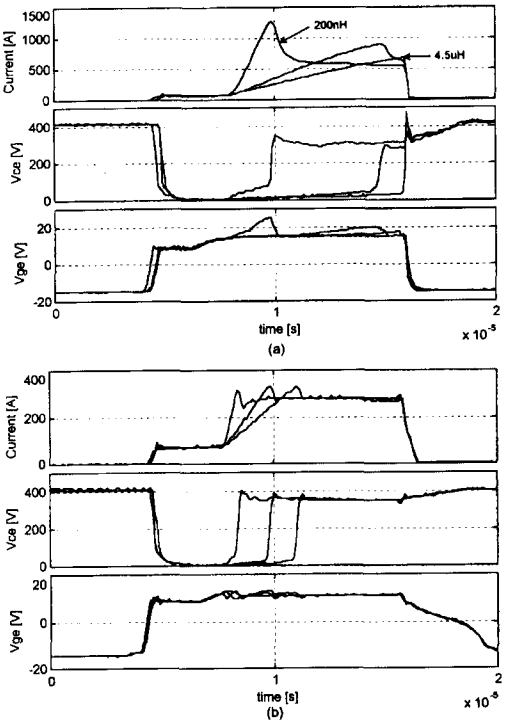


Fig. 9 FUL test results for IGBT1 under variation of inductance. (a) Without protection. (b) With protection. Selected inductances are as follows: 0.2, 2.5, 4.5uH. Other conditions are as follows: C_1 = 60nF, T = 24℃, Pre-charge voltage = 5V, V_{dc} = 405V, V_{ge} = 15V.

reduction in the difference between the collector current levels for FUL and HSF as the fault inductance is increased.

3.4 Circuit Parameter, C1, Variation

Figs. 12(a) and (b) show the effect of variation of the capacitor, C_1, which is designated in Fig. 1, on the response of the protection circuit for FUL and HSF. A large C_1 results in the device current reaching almost zero and then slowly building up to the clamped current level. A small C1 is not effective in discharging the gate capacitance rapidly and results in a higher initial peak in fault current. Figs. 13(a) and (b) show the influence of C_1 on the performance of the protection circuit for IGBTs 2 and 3. It can be seen from the graph that the variation of capacitance has a greater effect on limiting

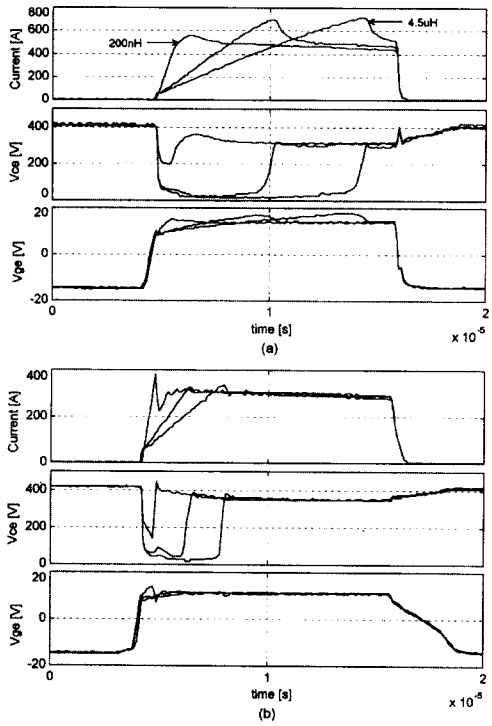
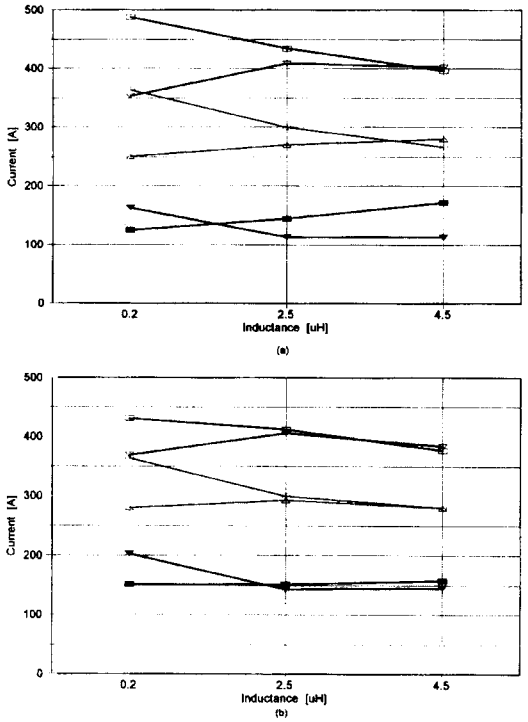


Fig. 10 HSF test results for IGBT1 under variation of inductance. (a) Without protection. (b) With protection. Selected inductances are as follows: 0.2, 2.5, 4.5uH. Other conditions are given as follows: C_1 = 30nF, T = 24℃, Pre-charge voltage = 4.5V, V_{dc} = 405V, V_{ge} = 15V.



Peak fault current under FUL without protection, peak fault current under HSF without protection, clamped current level under FUL without protection, clamped current level under HSF without protection, peak fault current under FUL with protection, peak fault current under HSF with protection

Fig. 11 Effect of variation of fault inductance on protection circuit performance. (a) Use of IGBT2 with the operating conditions FUL: C_1 = 60nF, pre-charge = 5V; HSF: C_1 = 20nF, pre-charge = 3.45V; V_{dc} = 405V, T = 24℃, V_{ge} = 15V. (b) Use of IGBT3 with the operating conditions FUL: C_1 = 60nF, pre-charge = 5V; HSF: C_1 = 30nF, pre-charge = 6V; V_{dc} = 405V, T = 24℃, V_{ge} = 15V.

the peak current levels in case of FUL than HSF. This is because of the larger delay in activation of the protection circuit in case of HSF. Also, the variation of C_1 does not affect the clamped current level, which is determined by the zener, Z_1.

3.5 Pre-charge Voltage Variation

Figs. 14(a) and (b) show the effect of the pre-charge voltage level on the response of the protection circuit for FUL and HSF, respectively. It can be seen that lowering the pre-charge voltage is effective in lowering the initial peak in fault current. The pre-charge voltage variation has a greater effect on FUL than HSF. This is because of the need to have a minimum delay before activation of the de-saturation detection circuit. Advancing the activation of the protection circuit by using the measured Vce voltage can minimize this effect. Similar results obtained for IGBTs 2 and 3 are shown in the graphs of Figs. 15(a) and (b), respectively.

3.6 Peak Power and Energy Dissipation

Table 1 lists a comparison of the peak power and the energy dissipation between the cases of with and without the active protection circuit, for FUL and HSF

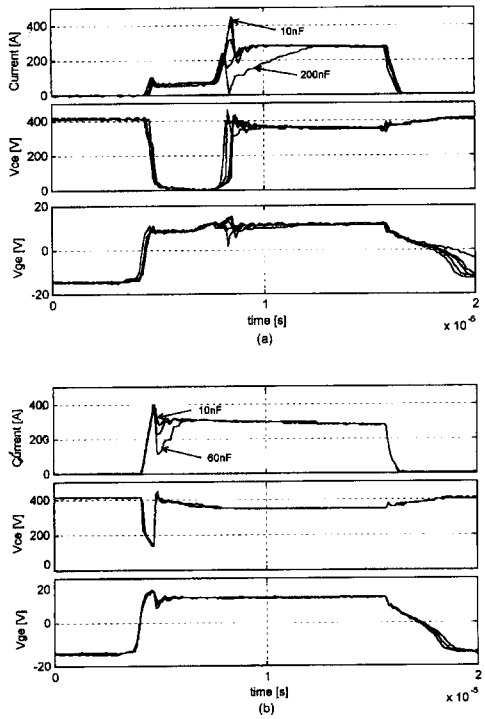
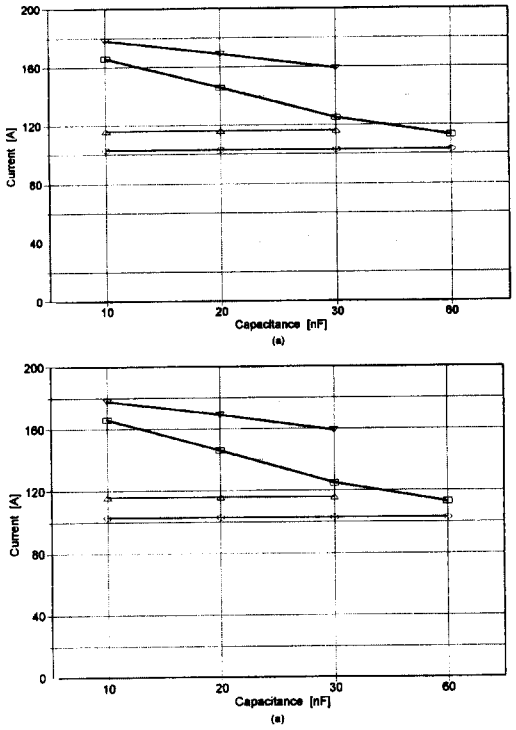


Fig. 12 Test results for IGBT1 under variation of capacitance, C_1. (a) FUL with selected capacitance as follows: 10, 30, 60, 100, 200nF. Pre-charge is at 4.8V. (b) HSF with selected capacitance as follows: 10, 30, 60nF. Pre-charge is at 5.0V. Other conditions are given as follows: Fault inductance = 200nH, T = 24℃, V_{dc} = 405V, V_{ge} = 15V.

Table 1 Peak power and Energy dissipation in the IGBTs with and without protection (Energy dissipation is normalized to 1.0 for operation without protection. Other conditions are : $V_{ge\ on}$ = 15V, V_{dc} = 405V, T = 24℃, L* = 200nH.)

Device	FUL		HSF	
	w/o[kW]	w[kW]	w/o[kW]	w[kW]
IGBT1 MG100Q2YS40	423 (1.0)	110 (0.59)	210 (1.0)	125 (0.73)
IGBT2 CM75DY-12H	178 (1.0)	44.3 (0.46)	135 (1.0)	62.0 (0.48)
IGBT3 2MBI75-060	156 (1.0)	55.9 (0.45)	145 (1.0)	82.5 (0.58)

*L is the fault inductance shown in Fig. 2.



Peak fault current under FUL without protection, peak fault current under HSF without protection, clamped current level under FUL without protection, clamped current level under HSF without protection,

Fig. 13 Effect of variation of protection capacitor, C1, on fault parameters. (a) Use of IGBT2 with the operating conditions - FUL: pre-charge = 4.55V; HSF: pre-charge = 3.45V; L = 200nH, T = 24℃, V_{ge} = 15V, V_{dc} = 405V. (b) Use of IGBT3 with the operating conditions - FUL: pre-charge = 5.9V; HSF: pre-charge = 6V; L = 200nH, T = 24℃, V_{ge} = 15V, V_{dc} = 405V.

for three different IGBTs. Under the given operating conditions, the peak power dissipation is reduced by a factor of 3 for FUL and by a factor of 1.8 for HSF on an average value by using the active protection circuit. The energy dissipation is reduced by a factor of 0.5 on an average. The reduction of power dissipation improves the ability of the device to endure the fault. This allows for better low pass filtering of the fault signals and can lead to improved noise immunity.

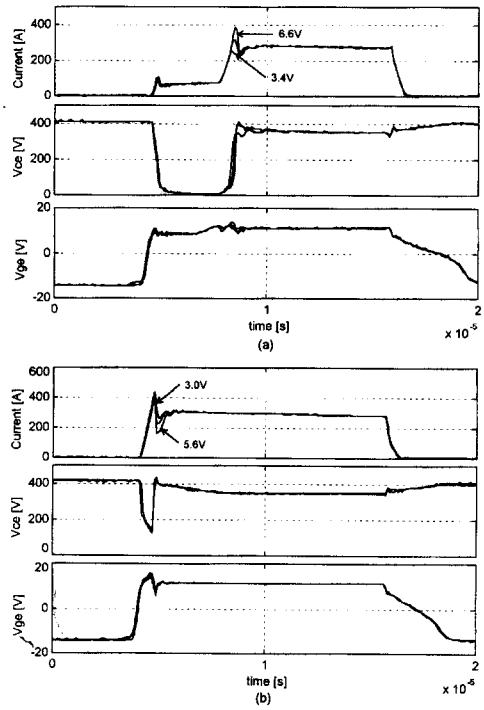
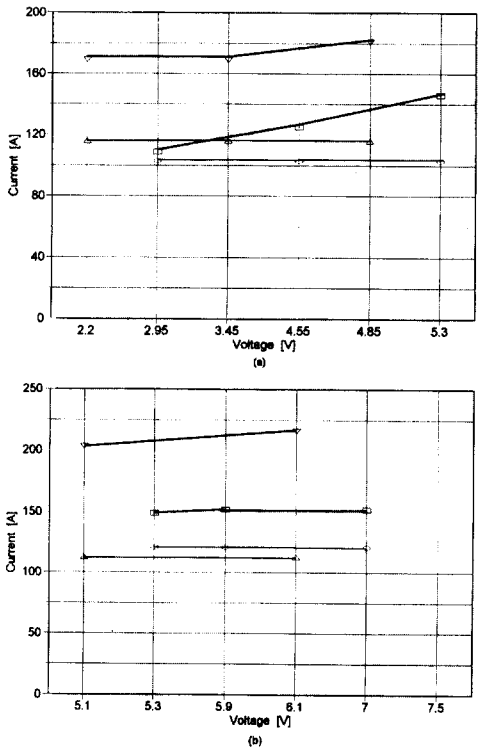


Fig. 14 Test results for IGBT1 under variation of C_1 pre-charge voltage. (a) FUL with selected pre-charge voltage values as follows: 3.4, 4.8, 6.6V. C_1 is 60nF. (b) HSF with selected pre-charge voltage values as follows: 3.0, 4.0, 5.6V. C_1 is 30nF. Other conditions are given as follows: Fault inductance = 200nH, T = 24℃, V_{dc} = 405V, V_{ge} = 15V.



Peak fault current under FUL without protection, peak fault current under HSF without protection, clamped current level under FUL without protection, clamped current level under HSF without protection,

Fig. 15 Effect of variation of pre-charge voltage of C_1 on fault parameters. (a) Use of IGBT2 with the operating conditions - FUL: C_1 = 30nF; HSF: C_1 = 20nF, L = 200nH, T = 24℃, Vge = 15V, V_{dc} = 405V. (b) Use of IGBT3 with the operating conditions - FUL: C_1 = 60nF; HSF: C_1 = 30nF; L = 200nH, T = 24℃, V_{ge} = 15V, V_{dc} = 405V.

4. Conclusion

This paper has shown a new active protection circuit for IGBTs. The experimental results obtained under various conditions indicate that the proposed circuit has the following features:

- Precise detection of the over-current can be done without an additional current sensor;
- Fast detection and quick reaction of the protection circuit are enough to effectively limit the initial peak current;
- Precise clamping of fault current reduces the peak power and the energy dissipation and hence increases the endurance time of fault current;
- Clamping of fault current and measurement of Vce can improve the error signal noise immunity;
- Safe shutdown of fault currents can control the over-voltage level at turn-off.

The circuit is able to control not only the steady state but also the transient fault currents. In particular, the circuit has the ability to activate the protection circuit and limit fault current at a similar current level irrespective of the fault impedance and the on-state gate voltage.

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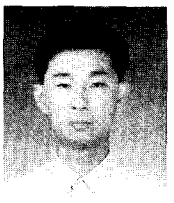

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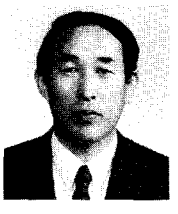

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