〈論 文〉 3-4-8

히스테리시스 제어를 사용하는 Buck Converter의 평균모델을 위한 Duty Cycle 모델링

洪 成 洙

Duty Cycle Modeling for Average Model of Buck Converter Employing Hysteresis Control

Sung-Soo Hong

요 약

히스테리시스 제어를 사용하는 Buck 컨버터의 평균모델을 위한 Duty Cycle 모델이 수학적으로 구해진다. 이 모델은 시간영역에서 연속 전도 모드와 불연속 전도 모드 모두를 동시에 시뮬레이션할 수 있다. 또한, SABER의 MAST언어를 이용하여, 제안된 모델의 템플릿이 제시되며, 이 템플릿은 시간영역이나 주파수 영역의 해석을 위해 사용되어질 수 있다. 이 템플릿의 정확성을 컴퓨터 시뮬레이션을 통하여 증명한다.

ABSTRACT

A duty cycle average model is mathematically developed for an average model of buck converter employing hysteresis control. The derived model is able to simultaneously deal with both the continuous conduction mode (CCM) and the discontinuous conduction mode (DCM) in the time domain. Also, taking advantage of the MAST language of SABER, a template of the proposed duty cycle average model is built for the time and frequency domain analyses. The accuracy of this template is verified through the computer simulations.

Key Words: Buck Converter, Hysteresis Control, Duty Cycle Model, SABER

1. INTRODUCTION

An average model for pulse width modulation (PWM) dc-dc converter is useful for both the time and frequency domain analyses. Especially, the average model which is able to simultaneously deal with both the continuous conduction mode (CCM) and the discontinuous conduction mode (DCM) plays an important role in simulating the time domain response, when a considerable amount of input voltage and load variations takes place instantaneously.

Recently, various average models for PWM dc-dc converter have been introduced, which include both the CCM and the DCM.[1~8] Among them, duty cycle models

for the current-injection control (CIC) have been presented in.[5~8] However, there is no duty cycle model available for the hysteresis control which has the advantages of low audio susceptibility and does not exhibit the sub-harmonic oscillation problem associated with constant frequency control.[9] The purpose of this paper is to present a duty cycle average model for hysteresis control among current-mode control techniques, which is capable of simultaneously dealing with both the CCM and the DCM.

First, a mathematical duty cycle model is derived from the dynamic relationship between on- and off-time duty ratios, average inductor current, and control input, considering the transient state of the current loop.

Secondly, utilizing the MAST language of SABER, a template of the presented duty cycle model is built. The accuracy of this template is verified by computer simulations in comparison with the actual circuit for the time domain analysis.

2. Relationship between Duty Cycles, Average Inductor Current, and Control Input

Fig. 1 shows the CCM operation of hysteresis control in the transient-state. Power switch is turned off when the sensed inductor current reaches the control input. Power switch is turned on at the instant when the sensed inductor current decreases by a chosen amount $R_i \Delta I$, where R_i is the current sensing network gain and $R_i \Delta I$ is the hysteresis band of actual inductor current. If control input v_c is less than $R_i \Delta I$, hysteresis control will not work. Therefore, a circuit is built into hysteresis controller which limit the off-time of power switch. This means that the DCM operation of hysteresis control is the same as one of constant off-time control, which is shown in Fig. 2. Also, it is important to note that converter employing this controller can be operated like constant off-time control even in the CCM according to the size of the off-time T_{off}.

To derive the relationship between the on- and off-time duty ratios and average inductor current, output voltage v_o and control input are presumed to be constant during one switching interval as shown in Fig. 1 and 2, since the dynamics of output voltage and control input is fairly slow compared with one of the inductor current. The on- and off-time current slopes, m_{1t} and m_{2t}, are defined as

$$m_{1t} = R_i \frac{v_g - v_o}{L}, \quad m_{2t} = R_i \frac{v_o}{L} \tag{1}$$

where v_g is the input voltage, L is the output filter inductance. Regardless of the current control schemes and the operating modes, the sensed average inductor current through the sensing network can be expressed as

$$R_i i_L = R_i I_o (d_1 + d_2) + m_{1t} T_s (0.5 d_1^2 + d_1 d_2) - 0.5 m_{2t} T_s d_2^2 \tag{2}$$
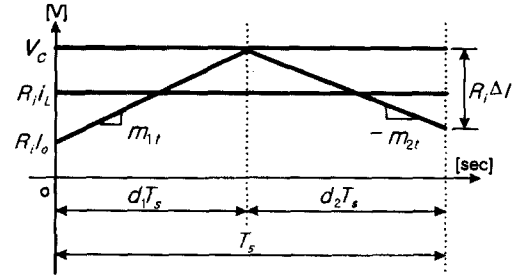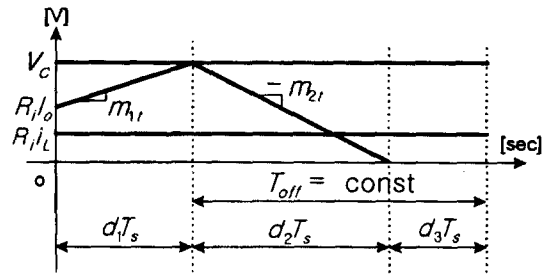

Fig. 1 CCM operation of hysteresis control

Fig. 2 DCM operation of hysteresis control

where I_o is the initial value of inductor current during one switching interval in the actual circuit. The expression is identical to one in [7] and [8].

The switching intervals for the CCM and DCM are easily found to be

$$T_s = \frac{R_i \Delta I}{(1 - d_1) m_{2t}} \quad \text{for the CCM} \tag{3}$$

$$T_s = \frac{T_{off}}{(1 - d_1)} \quad \text{for the CCM} \tag{4}$$

From (3) and (4), an important boundary equation between hysteresis control and constant off-time control in the CCM can be derived as

$$T_{offbnd} = \frac{L \Delta I}{v_o}. \tag{5}$$

At the point where the on-time current slope reaches control input, the following relationship can be obtained:

$$v_c = R_i I_o + m_{1t} d_1 T_s. \tag{6}$$

Eliminating I_o from (2) and (6) gives

$$R_i i_L = (v_c - m_{1t} d_1 T_s)(d_1 + d_2) + m_{1t} T_s (0.5 d_1^2 + d_1 d_2)$$
$$- 0.5 m_{2t} T_s d_2^2. \tag{7}$$

In the CCM, the following equation is satisfied:

$$d_2 = 1 - d_1. \tag{8}$$

Substituting (1), (3) and (8) into (7) gives

$$K_c = 2v_c - 2R_i i_L - R_i \Delta I = \frac{v_g}{v_o} d_1^2 - 2(R_i \Delta I + R_i i_L - v_c)d_1 \tag{9}$$

Since the off-time current slope reaches zero level in the DCM, this gives

$$v_c - m_{2t} d_2 T_s = 0 \tag{10}$$

Substituting (4) into (10) results in

$$d_2 = \frac{(1 - d_1)v_c}{m_{2t} T_{off}}. \tag{11}$$

From (4), (7) and (11), the following equation can be derived:

$$K_d \equiv v_c^2 - 2m_2 R_i i_L = (m_1 m_2 + 2m_2 v_c - v_c^2)d_1^2$$
$$- 2(v_c m_2 - v_c^2 + m_2 R_i i_L)d_1 \tag{12}$$

where

$$m_1 = m_{1t} T_{off}, \quad m_2 = m_{2t} T_{off}. \tag{13}$$

As can be seen in (9) and (12), the on-time duty cycle has either two real or complex roots. Therefore, it is necessary to choose a right duty cycle, considering the physical aspects in actual hardware.

3. Determination of Duty Cycles.

In this section, duty cycles are separately derived using equations for the CCM and DCM developed in the previous section. Also, a condition such that one operating mode is switched to the other is proposed.

A. CCM.

When the large amount of load resistance increase instantaneously, control input could drop all of a sudden. Therefore, the first-order term coefficient in the right-hand side of (9) can be negative in the transient-state and (9) can give the complex roots. Under this situation, actual circuit generates the on-time duty cycle of zero. In order to model this situation, the on-time duty cycle for average model should be forced to become zero, in case of the complex roots. However, if this happens abruptly, the convergence problem could take place. A solution to overcome this problem has been proposed in.[8] Meanwhile, if K_c increases, the on-time duty cycle should increase. Therefore, using d_{11c} instead of d_1 for convenience, this becomes

$$d_{11c} = \{d_{11c} \mid d_{11c} = (R_i \Delta I + R_i i_L - v_c + \sqrt{D_c} \frac{v_o}{v_g} \geq 0\} \tag{14}$$

where

$$D_c = \{D_c \mid D_c = (R_i \Delta I + R_i i_L - v_c)^2 + \frac{v_g}{v_o} K_c \geq 0\}. \tag{15}$$

The on-time duty cycle to avoid the convergence problem can be derived as

$$d_{12c} = \{d_{12c} \mid d_{12c} = S_c(K_c + \frac{v_o(R_i \Delta I + R_i i_L - v_c)^2}{v_g}) \leq 0\} \tag{16}$$

where S_c is an arbitrary number greater than zero. The resultant on- and off-time duty cycles in the CCM become

$$d_{1c} = \{d_{1c} \mid 0 \leq d_{1c} = d_{11c} + d_{12c} \leq 1\} \tag{17a}$$
$$d_{2c} = 1 - d_{1c}. \tag{17b}$$

B. DCM

To determine the duty cycles in the DCM, it is necessary to investigate the sign of the coefficients of (12). Let the second-order term coefficient of the right-hand side of (12) be

$$y = m_1 m_2 + 2m_2 v_c - v_c^2. \tag{18}$$

Substituting (10) into (18) results in

$$y_1 = m_1 m_2 - m_2^2 \{(d_2 - 1)^2 - 1\} \ge m_1 m_2 > 0. \quad (19)$$

Also, let the first-order term coefficient of (12) be

$$y_2 = -2(v_c m_2 - v_c^2 + m_2 R_i i_L). \quad (20)$$

In the similar way, from (10) and (20), the following equation and inequality are satisfied:

$$y_2 = -2(m_2 R_i i_L - m_2^2 (d_2^2 - d_2)) \le -2m_2 R_i i_L < 0. \quad (21)$$

As shown (19) and (21), the coefficients of the second-order term and the first-order term of (12) are always positive and negative. Therefore, the graph expressing (12) can be expressed as Fig. 3. In case of $K_d = K_{d1}$, there exist two real roots at the points A and B. However, since the on-time duty cycle should increase as the control input increases, the on-time duty cycle is determined as the value of point B. Denoting d_d as d_{11a}, this becomes

$$d_{11d} = \frac{v_c m_2 - v_c^2 + m_2 R_i i_L + \sqrt{D_d}}{m_1 m_2 + 2m_2 v_c - v_c^2} \quad (22)$$

where

$$D_d = \{D_d \mid D_d = (v_c m_2 - v_c^2 + m_2 R_i i_L)^2 + (m_1 m_2 + 2m_2 v_c - v_c^2) K_d \ge 0\}. \quad (23)$$

In case of $K_d = K_{d2}$, (22) and (23) give the solution of the point C in Fig. 3. In view of the physical aspects, this situation can happen only when the initial value of
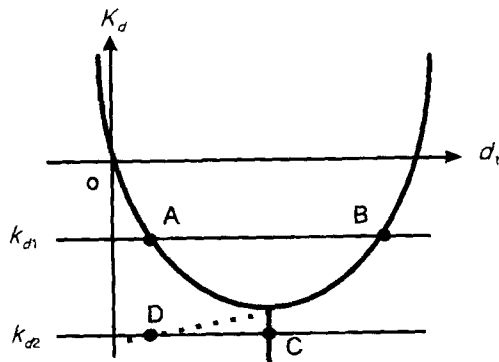

Fig. 3 Graphical interpretation of (12)

inductor current during one switching interval is higher than control input. In this case, it is reasonable that the on-time duty cycle should be forced to be zero like in the CCM. However, if this happens abruptly, the convergence problem can take place. Therefore, the dotted line in Fig. 3 is helpful to avoid the problem, which makes the on-time duty cycle slide to zero. The dotted line can be expressed as

$$d_{12d} = \{d_{12d} \mid d_{12d} = S_d(K_d + \frac{(v_c m_2 - v_c^2 + m_2 R_i i_L)^2}{v_c^2 - 2m_2 R_i i_L}) \le 0\} \quad (24)$$

where S_d represents the slope of dotted line and is an arbitrary number greater than zero. Therefore, the on-time duty cycle in the DCM can be obtained by adding (24) to (22) as

$$d_{1d} = \{d_{1d} \mid \le d_{1d} = d_{11d} + d_{12d} \le 1\}. \quad (25a)$$

From (11), the off-time duty cycle becomes

$$d_{2d} = \frac{(1 - d_{1d})v_c}{m_2}. \quad (25b)$$

C. Operating mode determination between CCM and DCM

As can be seen in Fig. 2, the DCM exists even though the initial value of the inductor current is not zero. Therefore, to derive a condition such that the operating modes are switched each other, it is desirable that the initial value of inductor current be considered. The initial value of sensed inductor current in the CCM can be derived from (2) and (3) as

$$R_i I_o = R_i i_L + R_i \Delta I \frac{v_g}{v_o} \frac{o.5 d_{1c}^2 - d_{1c}}{1 - d_{1c}} + 0.5 \frac{R_i \Delta I}{1 - d_{1c}}. \quad (26)$$

In the CCM, the following equation holds:

$$R_i I_o + m_{1i} d_{1c} T_s - m_{2i}(1 - d_{1c}) T_s > 0. \quad (27)$$

Therefore, the operating mode determination parameter MD can be expressed as

$$MD = \begin{cases} 0 & if \quad R_i I_o + R_i \Delta I \left(\dfrac{v_g - v_o}{v_o} \dfrac{d_{1c}}{1 - d_{1c}} - 1 \right) > 0 \\ 1, & otherwise \end{cases}$$

(28)

where $MD=0$ and $MD=1$ represent the CCM and the DCM, respectively.

Finally, duty cycles can be expressed as

$$d_1 = d_{1c}(1 - MD) + d_{1d}MD \qquad (29a)$$

$$d_2 = d_{2c}(1 - MD) + d_{2d}MD \qquad (29b)$$

$$d_3 = 1 - d_1 - d_2. \qquad (29c)$$

4. Model Validation and Discussions

In this section, the accuracy of the duty cycle model proposed in this paper is verified by computer simulations. Time domain accuracy is emphasized through the comparison with actual circuit response. Overall average circuit diagram is shown in Fig. 4. Symbol A is a template of the average duty cycle model for hysteresis control of buck PWM dc-dc converter proposed in this paper. Symbol B is a template of average PWM switch model presented in [8]. Symbol C is an ideal operational amplifier with a clamping function, which is convenient for limiting control input. All the templates are built using MAST language of SABER as shown in Table I, II and III. Constant voltage source V1 in the figure is used for the control instance of the current controlled voltage source CCVS
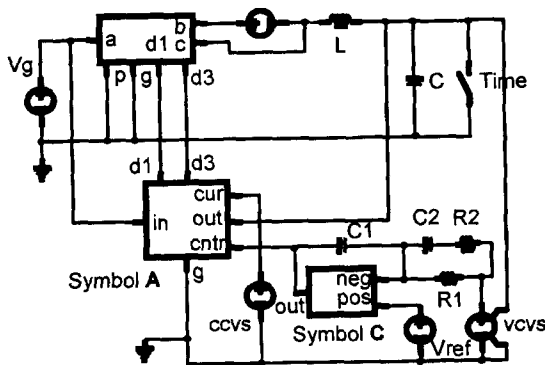

Fig. 4 Overall circuit diagram of average model

and set as zero. The common parameters used for the simulations are as follows:

$$V_g = 12 \ [V], \quad L = 37.5 \ [\mu H], \quad C = 80 \ [\mu F],$$

$$ESR = 20 \ [m\Omega], \quad C_1 = 9 \ [nF], \quad C_2 = 40 \ [nF],$$

$$R_1 = 5 \ [k\Omega], \quad R_2 = 160 \ [\Omega], \quad V_{ref} = 1 \ [V],$$

$$Gain \ of \ VCVS = 0.2, \quad T_{off} = 10 \ [\mu s], \quad R_i = 0.25,$$

$$\Delta I = 1 \ [A], \quad S_c = S_d = 10,000.$$

Fig. 5 shows the various waveforms of actual circuit and the average circuit employing the proposed average duty cycle model when the load resistance changes to 10 $[\Omega]$ from 1 $[\Omega]$ at the time of 2 [ms]. As can be seen in Fig. 5(a), the output voltage of the average circuit employing the proposed average duty cycle model has a good agreement with one of actual circuit. Also, Fig. 5(b) shows that the inductor current of the average circuit tracks the average motion of the inductor current of actual circuit. The dashed and dot-dashed line are the output voltages of average circuit without compensation slope for the CCM and DCM, respectively, proposed in this paper. The output voltages of the average circuit without compensation slope considerably deviate from those of actual circuit. Fig. 5(c) shows that the determinators of (9) and (12) can become negative, which are expressed as tD_c and tD_d in Table I. As mentioned earlier, this situation requires that the on-time duty cycle become zero in actual hardware. Therefore, the compensation slope is required for rapid drop to zero of the on-time duty cycle in both CCM and DCM. To verify this fact, Fig. 5(d) shows the on-time duty cycle of actual circuit and the proposed model. The on-time duty cycle of actual circuit becomes zero. The very short pulse in the figure is due to the limitation of control circuit and meaningless. The on-time duty cycle of the proposed model also becomes zero very rapidly as expected. In Fig. 5(c), the operating mode determination parameter MD tells that the circuit is operating in the DCM during the transient-state. In order to verify the accuracy of operating mode determination parameter, Fig. 5(e) is focused about the situation of the first transition from the CCM to the DCM. The sensed inductor current of actual hardware gives an idea of when the operating
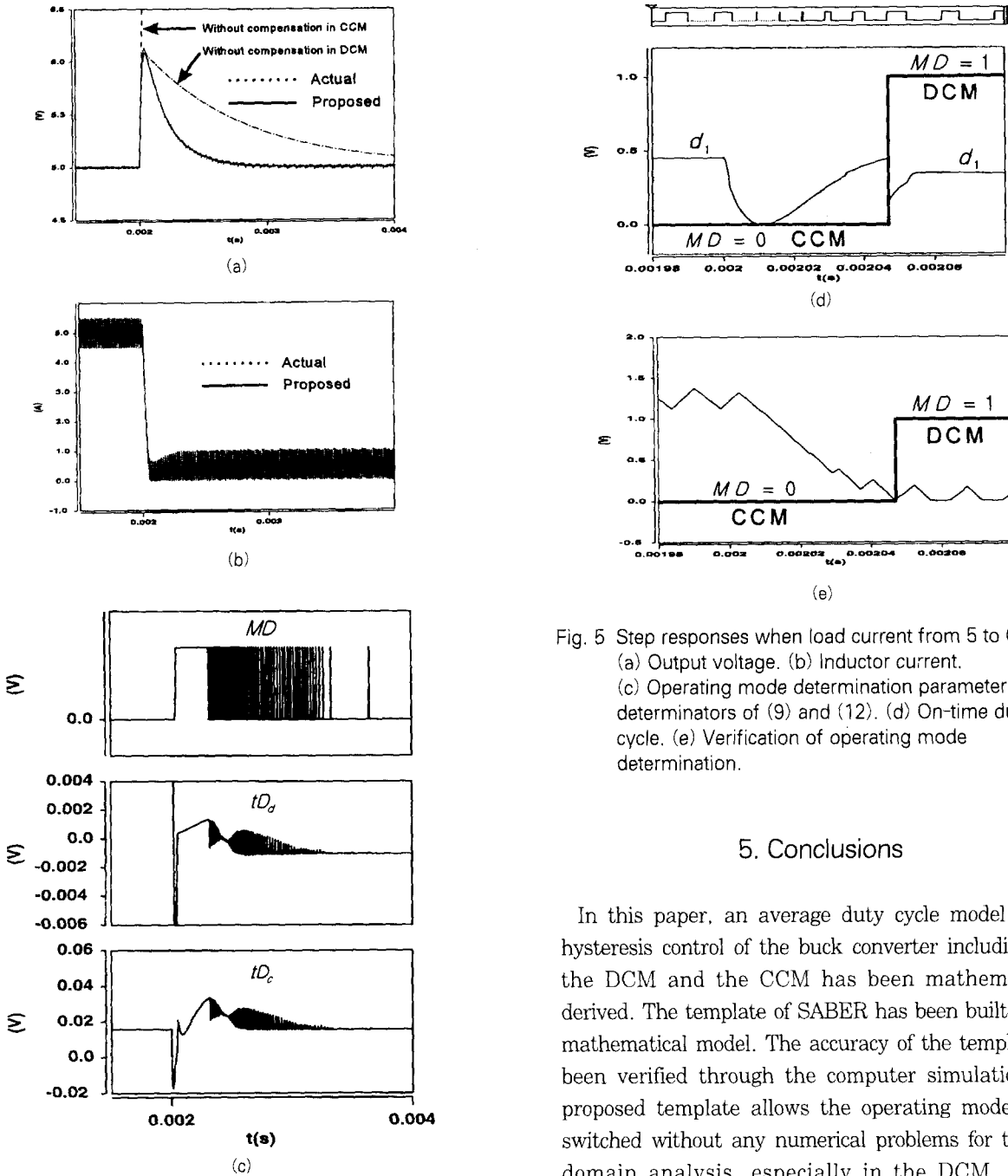
(a)

(b)

(c)

(d)

(e)

Fig. 5 Step responses when load current from 5 to 0.5 A
(a) Output voltage. (b) Inductor current.
(c) Operating mode determination parameter and
determinators of (9) and (12). (d) On-time duty
cycle. (e) Verification of operating mode
determination.

5. Conclusions

In this paper, an average duty cycle model for the hysteresis control of the buck converter including both the DCM and the CCM has been mathematically derived. The template of SABER has been built for this mathematical model. The accuracy of the template has been verified through the computer simulation. The proposed template allows the operating modes to be switched without any numerical problems for the time domain analysis, especially in the DCM. All the simulated signals using the proposed technique have a good agreement with those using actual circuit. Although the derivation of the model assumes a buck converter, the modeling process itself can easily be extended to include the boost and buck-boost converter topologies.

mode changes from the CCM to the DCM. The operating mode determination parameter coincides with the operating mode of actual circuit. This is also shown in Fig. 5(d). The off-time limitation T_{off} is given as 10 $[\mu s]$ in the DCM. The transition occurs at the time when the off-time becomes 10 $[\mu s]$.

TABLE I.

Symbol **A** : Template of Duty Cycle Model for
Hysteresis Control

```
element    template hysduty in out cur cntr d1 d3 g\ = L, Ri,
dI, Toff, Sc, Sd
# in = input voltage, out = output voltage, cur = sensed #
inductor current, cntr = control input, d1 = on-time
# duty cycle, d3 = duty cycle of inductor current zero,
# g = ground, L = output filter inductance, Ri = current #
sensing network gain, dI = hysteresis band current,
# Toff = constant off-time, Sc = Slope in CCM, Sd =
# Slope in DCM
electrical in, out, cur, cntr, d1, d3, g
number L, Ri, dI, Toff, Sc, Sd
{
branch vg = v(in,g)
branch vo = v(out,g)
branch vi = v(cur,g)
branch vc = v(cntr,g)
branch id1 = i(d1->g), vd1 = v(d1,g)
branch id3 = i(d3->g), vd3 = v(d3,g)
val v Kc, tDc, Dc, d11, td12c, d12c, d1c, d2c, m1, m2,\
       Kd, tDd, Dd, d11d, td12d, d12d, d1d, d2d, vIo,\
       Md, vd2
values {
# Duty Cycles in the CCM
Kc = 2*(vc - vi) - Ri*dI
tDc = (Ri*dI + vi - vc)**2 + Ri*dI*vg/vo*Kc
Dc = if tDc >= 0 then tDc\
        else 0
d11c = (Ri*dI + vi - vc + sqrt(Dc))/(Ri*dI*vg/vo)
td12c = Sc*(Kc + (Ri*dI + vi - vc)**2/(Ri*dI*vg/vo))
d12c = if td12c >= 0 then 0\
        else td12c
d1c = if d11c + d12c <= 0 then 0\
        else if d11c + d12c >= 1 then 1\
        else d11c + d12c
d2c = 1 - d1c

# Duty Cycles in the DCM
m1 = Ri*(vg - vo)*Toff/L
m2 = Ri*vo*Toff/L
Kd = vc**2 - 2*vi*m2
tDd = (vc*m2 - vc**2 + m2*vi)**2 + (m1*m2
       + 2*m2*vc - vc**2)*Kd
Dd = if tDd <= 0 then 0\
        else tDd
d11d = (vc*m2 - vc**2 + m2*vi
       + sqrt(Dd))/(m1*m2 + 2*m2*vc - vc**2)
td12d = Sd*(Kd + (vc*m2 - vc**2
       + m2*vi)**2/(m1*m2 + m2*vc - vc**2))
```

```
d12d = if td12d >= 0 then 0\
        else td12d
d1d = if d11d + d12d <= 0 then 0\
        else d11d + d12d
d2d = (1 - d1d)*vc/m2


# Determination between the CCM and the DCM
vIo = vi + Ri*dI*vg/vo*(0.5*d1c**2 - d1c)/(1     - d1c) +
0.5*Ri*dI/(1 - d1c)
MD = if vIo + Ri*dI*((vg - vo)/vo*d1c/(1
       - d1c) - 1) < 0 then 1\
        else 1

# Final Solutions
vd2 = d2c*(1-MD) + d2d*MD
        }
equations {
        vd1 = d1c*(1-MD) + d1d*MD
        vd3 = 1 - vd1 - vd2
        }
}
```

TABLE II.

Symbol **B** : Template of Average Model of PWM Switch
for dc-dc Converter

```
# Average model of PWM switch for dc-dc converter in [8]
element template  pwmavg a b c p d1 d3 g
electrical a, b, c, p, d1, d3, g
{
branch  vd1 = v(d1,g)
branch  vd3 = v(d3,g)
branch  ibp = i(b->p), vbp = v(b,p)
branch  iap = i(a->p), vap = v(a,p)
branch  vcp = v(c,p)
equations {
        vap = vd1*vap + vd3*vcp
   iap = (vd1 + vd3*vcp/vap)*ibp
        }
}
```

Table III.

Symbol **C** : Template of Ideal Op-amp. with Output
Voltage Clamping.

```
Element template idlop neg pos out g = rin,\
              gain, vmin, vmax
electrical neg, pos, out, g
number rin, gain, vmin, vmax
{
branch vin = v(pos,neg)
branch vout = v(out,g)
```

```
branch iin = i(pos->neg)
iin = vin/rin
vout = if gain*vin <= vmin then vmin\
       else if gain *vin >= vmax then vmax\
       else gain*vin
}
```

References

[1] V. Bello, "Computer aided analysis of switching regulator using SPICE," *IEEE PESC Rec.*, pp.3~11, 1980.

[2] V. Bello, "Using SPICE2 CAD package for easy simulation of switching regulators in both continuous and discontinuous modes," *Proc. Powercon 8*, pp.1~14, 1981.

[3] Y. Amran, F. Huliehel, and S. Ben-Yaakov, "A unified SPICE compatible average model of PWM converters," *IEEE Trans. on Power Electron.*, pp.585~594, Oct. 1991.

[4] L. Dixon, "SPICE simulation of switching power supply performance," Unitrode Power Supply *Design Seminar Handbook*, 1991.

[5] S. Ben-Yaakov, "Average simulation of PWM converters by direct implementation of behavioral relationships," *APEC Proc.*, pp.510~516, 1993.

[6] R. E. Griffin, "Unified power converter models for continuous and discontinuous mode," *IEEE PESC Rec.*, pp.853~860, 1989.

[7] F. D. Rodriguez and J. E. Chen, "A refined nonlinear averaged model for constant frequency current model controlled PWM converters," *IEEE Trans. on Power Electron.*, pp.654~664, Oct. 1991.

[8] Sung-Soo Hong, Byeong-Rim Jo, and Myung-Joon Youn, "Duty cycle generator for average model of buck converter with current-mode control Using analog behavioral modeling of Pspice," *IEEE Tran. Power Electron.*, pp.785~795, Nov. 1996.

[9] R. Red and N. O. Sokal, Current-mode control, "Five different types, used with three basic classes of power converters : small-signal ac and large-signal dc characterization, stability requirements, and implementation of practical circuits," *IEEE PESC Rec.*, pp.771~785, 1985.

〈 저 자 소 개 〉

홍성수(洪成洙)
1961년 1월 25일생. 1984년 서울대학교 전기공학과 졸업. 1986년 한국과학기술원 졸업(석사). 1992년 동 대학원 졸업(공박). 현재 현대전자 정보통신 연구소 위성연구실 근무.