의공학회지 : 제18권, 제4호, 1997
J. of KOSOMBE : Vol. 18, No. 4

연 구 논 문
97-18-4-17

Programmable DSP 코어를 사용한 고성능 디지털 보청기 프로세서

박영철·김동욱·김인영·김원기

= Abstract =

A High-performance Digital Hearing Aid Processor Based on a Programmable DSP Core

Y.C. Park, D.W. Kim, I.Y. Kim, and W.K. Kim

This paper presents a designing of a digital hearing aid processor (DHAP) chip being operated by a dedicated DSP core. The DHAP for hearing aid devices must be feasible within a size and power consumption required. Furthermore, it should be able to compensate for wide range of hearing losses and allow sufficient flexibility for the algorithm development. In this paper, a programmable 16-bit fixed-point DSP core is employed for the designing of the DHAP. The designed DHAP performs a nonlinear loudness correction of 8 frequency bands based on audiometric measurements of impaired subjects. By employing a programmable DSP, the DHAP provides all the flexibility needed to implement audiological algorithms. In addition, the chip has low-power feature and 5,500×5,000㎛² dimensions that fit for wearable hearing aids.

Key words : Digital hearing aid, Nonlinear loudness correction, DSP

INTRODUCTION

For human being, 'hearing' is more than a mere sensory mechanism. With a loss of hearing, man is restricted from his or her normal social activity, which may in turn cause undesirable influence on mental health [1]. In order to compensate for this kind of handicap, many researches have been conducted [2-5]. Most of them were focused on developing various signal processing algorithms for hearing aids. Ideal hearing aid for peripheral hearing losses would modify the incoming signal in order to provide a perfect match between the cochlear outputs of impaired ear to those of reference normal ear. In practice, however, this ideal approach is not feasible since it would require access to the complete set of neural fibers both in the impaired ear as well as the normal ear. The objective of hearing aids is to modify acoustic signals to produce the best possible match between outputs of simulated normal and impaired ears. Various signal processing algorithms so far have been suggested to achieve this goal.

Modern hearing aids can be subdivided into three groups: analog, digital, and analog/digital hybrid hearing aids. Though the majority of currently available hearing aids are analog devices employing conventional analog circuits, the digital technology has offered new possibilities for noticeable advances of hearing aids. Using digital technologies, the *ad hoc* nature of conventional hearing aids can be replaced by a more rigorous procedure. Furthermore, these technologies has conveyed convenient tools to implement powerful features in hearing aids, such as nonlinear amplification, noise reduction, and enhanced fitting

삼성생명과학연구소 임상의공학센터 DSP 연구실
DSP Lab., Biomedical Engineering Center, Samsung Biomedical Research Institute
통신저자 : 박영철, (135-230) 서울시 강남구 일원동 50, Tel. (02)3410-3732, Fax. (02)3410-3689

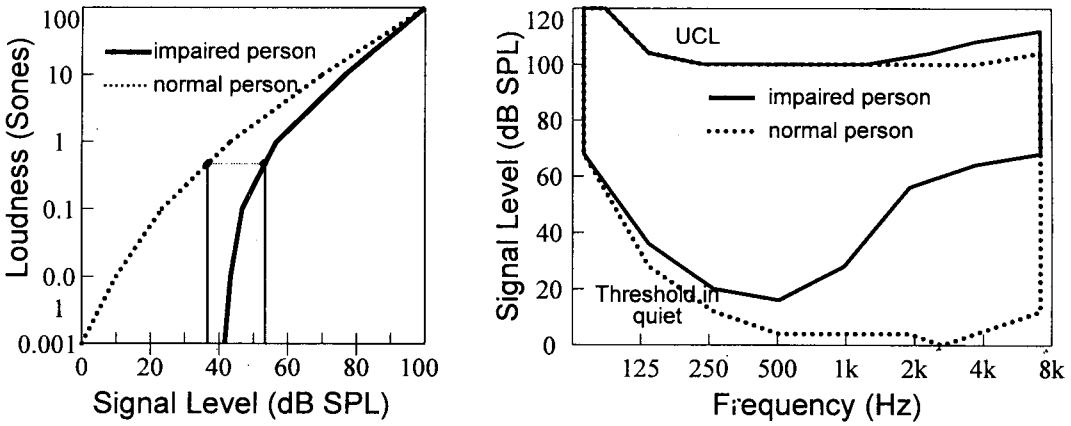


Fig. 1. Common features of the hearing loss. Nonlinear loudness growth (left), and reduced hearing range (right)

algorithms. There are also ongoing efforts in developing further advanced signal processing techniques for hearing aids. Despite the considerable possibility of the digital technology, size, computational capacity, and power consumption of digital equipment have limited its use for the hearing impairment in comparison with the analog devices. They have been main obstacles to the implementation of wearable digital hearing aids. However, due to the recent technological progress in very large-scale integrated (VLSI) circuits, digital signal processing (DSP) chips allow for the real-time implementation of highly sophisticated DSP algorithms in small units with low power.

This paper concerns a designing of a digital hearing aid processor (DHAP) chip being operated by a dedicated DSP core. The DHAP for hearing aid devices must be feasible within size and power consumption required. Furthermore, it should be able to compensate for wide range of hearing losses and allow sufficient flexibility for the algorithm development. In this work, a 16-bit fixed point DSP core is employed for the designing of the DHAP. The required computational power of the DHAP may totally depend on the complexity of the algorithm. However, as the gain compensation is often required for several frequency bands, the computational burden for the DHAP would be significant. Moreover, if additional signal processing algorithms, such as speech enhancement and adaptive feedback cancellation, are considered, the burden may increase up to a few tens of million instructions per second (MIPS). Another important issue of concern is the power consumption. As the operation speed of the processor increases, the processor would consume more power. But most hearing aids are implemented in small wearable units. Therefore, the power consumption is one of key factors to the successful development of the digital hearing aid. Based on these considerations, we choose a 16-bit programmable DSP core being capable of performing 30 MIPS with 3V power supply.

The hearing aid algorithm presented in this paper is based on a multichannel nonlinear loudness correction that transforms input speech signal according to the level and frequency to restore the loudness perception of the impaired person. The algorithm is generally known as the wide dynamic range compression [2,4,5]. To define the impaired mapping between the sound pressure level of the natural acoustical signals and the perceived loudness of the impaired auditory system, loudness scaling functions (LSF's) are generated from the audiometric measurements. These functions describe how much gain is needed for each frequency and level of the input to restore normal loudness perception. Later, energy estimates in 8 frequency bands are applied to the LSFs, and scaling factors for the loudness correction are computed.

DIGITAL HEARING AID (DHA) ALGORITHM

The most obvious feature of impaired hearing is the shift in auditory threshold as shown in Figure 1. Also, for most hearing-impaired subjects, the eleva-

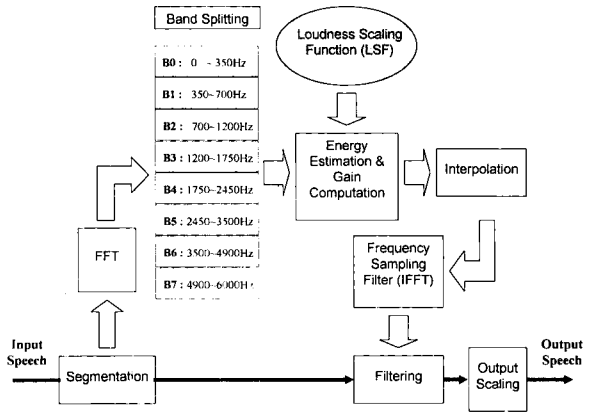


Fig. 2. Block diagram of the eight channel loudness correction algorithm

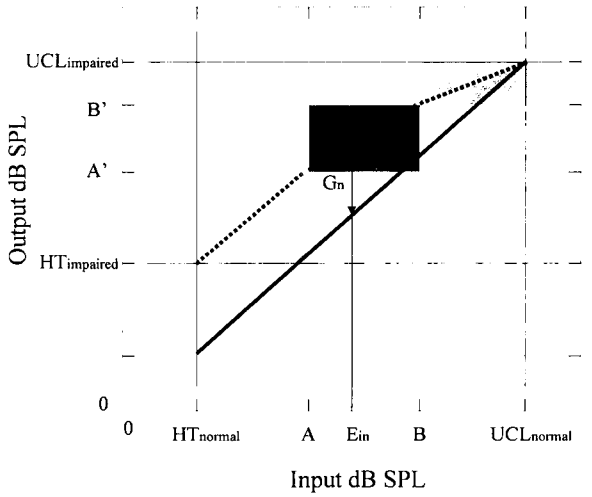


Fig. 3. Schematic diagram of the compression method based on the loudness scaling function. When the energy estimate of the band is Ein, the computed gain factor is Gn

tion of the hearing threshold is accompanied by an unequal elevation of the sound pressure level (SPL) beyond which the sounds become uncomfortably loud. As a result, their dynamic range can be considerably reduced. Another feature often associated with the sensorineural-type hearing impairment is the nonlinear growth of the loudness, so-called the recruitment [1], which is also illustrated in Figure 1

Since the hearing loss tends to vary with frequency, there have been attempts to confront these problems with wide dynamic-range compensation systems whose behavior also varies with the frequency. Recently, a variety of multichannel signal processing algorithms were suggested [2,4,5] as a remedy to those problems. In several studies, the detrimental or no consistent positive effect of the multichannel dynamic compression on the performance of the hearing aid was indicated [6,7]. Recent findings, however, suggest that the multichannel dynamic compression may be beneficial to individuals with mild to moderately severe sensorineural hearing loss. Hohmann and Kollmeier [9] indicated that the multichannel compression aids for the impaired persons with sensorineural hearing impairment should be included for further considerations. In particular, in situations with fairly high signal-to-noise ratio these aids provided substantial benefits on speech intelligibility. The effect of the multichannel dynamic compression on speech intelligibility is still a controversial issue and it is generally believed that the issue can only be resolved by laboratory experiments. Regarding the channel number, some studies indicate that no more than two or three channels of multichannel compression will be of benefit [7]. But Yund and Buckles [10] showed that the multichannel dynamic compression with at least 8 channels was a very effective way of providing maximal auditory information to individuals with broad range of hearing impairments.

1. Multichannel loudness correction algorithm

For the development of the digital hearing aid processor, a multichannel loudness correction algorithm with 8 processing channels is developed and implemented. Processing steps for the algorithm are shown in Figure 2.

The speech signal is A/D-converted at the rate of 12 kHz and divided up into 8 frequency bands via the spectral estimation. Within the spectral estimation procedure the energy of input signal is estimated for each frequency band to compute a time-varying correction factor. It should be mentioned that hearing losses are generally measured using narrow band (pure tone) signals and the incoming sounds consist mainly of broadband signals. To account for the loudness perception of the input complex sounds, the input energy, rather than the magnitude, is measured. The energy is estimated based on eight frequency bands. Specifications of eight frequency bands are list-

Table 1. Specifications of eight frequency bands

Band	0	1	2	3	4	5	6	7
f_c	–	500	1k	1.5k	2k	3k	4k	–
f_u	353	707	1.2k	1.7k	2.4k	3.5k	4.9k	6k

ed in Table 1. f_c and f_u in Table 1 represent the center frequency and the upper frequency limit, respectively. The frequency band parameters in the table are similar to those in [9] except the lowest two bands. Critical band channels were considered when the eight-band parameters were determined. After combining several adjacent critical band channels, the specifications for the eight processing channels were determined. Sampled input signal is segmented into windowed frames of 128 samples without overlap. Size of the windowed frames was determined by considering the computational efficiency. Hamming window is applied to the input for the segmentation. Each frame is then transformed into the frequency-domain via FFT. The input energy for each frequency band is obtained by adding up the powers of all FFT coefficients belonging to the corresponding frequency band. After computing the logarithm of the energy, a level adjustment of input energy is performed according to a predefined compression function sketched in Figure 3.

Given data on the hearing impairment of the patient, the gain for the momentary amplification or attenuation in decibels is computed using the loudness scaling function (LSF) which is obtained from the difference between the input energy and the desired energy. The LSF can be considered as a description of how much gain is required for each frequency band to restore the normal loudness perception. The LSF is defined at each of eight frequency bands based on the hearing threshold (HT) and uncomfortable loudness level (UCL) of the normal and impaired persons. To represent the nonlinear feature of the audiometric function, we break the LSF into three equally spaced regions as can be seen from Figure 3. Each region covers equal level range; (UCL-HT)/3. In the figure, A and B represent breaking points, and A′ and B′ are corresponding output levels. Thus, different compression ratio, *i.e.*, slope of the curve, can be applied to the input according to the input level. By using this method, we can introduce an expansive characteristics for levels below the noise level to avoid an overamplification of background and quantization noise [9].

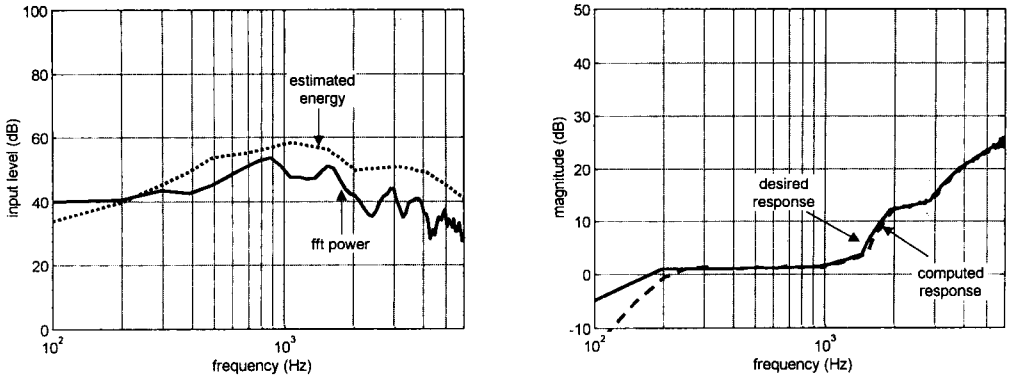
2. Frequency sampling filter design

After obtaining gain factors for eight frequency bands, the acoustic amplification is accomplished in time-domain by designing a finite impulse response (FIR) filter with which the input signal is modified into a desired form. The instantaneous gain factors obtained at each processing block are interpolated to define the frequency response of the desired filter in the linear frequency scale. The interpolation results in 64 frequency coefficients, and they are used to compute coefficients of the FIR filter. The overall flow of the filter design follows the frequency sampling method. The frequencysampling filter design method requires 2N-size cosine table to design N-th order FIR filter. The cosine table may be stored either in an internal memory or an external memory space of the processor. However, the table should be included in the internal memory space with the minimum occupation because its size affects not only the power consumption of the processor but the physical dimensions of the chip. As an effort to reduce the memory usage of the algorithm, the filter coefficients are obtained using the equation given by

$$h(m)=\frac{1}{N}\left\{H(0)+2\sum_{n=1}^{(N/2)-1}H(n)\cos\left(2\pi(m+1+\frac{N}{2})n\right)\right\},\ 0\le n\le\frac{N}{2}, \quad (1)$$

where N=128. The filter designed using Eq. (1) has N/2 sample group delay, rather than (N-1)/2, so that it can be implemented with a N-size cosine table.

The use of a single FIR filter has several distinctive advantages over the filter-bank approach [4]. First of all, the spectral distortion due to different gains in different frequency bands can be prevented



(a) Estimated energy at each frequency band

(b) Frequency response of the frequency sampling filter

Fig. 4. Example of the energy estimation and gain computation

because the frequency response is obtained by smoothing the gains of eight frequency bands. Thus, it supports smooth and temporarily flexible realization of the dynamic compression. Another advantage of employing the single filter approach can be found in the system complexity. The filter-bank method is often implemented with a bank of FIR band-pass filters. To avoid spectral overlap between adjacent bands, the band-pass filters should meet a specified requirement for the stop-band, which often results in long impulse responses. Thus, the increase of the channel number is possibly associated with a significant increase of the computational complexity. However, the single filter method can comprise the increase of the channel number within the gain factor computation procedure because the issue in this case is simply how to group the frequency powers to obtain gain factors. To show the performance of the compression method employed in this study, the energy estimates obtained from the FFT power and the desired and computed frequency responses are presented in Figure 4. The figure clearly shows the flexibility and effectiveness of the developed compression method.

3. Characteristics of the algorithm

In the algorithm the compression time constants are not selectable as an independent parameter. Instead, the effective time constants are determined by the refresh timing of the coefficients of the FIR filter. The effective time constants in this study correspond to an equal attack and release time of 10.7 msec. Increasing the effective time constants is possible by setting the coefficient of the one-pole infinite impulse response (IIR) low pass filter which averages the gain factor in each channel. In this case, the effective time constants are given by multiples of the fundamental time constant. Another issue often associated with any digital hearing aid algorithm is the time delay. Too long time delay would be expected to interfere with lip reading, but it was shown in [11] that time delays up to about 40 msec do not disturb audio-visual integration of speech information. The sample delay expected in the presented method is within 128 to 192 samples, *i.e.*, 1 to 1.5 frames, depending on how to operate data buffers. In the worst case, the expected time delay would be 16 msec when the input signal is sampled at 12 kHz rate.

By looking at the frequency response of the processing filter, it is possible to characterize the performance of multichannel dynamic compression, at least, in the signal processing perspective. However, since the frequency response of the FIR filter changes continuously as a function of spectral energy distribution of the input speech, the multichannel dynamic compression does not characterize its function in a static form. Rather, its dynamic behavior is more important to characterize its performance. Though the instantaneous frequency response generally will not show the frequency response of the hearing aid processor, an averaged frequency response still can be measured as the difference between the long-term output and input spectra. Figure 5 shows the input

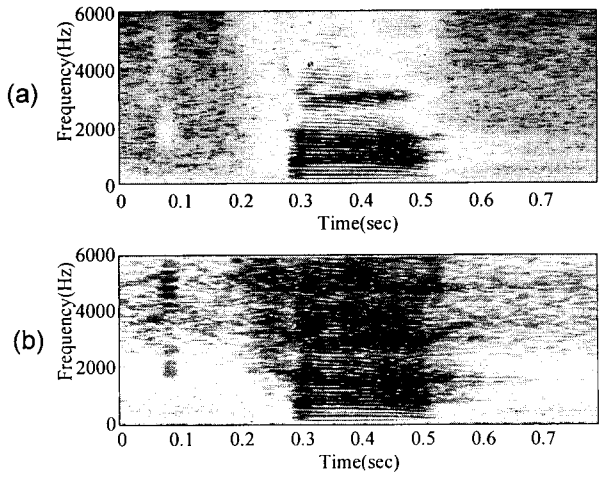


Fig. 5. Spectrogram of the monosyllable /SA. Before (a) and after (b) processing by the multichannel dynamic compression algorithm

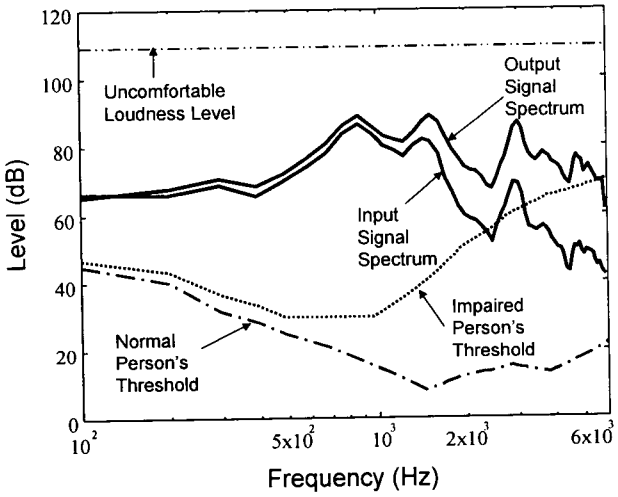


Fig. 6. Averaged spectra of the monosyllable /SA. Input and output of the multichannel dynamic compression system are compared

and output spectrograms of the eight channel dynamic compression for the monosyllable '/SA/', and the averaged input and output spectra are shown in Figure 6. The nonlinear amplification of the algorithm depends on the audiometric data of the hearing impairment. In these simulations, it was assumed that the subject had hearing losses shown in Table 2.

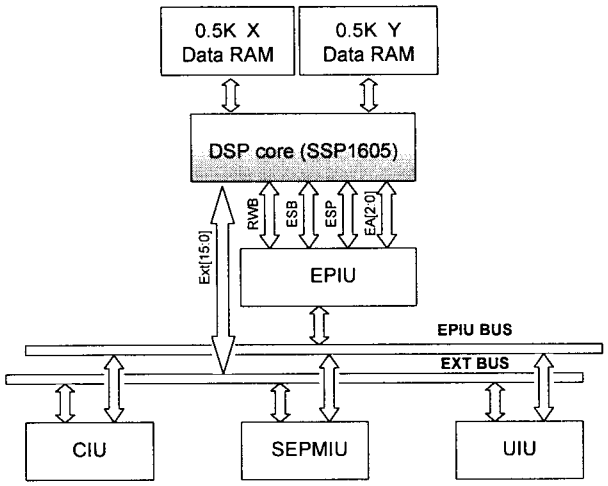


Fig. 7. Schematic diagram of the DHAP

4. Real-time software

Real-time software was designed using the SSP1605 assembly language to implement the multichannel dynamic compression described in the previous sections. In summary, the DSP core consumes 100k clock cycles to implement the algorithm, which corresponds to 9.4 MIPS complexity. The size of the required internal RAM is 1k words in total. Table 3 summarizes the clock and memory usage of the algorithm for the real-time implementation.

Table 3. Complexity of the multichannel dynamic compression algorithm implemented by using SSP1605 DSP core

Procedure	# of cycles
Energy estimation	27,288
Gain factor computation	3,017
Filter design	40,217
Filtering	22,184
Interrupt service routine	7,622
Total	100,228

DESIGNING OF THE DHAP CHIP

The DHAP is based on a general-purpose 16 bit

Table 2. Assumed hearing losses of the subject for the simulation

Frequency (Hz)	250	500	1k	1.5k	2k	4k
Hearing loss (dB)	5	5	15	30	40	55

Table 4. Interrupt usage of the DSP core

Interrupt	0	1	2
Function	UIU	SEPMIU	CIU

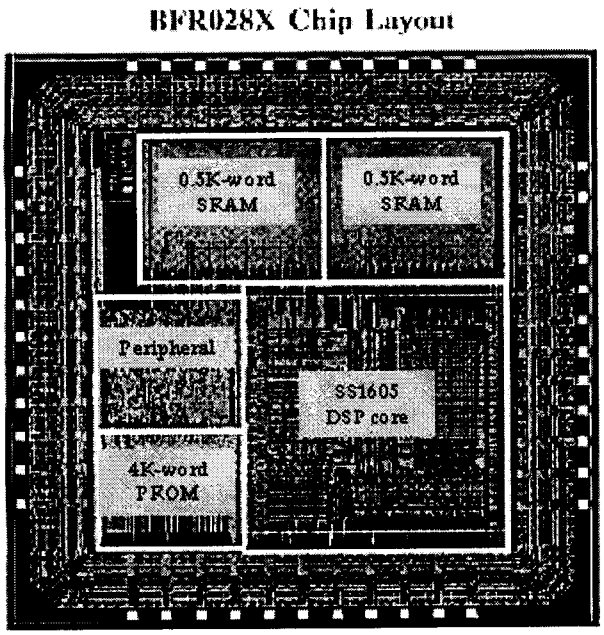


Fig. 8. Internal architecture of the DHAP chip

DSP core (SSP1605) which is able to perform maximum 33 MIPS at 33 MHz clock with 3.3V power supply. The processor is composed of seven units: DSP core, 4k word program ROM, 1k word data RAM (0.5k word X ad Y data RAMs each), external peripheral interface unit (EPIU), CODEC interface unit (CIU), serial electrically erasable PROM (EEPROM) memory interface unit (SEPMIU), and universal asynchronous receiver-transmitter (UART) interface unit (UIU). Figure 7 shows a schematic diagram of the DHAP.

The sizes of the program ROM and the data RAM were estimated from the real-time software. The EPIU controls interrupt access of external peripherals such as CODEC, EEPROM, and UART. The CIU was designed to support a 16-bit single-channel audio CODEC (AD73311). The CODEC clock signal is generated by the DSP core, and the frame sync pin of the CODEC is directly connected to Interrupt 1 pin of the core. To preserve the audiometric parameters of the patient in the power-out situation, a ROM-type memory is required. The power-out may happen when the user changes batteries. A serial EEPROM is selected for this purpose. The EEPROM, in general, is small in size and relatively simple in the interface logic. However, additional interface logic is not included except serial-to-parallel and parallel-to-serial converters. The exact timing for the interface is controlled by the software using the interrupt signal from the SEPMIU unit. Consequently, the SEPMIU in Figure 6 can provide a path between the DSP core and the serial EEPROM.

Another requirement for the hardware design is that it should allow for the change of audiometric parameters of the patient in order to provide the impaired person with the best fitting. To meet this requirement, the UART interface unit (UIU) is comprised in the processor. When the parameter change is required for fitting, the program running on a PC may send out parameters through RS232C port. The parameters are received by the DSP through UIU and then, written onto the EEPROM by the DSP. An asynchronous communication protocol was chosen to minimize physical connections between the host PC and the DHAP. The transmission rate in this case is not a serious issue because the UIU interface will be enabled and the hearing aid may not be worn by the user during download. The communication protocol for the UIU was set to 2400 baud rate, one start bit, no parity, and 8 bit data.

In the real-time program, Interrupt 2 of the DSP core is initialized by the frame sync signal from the CODEC. Complying with the interrupt request, the DSP collects input samples for one-frame (128 sample) period, during which it processes previous 128 samples using the eight channel loudness correction. The table in the EEPROM is copied onto the internal RAM of the processor at the initialization stage. In such a way, the audiometric data is accessible without additional time delay. When new fitting is requested, Interrupt 0 of the DSP core is initiated by the UIU unit. Interrupt 1 is used for the interface with the EEPROM. Table 4 summarizes the interrupt usage of the DSP core.

Since the computational complexity of the DHA algorithm is a little less than 10 MIPS, lower system clock, such as 12.288 MHz, can be applied to the DSP core at which it delivers 12.288 MIPS. By oper-

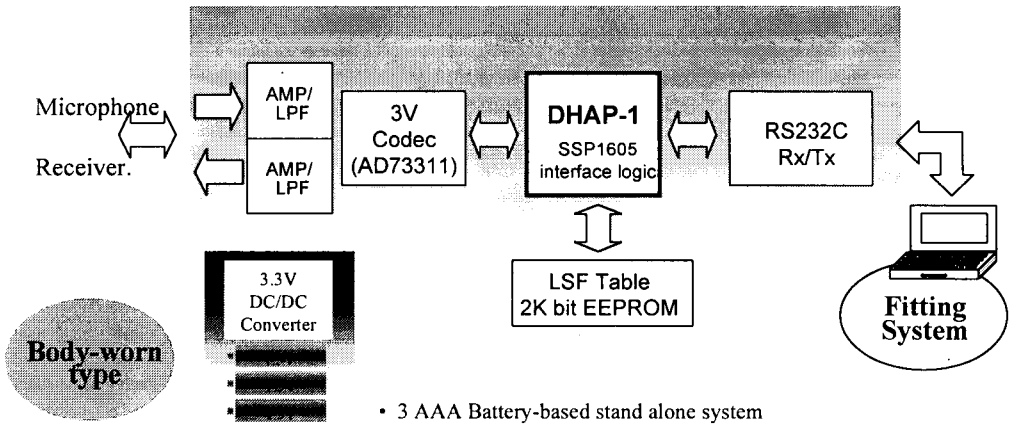


Fig. 9. Block diagram of the prototype system designed using the DHAP processor

ating the chip at low clock speed, it may be is possible to save the power.

Figure 8 shows the internal architecture of the DHAP chip fabricated with 0.65 μm double metal process. The fabricated DHAP has dimensions of 5,500 × 5,000 mm^2 that is small enough to fit for wearable hearing aids. Moreover, the chip features a low power operation manageable with small batteries. The followings are general specifications of the DHAP chip.

* Application specific DSP based on SSP1605 DSP core
* CSP4HS (0.65 μm) double layer metal CMOS technology
* 44 QFP package type
* Operation clock : 12.5MHz
* Operation voltage : 2.7~3.3V
* Operation current is less than 35 mA

PROTOTYPE SYSTEM

Figure 9 shows a block diagram of a hearing aid prototype system based on the DHAP chip developed in this study. To supply the 3.3V power to the hearing aid, three AAA batteries are used together with a 3.3V DC-DC converter. The prototype system is designed for body-worn type hearing aids. Since the LSF in each frequency band is defined using 8 parameters, a 2k bit serial EEPROM is employed to preserve the eight frequency band LSF functions. Analog microphone and receiver circuits conventionally used in analog hearing aids were included in the system. Analog circuits were, however, modified to fit their input and output ranges into those of the CODEC's. For the UART interface with the host PC, a graphic user interface software was developed and run on the PC. The software can be combined with a fitting software that may be built based on a standard platform. General features of the prototype system are summarized as

* Body-worn type hearing aid
* Dimensions 5.3 × 7.5 × 1.2 cm^3, weight 32g without batteries
* 8 band nonlinear wide dynamic range compression
* Maximum gain 50 dB in digital
* Low spectral distortion due to the single filter structure
* Programmable DSP employed
* Fitting parameters are downloadable from a PC.

CONCLUSIONS

A digital hearing aid processor chip built around a 16-bit DSP core is developed. The algorithm based on the eight-channel dynamic compression and the high performance achievable with low power describe distinctive features of the designed DHAP. In addition, the chip has the dimensions fit for wearable hearing aids. Using the chip, a body-worn type hearing aid has been developed and its electrical as well as clinical performances are currently under test. Despite the existing or potential features of the DHAP chip, fur-

ther reduction of the operation voltage and current is still required to fit for smaller hearing aids such as behind-the-ear (BTE), in-the-ear (ITE), and custom in-the-canal (ITC) type devices. Also, it would be desirable to include the CODEC within the processor chip. Those aspects would remain as a future work and will be considered in the next version of the DHAP chip.

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=국문초록=

본 논문에서는 DSP 코어를 채용한 디지털 보청기 칩을 설계 제작하였다. 디지털 보청기 칩은 크기와 소비전력면에서 크게 제한을 받는다. 이와함께 다양한 형태와 범위의 청각 손실에 대해 보상을 할 수 있어야 하기 때문에 알고리즘 개발을 위해 구조적인 유연성을 필요로 한다는 점도 칩 설계에 있어 또다른 제약이 된다. 본 연구에서는 16 비트 고정 소수점 연산을 하는 프로그래머블 DSP 코어를 사용하여 보청기 칩을 설계하였다. 제작된 보청기 칩은 난청자의 청각 측정치를 바탕으로 8 개의 주파수 대역에 걸쳐 비선형적으로 라우드니스를 보상해 준다. 필터 뱅크를 사용하는 대신에 본 연구에서에서는 단일필터를 주파수 샘플링 방법으로 설계함으로써 주파수 왜곡을 최소화 하였다. 또한 프로그램 가능한 DSP 코어를 사용하였기 때문에 알고리즘 개발을 위한 시스템으로도 활용이 가능할 뿐만 아니라 5,500×5,000 μm^2의 크기와 저전력 동작특성을 갖고 있어서 소형 보청기 제작에 적합하다.