# A 10-Gbit/s Limiting Amplifier Using AlGaAs/GaAs HBTs

Sung-Ho Park, Tae-Woo Lee, Yeong-Seuk Kim, Il-Ho Kim, and Moon-Pyung Park

## Abstract

To realize 10-Gbit/s optical transmission systems, we designed and fabricated a limiting amplifier with extremely high operation frequencies over 10 GHz using AlGaAs/GaAs heterojunction bipolar transistors (HBTs), and investigated their performances. Circuit design and simulation were performed using SPICE and LIBRA. A discrete AlGaAs/GaAs HBT with the emitter area of $1.5\times10\ \mu m^2$, used for the circuit fabrication, exhibited the cutoff frequency of 63 GHz and maximum oscillation frequency of 50 GHz. After fabrication of MMICs, we observed the very wide bandwidth of DC~15 GHz for a limiting amplifier from the on-wafer measurement. Ceramic-packaged limiting amplifier showed the excellent eye opening, the output voltage swing of 750 $mV_{p-p}$, and the rise/fall time of 40 ps, measured at the data rates of 10-Gbit/s.

## I. Introduction

More capacity and higher speed communication systems are needed to meet more complicated and specific requirements of customers. Up to date, transmission system has been reached a practical application level, and expected to be the backbone of broadband and integrated services digital networks(B-ISDN) for future multimedia services. High-speed limiting amplifiers have been widely used in optical and satellite communication systems. Fig. 1 shows the block diagram of a 10-Gb/s optical transmission system. For these applications, AlGaAs/GaAs heterojunction bipolar transistors(HBTs) are potential devices because of their excellent high-frequency performance, large current drivability, uniform threshold voltage, and high breakdown voltage[1-6].

In the typical fiber-optic systems, the optical receiver comprises a photo-diode(PD), a preamplifier, an AGC(automatic gain controlled) amplifier, a limiting amplifier, a clock recovery circuit, a decision circuit, and a DMUX(demultiplexer). A limiting amplifier must exhibit the constant output power over a wide input dynamic range as well as the wide bandwidth. The performances of the limiting amplifier are very important because its characteristics significantly affect the shape of the transmitted optical signal. Also, monolithic integration is required to realize small, very reliable, and light-weight systems.

This paper discusses the design and performance of a limiting amplifier as the principal electronic devices of 10-Gb/s optical transmission systems. In Section II, the fabrication and performances of devices used in the circuits are described. In Section III, the circuit design and the layout are focused. In Section IV, the frequency response and the eye diagram of the limiting amplifier package module are discussed. In Section V, the conclusion is given.

## II. Device Technology

HBT epi-layer structures, prepared by MOCVD on a 3-inch semi-insulating GaAs substrate, include an InGaAs emitter cap layer(800 Å), an AlGaAs emitter layer(2000 Å), a C-doped GaAs base layer(700 Å), and a GaAs collector layer(4000 Å), as shown in Table 1.

HBTs were fabricated by the semi-self-alignment process, where the spacing between emitter and base was 0.25 $\mu m$. An i-line stepper was used in all the photolithography processes. For the ohmic contacts of the emitter, base, and collector, Ti / Pt / Au, Ti / Pt / Au, and Ni / Ge / Au / Ti / Au metals were deposited sequentially on the HBT epi-structures using an electron beam evaporator. And these ohmic metals were alloyed simultaneously at 375℃ for 10-s in $H_2/N_2$ atmosphere, resulting in the specific contact resistances of $2\times10^{-6}$, $3\times10^{-5}$, and $7\times10^{-6}\ \Omega cm^2$, respectively. Each HBT was isolated by wet mesa etching and was deposited with PECVD-SiN film. Prior to the first metallization, via-holes were formed by MERIE (magnetically enhanced reactive

Manuscript received July 24, 1997; accepted October 23, 1997.

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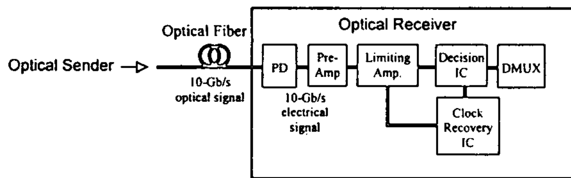


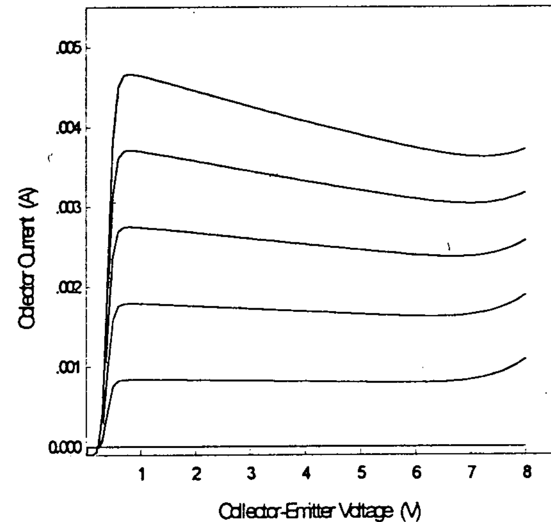

**Fig. 1.** Block diagram of a 10-Gb/s optical transmission system.

**Table 1.** AlGaAs/GaAs HBT epi-layer structures.

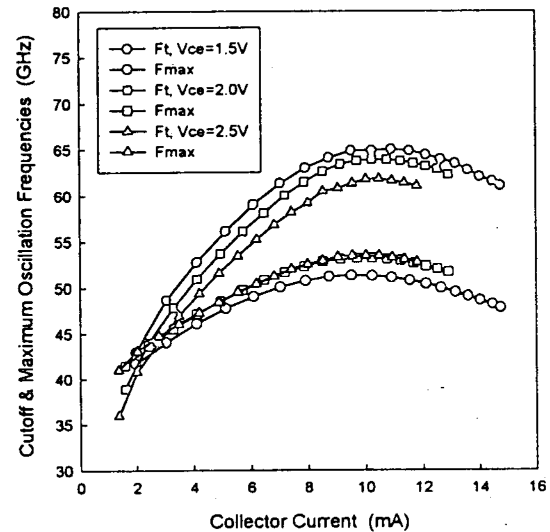
| Layer | | Thickness (Å) | Doping ($cm^{-3}$) | Al(In) Fraction |
|---|---|---|---|---|
| Cap | $n^+$-InGaAs | 400 | $1\times10^{19}$ | 0.5 |
| | $n^+$-InGaAs | 400 | $1\times10^{19}$ | 0 →0.5 |
| | $n^+$-GaAs | 1000 | $4\times10^{18}$ | |
| Emitter | n-AlGaAs | 500 | $5\times10^{17}$ | 0.3→0 |
| | n-AlGaAs | 1500 | $2\times10^{17}$ | 0.3 |
| Base | $p^+$-GaAs | 700 | $3\times10^{19}$ | |
| Collector | $n^-$-GaAs | 4000 | $2\times10^{16}$ | |
| Subcollector | $n^+$-GaAs | 5000 | $4\times10^{18}$ | |

ion etching) using $C_2F_6$ plasma. In addition to AlGaAs / GaAs HBTs, on-chip NiCr resistors (20Ω/sq) and capacitors were also utilized for fabricating 10-Gb/s MMICs. First- and second-level interconnects were provided by Ti/Au metals. Thick PECVD-SiN was used as both the inter-level dielectric and the MIM capacitor.

Fig. 2 shows the typical performances of HBTs with the emitter area of $1.5\times10\ \mu m^2$ used in circuits fabrication. As shown in the common-emitter I-V characteristics of Fig. 2(a), a collector-emitter offset voltage ($V_{CE}$) of 0.26 V, a forward breakdown voltage ($BV_{CEO}$) of 11 V, and a current gain ($\beta$) of about 50 are observed. And the ideality factors of the collector and base currents were 1.2 and 1.9, respectively. Microwave *S*-parameters were measured on wafer over the frequency range of 0.5 to 39.5 GHz using a HP8510B Network Analyzer and a CASCADE Microtech probe station, in which the current gain ($H_{21}$) and maximum available gain (MAG) were calculated from S-parameters. In Fig. 2(b), the cutoff frequency ($f_T$) and maximum oscillation frequency ($f_{max}$) of HBTs were 63 GHz and 50 GHz at a bias point of the circuit, respectively. Peak $f_T$ and $f_{max}$ were 67 GHz and 54 GHz. It was believed that these performances enabled to develop the limiting amplifier.




(a)




(b)

**Fig. 2.** Performances for HBTs used in circuits fabrication (a) common-emitter I-V characteristics (b) cutoff and maximum oscillation frequencies as a function of $V_{CE}$ and $I_C$ (emitter area: $1.5\times10\mu m^2$).

## Ⅲ. Circuit Design and Layout

A limiting amplifier must exhibit the low phase shift deviation between input and ouput signals and the constant output power over a wide input dynamic range at very high frequencies. Key feature of this circuit design is to utilize a differential configuration with emitter peaking technique to achieve both low phase deviation and wide bandwidth. The functional block diagram of designed limiting amplifier is shown in Fig. 3. It consists of an input buffer, two-stage differential amplifiers for high gain, an output buffer, and a feedback circuit for offset voltage control. It can be operated with differential or single input and output. It was reported that differential input and output effectively cancels the non-linearity of the input capacitances and remarkably reduces the phase deviation compared with single-ended input and output[1]. The input buffer includes an emitter follower with 50 Ω NiCr resistor to satisfy input impedance matching. A differential input signal is generated at the input buffer. The main amplifier employs a current feedback amplification circuit, so called a

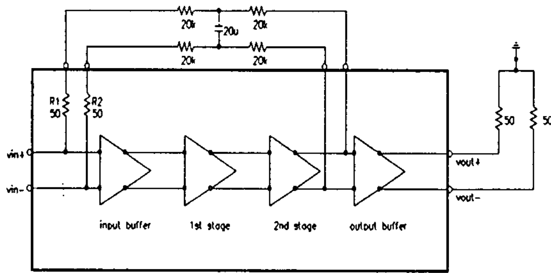



**Fig. 3.** Functional block diagram of the limiting amplifier.

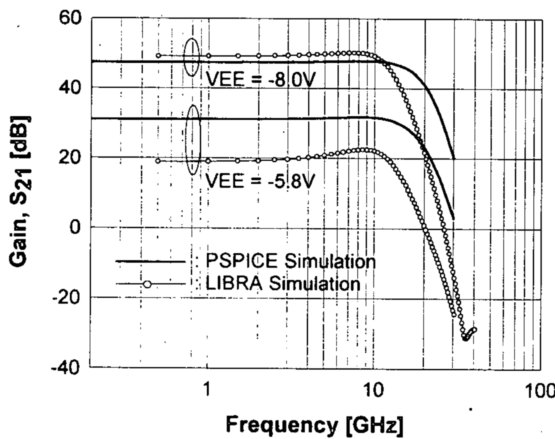



**Fig. 4.** Frequency responses of the limiting amplifier simulated by SPICE and LIBRA.

modified Cherry-Hooper(C-H) circuit, to obtain high small-signal voltage gain and broad bandwidth[5, 7]. The modified C-H circuit is basically constructed of two-stage differential amplifiers, two-stage output buffer, and a feedback resistor, where the feedback resistor is connected to the second amplifier through an emitter follower. To broaden the operating bandwidth and to lower the phase deviation, the output buffer uses an emitter peaking circuit which consists of series resistor and capacitor at the emitter. Each circuit block operates with its own reference current source to reduce the crosstalk. Single power supply of -8 V is used with the maximum power consumption of 1.5 W.

Firstly, the circuit was optimized using SPICE to determine the operating bias points at each circuit block. Parasitic capacitance and inductance due to the interconnections must be considered for better performance optimization at the bit rates exceeding 10-Gbit/s. Fig. 4 shows simulation results by SPICE and LIBRA at $V_{EE}$ = -8 V (ideal bias) and $V_{EE}$ = -5.8 V (real bias), respectively. It is observed from a gain bandwidth characteristic simulated using the SPICE that the bandwidth and the $S_{21}$ gain are DC~17 GHz and 48 dB at $V_{EE}$ = -8 V, and DC~17 GHz and 32 dB at $V_{EE}$ = -5.8 V, respectively. As a result of LIBRA simulation including various parasitic effects, the $S_{21}$ gain and the bandwidth are DC~

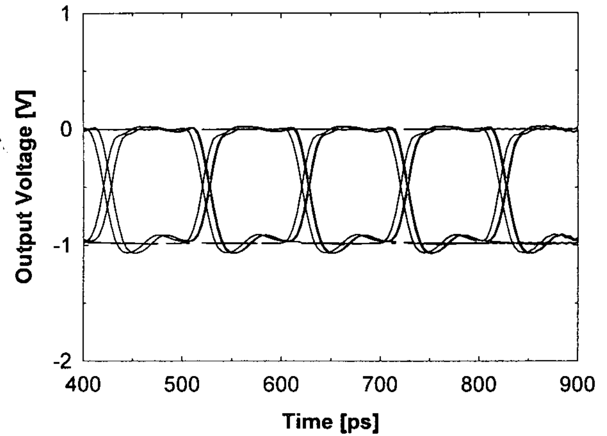



**Fig. 5.** Limiting amplifier output wave forms at 10-Gb/s obtained by LIBRA simulation.

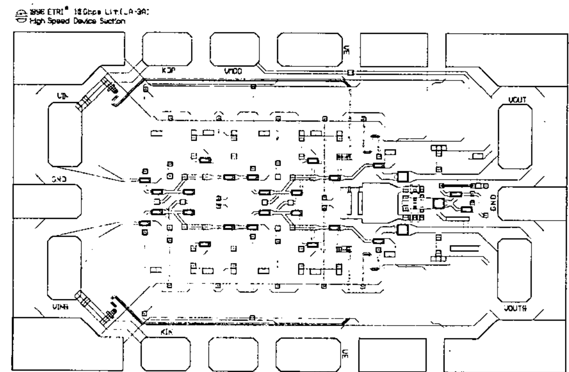


**Fig. 6.** Chip layout for the limiting amplifier (chip size: 1.0×1.2 $mm^2$).

12 GHz and 50 dB at $V_{EE}$ = -8 V, and DC~13 GHz and 20 dB at $V_{EE}$ = -5.8 V, and the characteristic peaking due to the emitter peaking circuit is also observed. The reduction of bias voltage ($V_{EE}$) significantly decreased the small-signal gain with the negligible bandwidth variation.

Pseudo-random pulse patterns were used as the input data signals, instead of periodic pulse patterns, to accurately estimate the circuit speed performance. An output eye diagram at 10-Gb/s of the limiting amplifier, obtained by LIBRA simulation, are shown in Fig. 5. For $V_{EE}$ = -8 V, output signal is limited to 900 $mV_{p-p}$ and relatively good eye crossings are observed in spite of a little bit eye undershooting and small timing jitter.

Fig. 6 shows a layout for the limiting amplifier. The chip size is relatively compact; 1.0×1.2 $mm^2$. The layout was carried out preserving the symmetry of the differential amplifier to reduce deviation between the layout and the processing. Input and output pads are located with the configuration of Signal-Ground-Signal (SGS) at left and right sides, respectively. And bias pads are placed symmetrically by the sequence of Ground-Power-Power-Power-Ground (GPPPG) at upper and lower sides. Pad pitch is

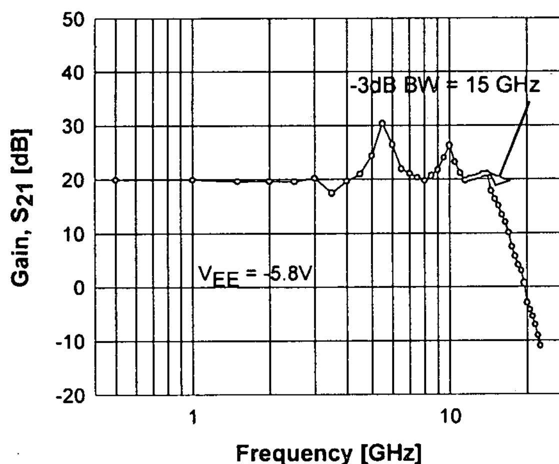



**Fig. 7.** Frequency response of the limiting amplifier.

fixed to 150 mm for on-wafer probing.

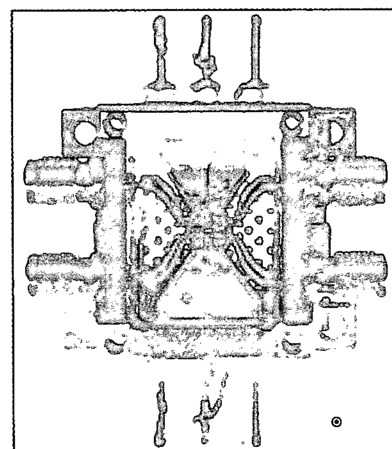
## Ⅳ. IC Performances

Prior to the packaging, the limiting amplifier fabricated by a MMIC process was tested with on-wafer RF probes. As shown in Fig. 7, the highest $S_{21}$ gain of 20 dB and widest bandwidth of DC ~15 GHz were obtained at $V_{EE}$ = -5.8 V lower than designed supply voltage ($V_{EE}$ = -8 V), which is due to assumedly occurrence of leakage current. These results approximately agreed with those of LIBRA simulation of Fig. 4, except for a little bit wider bandwidth. Supply voltage lower than designed value is responsible for the low small signal gain.

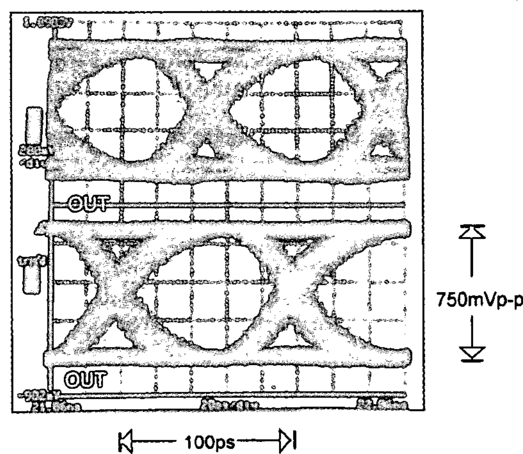
The limiting amplifier was lapped to the substrate thickness of 100 $\mu$m, metallized on its backside, mounted in alumina ceramic package, ribbon-bonded, and finally assembled in an Au-plated case module with SMA-connectors. Fig. 8(a) shows a photograph of the limiting amplifier package module. Eye patterns of the limiting amplifier were measured using an Anritsu 1763B Pulse Pattern Generator and a HP Sampling Oscilloscope. As shown in Fig. 8(b), when pseudo-random pulse patterns were used as the input data signals, clear and wide eye openings were observed, and the rise and fall times were about 40 ps from 20 to 80% of the output amplitude. The output voltage swing was limited to 750 $mV_{p-p}$ with input voltage ranging from 50 to 500 mV and the power consumption was less than 1.5 W with a supply voltage of -8 V. Measured timing jitter is approximately 20 ps. It is concluded that these results satisfy the principal design specifications of the limiting amplifier.

## Ⅴ. Conclusion

In summary, a limiting amplifier with the very wide bandwidth has been successfully designed, simulated, and implemented using high speed AlGaAs/GaAs HBTs. Typical HBTs used for the circuit showed the cutoff and maximum oscillation frequencies of 63 GHz and 50 GHz, respectively at a operating bias point. The measured gain bandwidth characteristics showed the bandwidth of DC~15 GHz and small signal gain of 20 dB on wafer, which well agreed with the results of simulation by LIBRA. After metal packaging we confirmed the symmetric clear eye diagram of the limiting amplifier module operating at the data rates of 10-Gbit/s.



(a)




(b)

**Fig. 8.** Photograph and output waveform of limiting amplifier package module. (a) IC chip mounted on a ceramic substrate. (b) 10-Gb/s eye diagram of limiting amplifier module.

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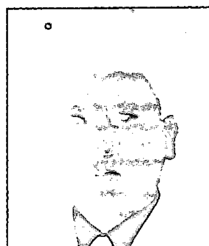

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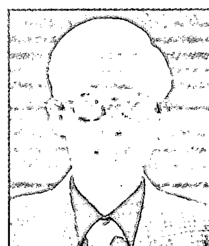

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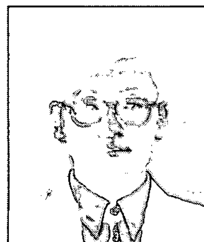
**Yeong-Seuk Kim**, for a photograph and biography, see p. 132 of the June 1997 issue(Vol. 2, No. 3) of this Journal.



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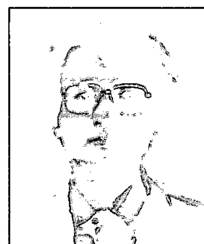

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