# Experimental Characterization-Based Signal Integrity Verification of Sub-Micron VLSI Interconnects

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## Abstract

Interconnect characterization on a wafer level was performed. Test patterns for single, two-coupled, and triple-coupled lines were designed by using 0.5um CMOS process. Then interconnect capacitances and resistances were experimentally extracted by using two port network measurements. Particularly to eliminate parasitic effects, the Y-parameter de-embedding was performed with specially designed de-embedding patterns. Also, for the purpose of comparisons, capacitance matrices were calculated by using the existing CAD model and field-solver-based commercial simulator, METAL and MEDICI. This work experimentally verifies that existing IC interconnect CAD models or parameter extraction may have large deviation from real values. The signal transient simulation with the experimental data and other methodologies such as field-solver-based simulation and existing models was performed. As expected, they significantly affect on the signal delay and crosstalk. The signal delay due to interconnects dominates the sub-micron-based gate delay (e.g., inverter). Particularly, coupling capacitance deviation is so large (about more than 45% in the worst case) that signal integrity cannot be guaranteed with the existing methodologies. The characterization methodologies of this paper can be very usefully employed for the signal integrity verification or the electrical design rule establishments of IC interconnects in the industry.

## I. Introduction

As the minimum feature size is shrinking down and switching speed which currently requires several GHz clock bandwidth becomes faster than before, IC interconnects play a pivotal role of the circuit performance[1-6]. Particularly, tighter physical spacing between the metals causes significant electromagnetic interference noises, i.e., crosstalk. Further, the signal delay due to interconnects dominates the critical path delay. Thus, the interconnects significantly affect on the overall performance of the today's circuits. Since the crosstalk may limit the overall chip size as well as packing density and the signal delay may limit the overall circuit speed, interconnect design is a kind of important issues in modern high-speed and high-density VLSI circuit design.

The most simplest interconnect model is RC model. The RC model can afford to be readily integrated into any existing CAD tools for signal integrity simulation. Thereby, with this RC model, many of the integrated circuit timing verification and noises can be predicted. The key thing to be done is to extract the accurate values of both R and C.

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The resistance can be readily monitored by sheet resistance measurements. However, capacitance characterization needs careful treatments as well as parasitic calibration during the measurements. Therefore, many works have been reported for extraction of the capacitances [7-10]. There are numerous techniques to calculate the capacitances. Among them, empirical fitting expressions or software packages such as RAPHAEL, MEDICI, METAL, and MAXWELL have been usually employed in the industry to yield the interconnect capacitances. Although the empirical models are simple, they may have a fundamental limitation in accuracy. In contrast, the field-solver-based software packages may yield the more accurate values than the empirical expressions if the simulation environments are carefully adjusted for reliable data. However, both methodologies cannot fully reflect the realistic situations such as process variations and non-ideal characteristics of the devices. Such deviations from the ideality become more serious as the deep-sub-micron process technologies come true. Possibly the circuit designers must cope with the more challenging interconnect problems as the next generation process technologies, i.e., nano-technologies, come near at hands. Thus, the experimental verification of the interconnect models is essential for guaranteeing the signal integrity of the modern high performance VLSI circuits.

This work presents a novel experimental-characterization of the multiple interconnect lines. To verify the accuracy of the existing

models and simulation methodologies, new test patterns for experimental characterizations were designed and fabricated by using the advanced 0.5 ㎛ CMOS process technology. Furthermore, the parasitic calibrations have been performed with newly developed de-embedding patterns. The parasitic pad de-embedding has been performed with Y-parameter de-embedding[11]. Then experimental data and simulation are compared with each other. Not only the realistic interconnect structures have inherent problems due to non-ideality, but also the simple CAD models have the deficiency in their accuracy. Thus, the experimental characterization and its data analysis are essential parts of the circuit design. The paper is an important contribution to the experimental characterization methodologies for new process developments and establishments of the circuit design rules pertinent to IC interconnects.

The paper is organized as follows. The necessary theory for the experimental characterization is presented, followed by the experimental data analysis. Then the existing CAD models and simulation are compared with the experimental data. Next, the signal transient simulation based on existing parameter extraction and experimental data are performed. Finally, the paper is summarized and concluded.

## II. Theory for Experimental Characterization of Interconnects

### *1. Test Pattern Design*

To experimentally characterize the interconnect capacitances and resistances, various test patterns were designed and fabricated by using 0.5 ㎛ twin-tub CMOS process technology. The layouts of the test patterns are shown in Fig. 1. The cross-section of test patterns of triple-coupled lines are shown in Fig. 2. The p-type silicon substrate doping concentration is $1\times10^{15}cm^{-3}$ and nominal metal thickness 7000Å, and the field oxide thickness between the top of silicon and the bottom of metal-I is 1.5 ㎛, respectively. Nominal oxide thickness between the top of silicon and bottom of poly is 3500Å and that of metal-I to metal-II, i.e., IMD, is 1.㎛. Minimum metal-I spacing is 0.8 ㎛. The signal line structures have 0.7 ㎛ and 1.4 ㎛ width, respectively. The test patterns of two- and triple-lines have 0.8 ㎛ spacing and 0.7 ㎛ width.

### *2. Mathematical Formulation for Two-Port Capacitance Measurements*

Interconnects are physically modeled as n-conductor system. In the n-conductor system, the charge equation of i-th conductor can be written as

$$Q_i = C_{ii}V_i + \sum_{j=1, j\neq i}^{n} C_{ij}(V_i - V_j) \quad (1)$$

where $C_{ii}$ is the self-capacitance of i-th conductor and $C_{ij}$ is the coupling capacitance between i-th and j-th conductor. Since capacitance measurements or numerical calculation can be readily performed with two-terminal network configuration, new capacitance which is analogous to the node admittance matrix[10] is defined as

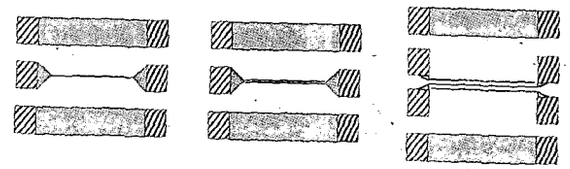



**Fig. 1.** Layouts of test patterns. (a) single line (b) two-coupled lines (c) triple-coupled lines (d) open pad for Y-parameter de-embedding

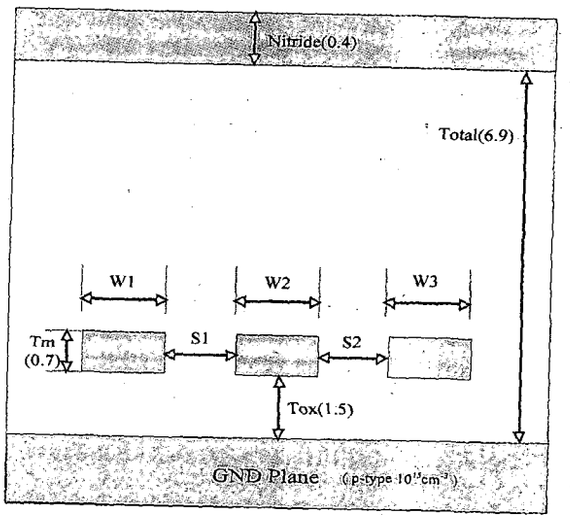



**Fig. 2.** Cross-sections for field-solver-based simulation of triple line interconnect capacitances : dimension is ㎛

$$C_S = \begin{bmatrix} C_{s11} & \cdots & \cdots & C_{s1n} \\ \vdots & \ddots & & \vdots \\ C_{sn1} & \cdots & \cdots & C_{snn} \end{bmatrix} \quad (2)$$

where diagonal components and off-diagonal components have the following relationships

$$C_{sii} = \sum_{j=1}^{n} C_{ij}$$
$$C_{sij} = -C_{ij} \quad (3)$$

Then (1) can be rewritten with admittance matrix components

$$Q_i = \sum_{j=1}^{n} C_{ij}V_i - \sum_{j=1, j\neq i}^{n} C_{ij}V_i \quad (4)$$

Now since the measurement system is fundamentally two-port network, n-conductor system must be modified to the two port system. Then its repetitive measurements can gives the experimental data. The two port measurement system can be mathematically presented as [7]

$$V_i = V \quad \text{if} \quad i \in A$$
$$V_i = 0 \quad \text{if} \quad i \notin A \quad (5)$$

where A is active node set. Then the measured capacitance between node set $x \in A$ and node set $y \notin A$ is

$$C_{measure} = \sum_{i=A} \frac{Q_i}{V} \quad (6)$$

Thus, n-port network capacitance can be extracted as two port network measurements by using (6). That is, several independent node set measurements can yield the self and coupling capacitances. The capacitances have been extracted with Kiethly 590 and HP4275 LCR meter. In order to get the reasonable data in our measurements, we assumed that

1. all the conductors are perfect conductors for capacitance measurements
2. very high frequency effects which may not define real open circuits are negligible
3. external electromagnetic noise is negligible

Since the measurements were performed on 1MHz or below, the above assumptions are very reasonable. Moreover, since other noise sources such as connectors, cables, and equipments can be eliminated during the pad-parasitic de-embedding processes, the reliable data can be achieved. To maintain the consistent measurements, symmetry properties were also employed. Furthermore, in wafer-level characterizations, the parasitics may dominate all the measured data. That is, since the DUT(device under test) capacitances of all above test structures have sub-pF dimension which has the same amount as the parasitics, its calibration must be carefully performed. Therefore, both the equipment calibration and parasitic calibrations (i.e., de-embedding) are essential. To eliminate the parasitic effects, the pad parasitic de-embedding patterns (open pad) were redundantly designed. Then Y-parameter de-embedding was performed. During the experiments, some of data were discarded if the data violate fundamental physics law due to electrical short or open. The experimentally extracted capacitances are summarized in Table 1-Table 3. Table 4 shows the deviation of existing methodologies from experiments. The % error in the table was calculated by using the experimental data as a reference.

**Table 1.** Measured capacitances of single line.

| Die# | Width : 0.7[㎛] | Width : 1.4[㎛] |
|---|---|---|
| | C1 [pF/cm] | C2 [pF/cm] |
| 1 | 0.844 | 1.07 |
| 2 | 0.826 | 1.06 |
| 3 | 0.826 | 1.06 |
| 4 | 0.815 | 1.05 |
| 5 | 0.826 | 1.06 |
| 6 | 0.826 | 1.05 |
| 7 | 0.826 | 1.05 |
| 8 | 0.822 | 1.05 |
| 9 | 0.841 | 1.07 |
| 10 | 0.833 | 1.06 |
| 11 | 0.837 | 1.07 |
| 12 | 0.822 | 1.06 |
| 13 | 0.837 | 1.07 |
| 14 | 0.811 | 1.05 |
| Ave. | 0.828 | 1.06 |

**Table 2.** Measured capacitances for two-coupled lines.

| Die# | Width : 0.7[㎛] | | Width : 1.4[㎛] | |
|---|---|---|---|---|
| | C11 [pF/cm] | C12 [pF/cm] | C11 [pF/cm] | C12 [pF/cm] |
| 1 | 0.753 | 0.500 | 0.962 | 0.585 |
| 2 | 0.746 | 0.490 | 0.956 | 0.553 |
| 3 | 0.751 | 0.503 | 0.959 | 0.559 |
| 4 | 0.744 | 0.496 | 0.950 | 0.550 |
| 5 | 0.756 | 0.513 | 0.947 | 0.569 |
| 6 | × | × | 0.944 | 0.560 |
| 7 | 0.749 | 0.515 | 0.947 | 0.574 |
| 8 | 0.749 | 0.512 | 0.949 | 0.569 |
| 9 | 0.756 | 0.528 | 0.954 | 0.582 |
| 10 | 0.753 | 0.507 | 0.957 | 0.560 |
| 11 | 0.750 | 0.506 | 0.957 | 0.565 |
| 12 | 0.753 | 0.503 | 0.954 | 0.556 |
| 13 | 0.757 | 0.507 | 0.963 | 0.550 |
| 14 | 0.746 | 0.491 | 0.954 | 0.538 |
| Ave. | 0.751 | 0.505 | 0.954 | 0.562 |

Note "x" means unstable data

### *3. Resistance Measurements*

Since interconnect can be simply modeled as RC network, the resistance must be also experimentally monitored with simple DC measurements. In facts, SEM (scanning electro-microscopy) picture of the cross-section is not enough to describe the process variation because it is only one aspect of innumerable cross-sections of long interconnects. Thus, the average of measurement data is considered. The theoretical resistance is

$$R = \rho \frac{l}{t \cdot w} = R_s \left(\frac{l}{w}\right) \quad (7)$$

**Table 3.** Measured capacitances for triple-coupled lines.

| Die# | Width : 0.7[㎛] , Capacitance [pF/cm] | | | | | |
|---|---|---|---|---|---|---|
| | C11 | C22 | C33 | C13 | C12 | C23 |
| 1 | 0.680 | 0.361 | 0.731 | 0.0397 | 0.491 | 0.487 |
| 2 | × | × | × | × | × | × |
| 3 | 0.680 | 0.363 | 0.727 | 0.0346 | 0.490 | 0.476 |
| 4 | 0.676 | 0.363 | 0.724 | 0.0346 | 0.479 | 0.465 |
| 5 | 0.676 | 0.355 | 0.715 | 0.0375 | 0.492 | 0.479 |
| 6 | 0.672 | 0.362 | 0.718 | 0.0375 | 0.483 | 0.470 |
| 7 | 0.673 | 0.358 | 0.718 | 0.0368 | 0.499 | 0.485 |
| 8 | 0.672 | 0.363 | 0.724 | 0.0390 | 0.498 | 0.488 |
| 9 | × | × | × | × | × | × |
| 10 | 0.679 | 0.362 | 0.707 | 0.0324 | 0.499 | 0.465 |
| 11 | 0.674 | 0.351 | 0.718 | 0.0441 | 0.496 | 0.484 |
| 12 | 0.673 | 0.352 | 0.719 | 0.0434 | 0.489 | 0.476 |
| 13 | 0.682 | 0.355 | 0.723 | 0.0419 | 0.486 | 0.477 |
| 14 | 0.675 | 0.341 | 0.711 | 0.0449 | 0.477 | 0.462 |
| Ave. | 0.676 | 0.357 | 0.720 | 0.0388 | 0.490 | 0.476 |

Note "x" means unstable data

**Table 4.** Experimental average, simulation, and empirical model of interconnect capacitance for the test patterns.
(a) single line (b) two-coupled lines (c) triple-coupled lines

(a) unit : [pF/cm]

| Width | Type | Exp_ave. | Simulation | Error(%) | Empirical | Error(%) |
|---|---|---|---|---|---|---|
| 0.7[㎛] | C1_self | 0.828 | 1.058 | + 22.7 | 1.002 | + 21.0 |
| 1.4[㎛] | C2_self | 1.060 | 1.250 | + 17.9 | 1.187 | + 11.9 |

(b) unit : [pF/cm]

| Width | Type | Exp_ave. | Simulation | Error(%) | Empirical | Error(%) |
|---|---|---|---|---|---|---|
| 0.7[㎛] | C11_self | 0.751 | 0.726 | − 3.3 | 0.701 | − 6.6 |
| | C12_couple | 0.505 | 0.732 | + 44.9 | 0.575 | + 13.8 |
| 1.4[㎛] | C11_self | 0.954 | 0.903 | − 5.3 | 0.827 | − 13.3 |
| | C12_couple | 0.562 | 0.775 | + 37.9 | 0.646 | + 14.9 |

(c) unit : [pF/cm]

| Width | Type | Exp_ave. | Simulation | Error(%) | Empirical | Error(%) |
|---|---|---|---|---|---|---|
| 0.7[㎛] | C11_self | 0.676 | 0.698 | + 3.2 | – | – |
| | C22_self | 0.357 | 0.423 | + 18.4 | 0.149 | − 58.2 |
| | C33_self | 0.720 | 0.698 | − 3.0 | – | – |
| | C12_couple | 0.490 | 0.699 | + 42.6 | 0.563 | + 14.8 |
| | C23_couple | 0.476 | 0.699 | + 46.8 | 0.563 | + 18.2 |
| | C13_couple | 0.0388 | 0.0630 | + 62.3 | – | – |

The resistance of the metal may have, in practice, large deviations from layout dimensions due to over etching or under etching although the contact resistance can be eliminated from the de-embedding process. Therefore, considering the process variations on metals, R may be bounded within the following inequality

**Table 5.** Measured resistances and their variatons.
(a) measured resistances (b) resistance variations; Note that each pattern shows about 4~6%, however, the resistance variations between 0.7㎛ and 1.4㎛ is about 10%, (c) resistance for circuit design.

(a)

| total length = 2700㎛, unit : [Ω] | | | | | |
|---|---|---|---|---|---|
| Die # | width | | Die # | width | |
| | 0.7[㎛] | 1.4[㎛] | | 0.7[㎛] | 1.4[㎛] |
| 1 | 290 | 145 | 8 | 308 | 135 |
| 2 | 278 | 130 | 9 | 302 | 139 |
| 3 | 292 | 135 | 10 | 316 | 137 |
| 4 | 292 | 137 | 11 | 295 | 133 |
| 5 | 309 | 143 | 12 | 298 | 137 |
| 6 | 315 | 139 | 13 | 297 | 136 |
| 7 | 309 | 140 | 14 | 296 | 133 |

(b) unit : [Ω (mΩ/□)]

| Width | R-ave | R-max | R-min |
|---|---|---|---|
| 0.7 | 299.78 (78) | 316 (82) | 278 (72) |
| 1.4 | 137.07 (71) | 145 (75) | 130 (67) |

(c) uint : [mΩ/□]

| R_ave | R-max | R-min |
|---|---|---|
| 75 | 82 | 67 |
| x | + 9.3% | − 10.6% |

$$R_s \frac{l}{W_{\max}} \le R \le R_s \frac{l}{W_{\min}} \tag{8}$$

Thus, for example, R with 5% variation may have

$$R_s \frac{l}{1.05 W_{\max}} \le R \le R_s \frac{l}{0.95 W_{\min}} \tag{9}$$

Since interconnects are thin-film conductors, sheet resistances were measured. The resistances were also calibrated by parasitic pad resistance measurements. The resistances for more than 10 dies of each different wafers were measured with HP4145. The experimental data are summarized in the Table 5.

## Ⅲ. Data Analysis of IC Interconnect Parameters

The capacitance calculation was performed by using the simulation and empirical models and compared with experimental data. The simulation meshes and all the dimensions are defined with nominal design rules, although there may be somewhat differences between real wafer structures and layout structures. The simulation structure definition for triple coupled lines as an example is shown in Fig. 2. Even if several oxide layers use different process technologies, their dielectric constants were assumed to be ideal value of 3.9. In addition, it is assumed that

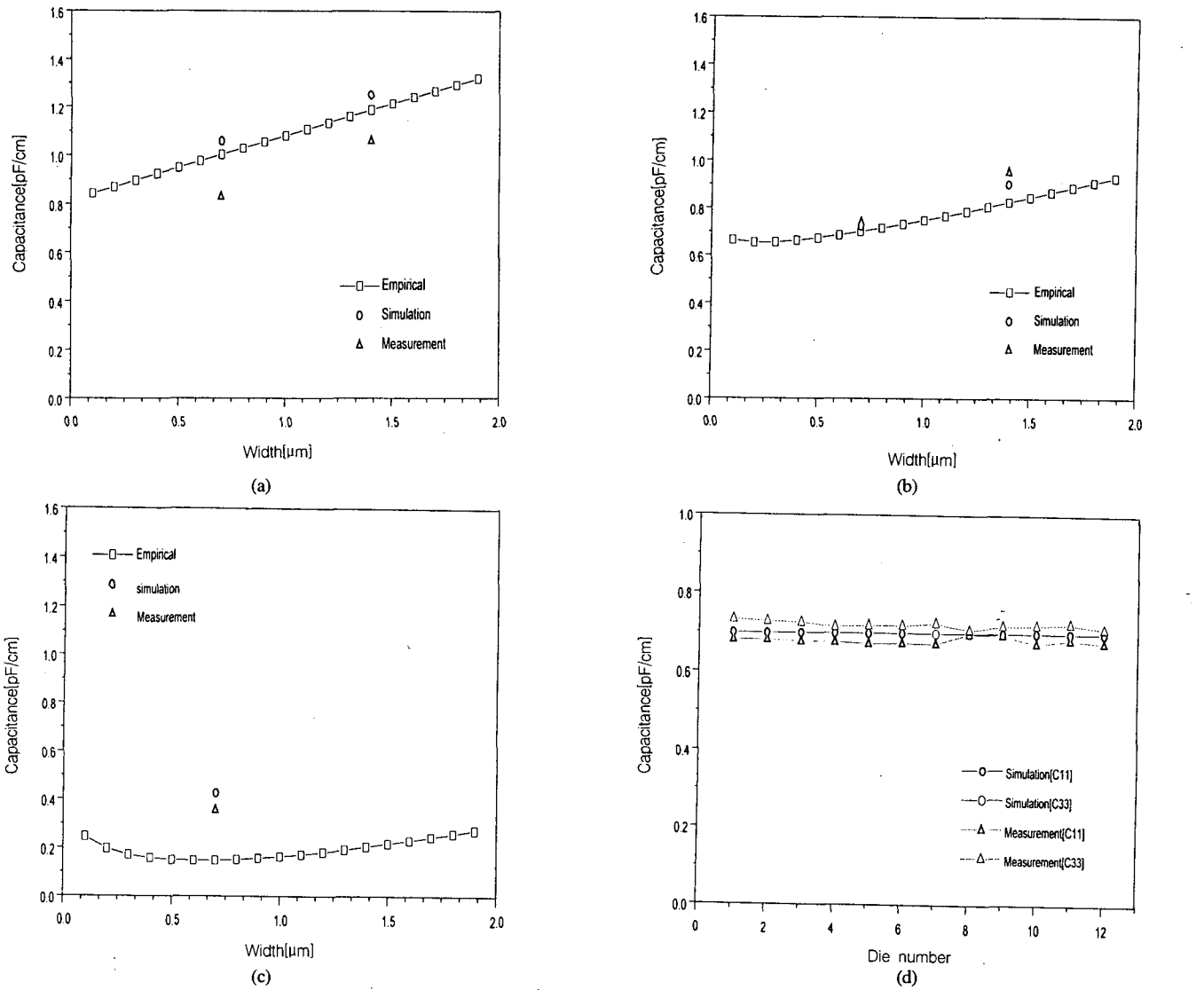



**Fig. 3.** Self-capacitance variation of test patterns with metal width.
(a) self-capacitance of single line, (b) self capacitance of two- coupled lines, (c) self-capacitance of center line of triple-coupled lines, (d) self-capacitance of outer line of triple-coupled lines

planarization throughout the structure is perfect during the simulation. In fact, such ideality may not be true. Thus, one of the goals in this work is to experimentally verify how the data under the ideal conditions deviate from real one. The difference between real environments and ideal one can be investigated through this experimental work. Then the well-known empirical capacitance models of[12] were employed for the CAD model verification. There, the self- capacitances are

$$C_1 = \varepsilon_{ox}\left[2.80\left(\frac{t}{h}\right)^{0.222} + 1.15\left(\frac{w}{h}\right)\right] \quad \text{for single line}$$

$$C_2 = C_1 + \varepsilon_{ox}\left[0.83\left(\frac{t}{h}\right) - 0.07\left(\frac{t}{h}\right)^{0.222} + 0.03\left(\frac{w}{h}\right)\right]\left(\frac{s}{h}\right)^{-1.34} \quad \text{for two couple lines} \tag{10}$$

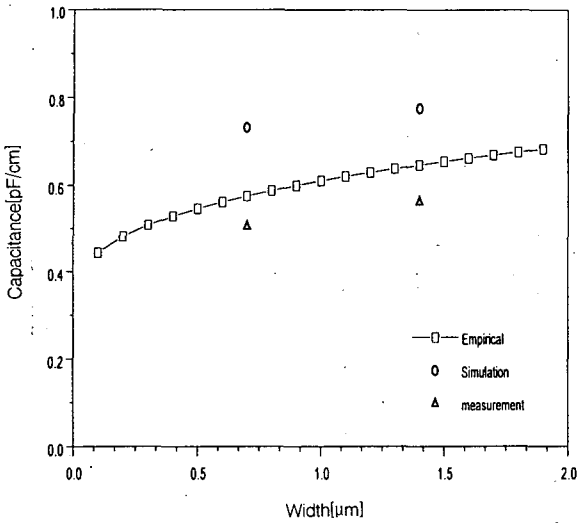
$$C_3 = C_1 + \varepsilon_{ox}\left[0.83\left(\frac{t}{h}\right) - 0.07\left(\frac{t}{h}\right)^{0.222} + 0.03\left(\frac{w}{h}\right)\right]\left(\frac{s}{h}\right)^{-1.34} \quad \text{for triple coupled lines}$$

The coupling capacitances are

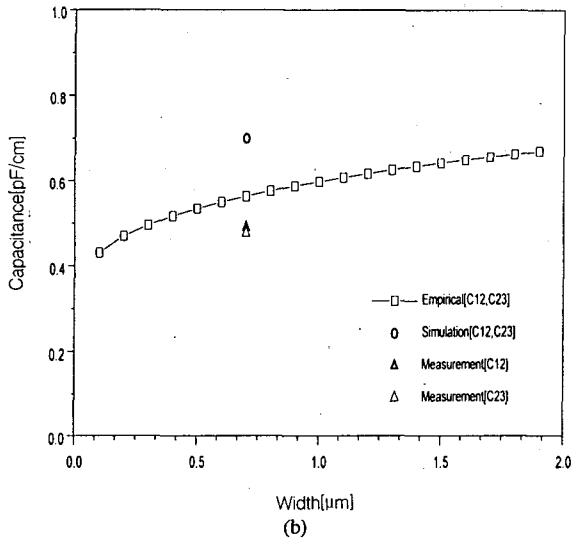
$$C_c^{two} = \varepsilon_{ox}\left[1.82\left(\frac{t}{h}\right)^{1.081} + \left(\frac{w}{h}\right)^{0.32}\right]\left(\frac{s}{h} + 0.43\right)^{-1.38} \quad \text{for two coupled lines}$$

$$C_c^{triple} = \varepsilon_{ox}\left[1.93\left(\frac{t}{h}\right)^{1.1} + 1.14\left(\frac{w}{h}\right)^{0.31}\right]\left(\frac{s}{h} + 0.51\right)^{-1.45} \quad \text{for two coupled lines} \tag{11}$$

These model-based capacitances and field-solver-based capacitances were plotted on Fig. 3 through Fig. 5. The self capacitance variations in Fig. 4 show that empirical model and simulation have about 20% deviation in sub-micron dimension. Particularly, the center line self-capacitance of empirical model in the triple lines is too large to be employed for timing verification. The coupling capacitance in Fig. 4 shows even worse deviations, i.e., more than 45% in the worst case. This is significant because




(a)




(b)

**Fig. 4.** Coupling capacitance variation of test patterns with metal space.
(a) coupling capacitance of two-coupled lines
(b) coupling capacitance of triple-coupled lines

coupling capacitance means crosstalk noise during the signal transients. In Table 4, experimental average, field-solver-based simulation, and empirical model are summarized. As they were shown, there is large difference between real and calculated values. Particularly, coupling capacitance difference which amounts to more than 45% results in such overestimation or underestimation of crosstalk and delay of real circuits as in parametric difference.

Moreover, in the fine lines, i.e., sub-micron process, fringing capacitance is significantly high. Thus, the fringing capacitances are investigated by using Yuan's model[13]. The fringing capacitance in[13] was modeled by using cylindrical approximation of the interconnect line

$$C_{fringing} = 2\varepsilon_{ox}\left\{\frac{\pi}{\ln\left(1+\frac{2h}{t}\left(1+\sqrt{1+\frac{t}{h}}\right)\right)}-\frac{t}{4h}\right\} \quad (12)$$

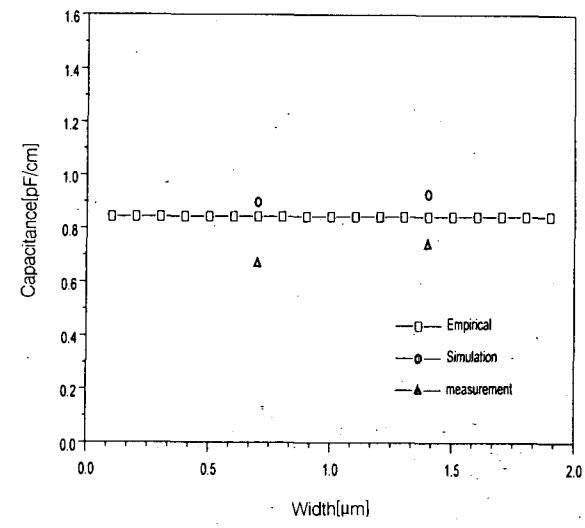



**Fig. 5.** Fringing capacitance for single interconnect lines.

That is,

$$C_{total} = \left(\frac{\varepsilon_{ox}}{h}\right) W + C_{fringing} \quad (13)$$

where the first term, $C_p = \left(\frac{\varepsilon_{ox}}{h}\right) \cdot W$, is parallel plate capacitance. The measured fringing capacitance can be given by

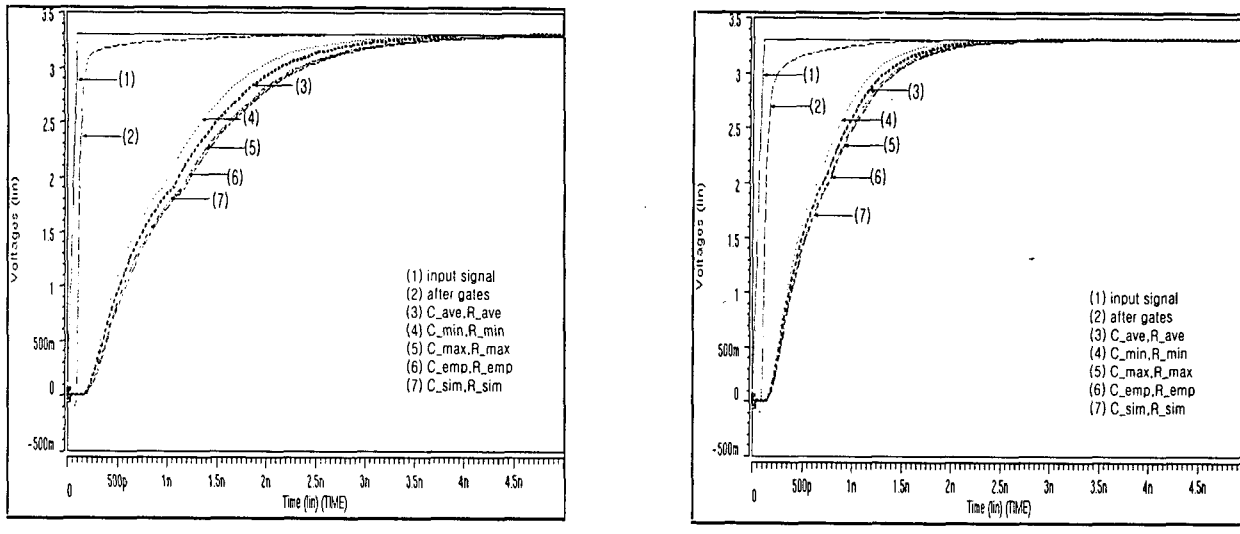
$$C_{fringing} = C_{total} - C_p \quad (14)$$

The fringing capacitances were compared in Fig. 5. As we can see in Fig. 5, the fringing capacitance also shows large deviations. Since[13] is based on relatively wide strip, it is not suitable for modern fine line interconnects.

In summary, whichever process technologies were employed for the circuit design, they have inherent process variations. Thus blind simulation or CAD model-based parameter extraction without experimental verification may cause catastrophic circuit failures. Since such process technology can not be avoided, simulation conditions and interconnect design rules must resort to the experimental work. That is, simulation environments and models must be adjusted based on the careful experimental data with test pattern design. In the next section, signal delay and crosstalk are investigated based on previous data.

## Ⅳ. Signal Delay and Crosstalk Based on Experimental Data

In this section, the effects due to RC parameter variation of exiting CAD model and experiment-based parameter extraction are investigated. If interconnect line parameter matrices are known, the time domain responses of the interconnects under generalized conditions can be obtained by inverse Fourier transform. The methodology was well verified with TDR/TDT measurements and S-parameter-based measurements[14]. However, for the resistive




(a) (b)

**Fig. 6.** Single line signal transients with experimental data, empirical model, and field-solver-based simulation.
(a) signal transients with width 0.7$\mu$m, (b) signal transients with width 1.4$\mu$m

Note that min, max, and ave mean experimental minimum, experimental maximum, and experimental average, respectively. For example, C_ave means experimental average capacitance. Further, emp and sim mean the empirical model and field-solver-based simulation, respectively. Length is 1cm long.

lines, segmented ladder network model can explain both magnitude and phase[15]. Thus, we modeled the interconnects as 10 segment RC ladder network for circuit simulation with HSPICE. For the simulation, BSIM model for transistors and Table 1~ Table 5 for RC were used. Then the signal delay and crosstalk based on experimental data and existing model are investigated. The single line signal transients for experimental data, field-solver-based simulation, and empirical data are shown in Fig. 6. Input signal rise time is 0.1nsec, i.e., (1) in Fig. 6. The (2) in Fig. 6 presents the signal after two inverter switching. Thus, 1cm long interconnect occupies the 85% of total delay in sub-micron interconnects. Similar results for multiple lines are shown in Fig. 7 and Fig. 8. Particularly, the crosstalk between lines as shown in Fig. 7-(b) and Fig. 8-(b) presents the significantly large deviations. Therefore, not only simple parameter extraction under the ideal condition can never guarantee the signal integrity as shown in Fig. 6, but the signal transient based on process variation cannot be neglected. Judging from authors experimental experiences, even for the very stable process, this kind of deviation always exist. Thus, the accurate interconnect simulation, not by blind simulation without any other verification, requires necessarily adjustments with the experimental work. Thereby the discrepancy between real signal variation and simulation can be reduced. Furthermore, the electrical design rules based on the similar methodology as in this papers must be established. That is, in more detail, length-, width-, and layer-based design rules of IC interconnects must be established for high-speed circuit design. This kind of work can guarantee the signal integrity of high-speed and high-density VLSI circuits. Thereby the circuit designers can design their circuits much more safely. For the process engineer, these kinds of data may give the directions for their process improvements. In addition, since many dynamic noises such as simultaneous switching noise, ringing, and reflections cause more serious design failure than before (i.e., low-speed circuits), the electrical design rules for IC interconnects beside the process-based design rules may become increasingly more important.

## V. Conclusion

The existing CAD models may be inaccurate because they cannot fully consider fringing effects, process variations, non-ideal physical constants, and etc. These cause the significant deviations from realistic parameter values which result in catastrophic failures of circuits. In this work, it has been experimentally verified. That is, this experimental work shows there are significant differences between the simulation and experimental data. Although these limited experiments are not sufficient to conclude general statements, much concern with simulation data is required. There are some simulation uncertainties such as non-ideal dielectric constant, non-uniformity of process parameters, and other process variations. Nonetheless, some of the self-capacitances in many cases have excellent agreements with experiments but coupling capacitances are not the case. These coupling capacitances are very important circuit parameters to determine the interconnect design rules which are directly related with packing density. Furthermore, timing verification due to interconnects is also highly related to this parameter. Particularly, the inaccuracy of coupling capacitance and center line self-capacitance inaccurately estimate both timing and coupling noise. These make global

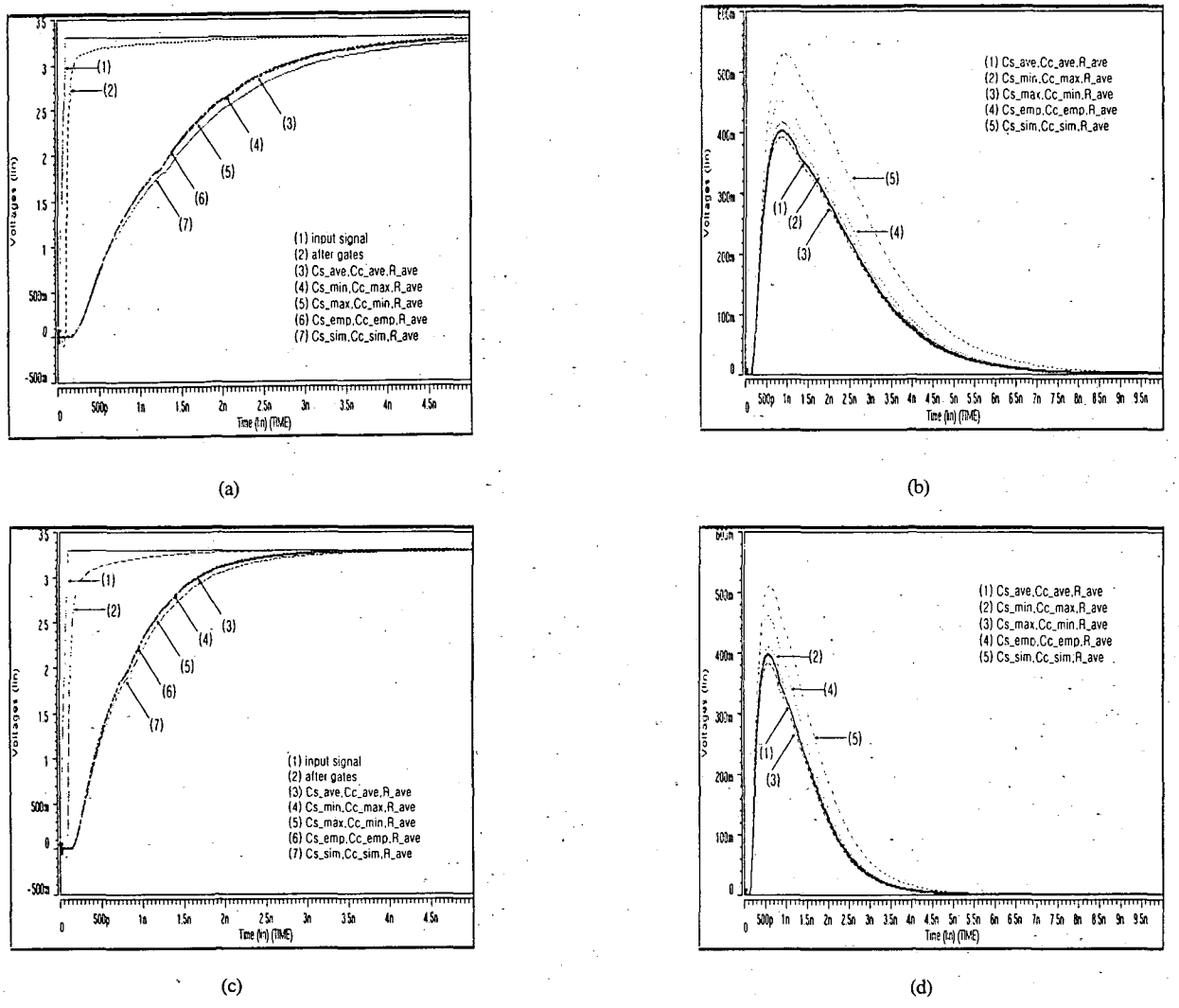



**Fig. 7.** Signal delay and crosstalk of 1cm long two-coupled lines.
(a) signal transient for dealy (0.7$\mu$m width, 0.8$\mu$m spacing), (b) signal transient for crosstalk (0.7$\mu$m width, 0.8$\mu$m spacing), (c) signal transient for dealy (1.4$\mu$m width, 0.8$\mu$m spacing), (d) signal transient for crosstalk (1.4$\mu$m width, 0.8$\mu$m spacing)

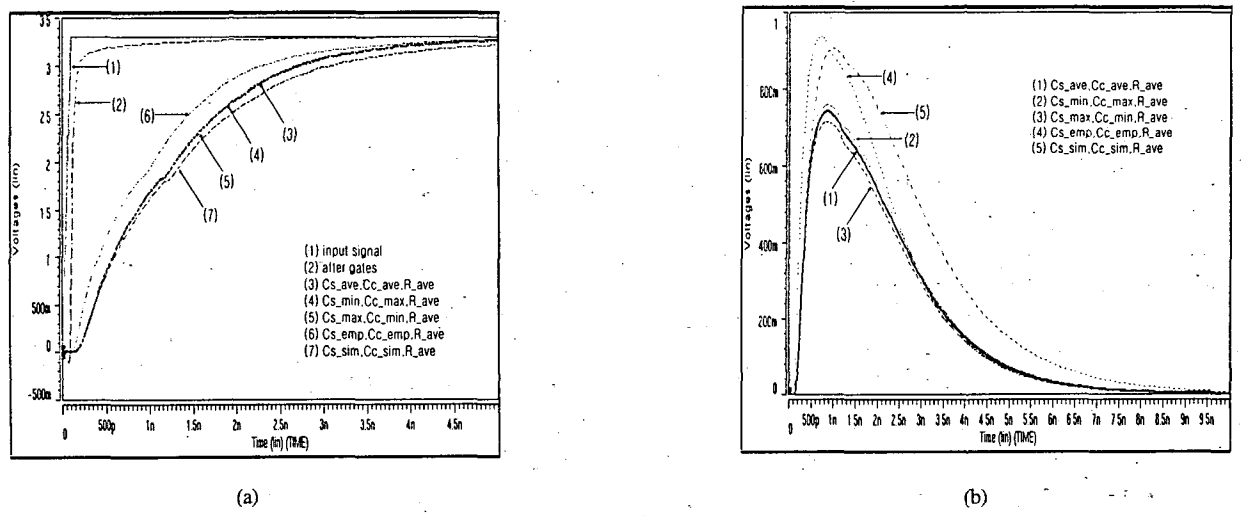



**Fig. 8.** Signal delay and crosstalk of 1cm long triple-coupled lines. (a) outer line signal transients for delay (0.7$\mu$m width, 0.8$\mu$m spacing), (b) center line signal transients for crosstalk (0.7$\mu$m width, 0.8$\mu$m spacing)

routing such as clock circuit design and critical path design difficult and significantly reduce circuit design flexibility.

As the process technology is advanced, more higher packing density will be tried. At the same time, circuit switching speed will be more increased in order to meet high performance circuit design specification. Such technological trend necessitates much more stringent interconnect characterization. This paper can be readily applied for such experimental data base and electrical design rule establishments of IC interconnects. This work is an important contribution to the existing CAD model verification, the process improvements for integrated circuit interconnects, and the detailed interconnect design rule for IC interconnects.

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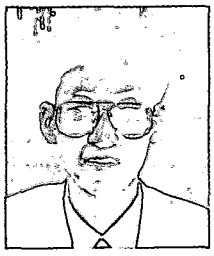

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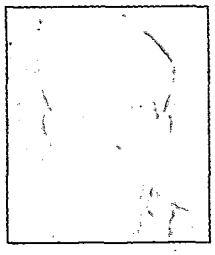

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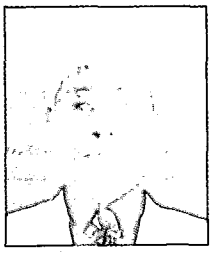

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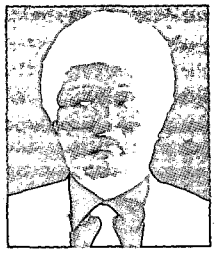

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