Fabrication and Characterization of Self-Aligned Recessed Channel SOI NMOSFETs

Jong-Ho Lee

Abstract

A new SOI NMOSFET with a 'LOCOS-like' shape self-aligned polysilicon gate formed on the recessed channel region has been fabricated by a mix-and-match technology. For the first time, a new scheme for implementing self-alignment in both source / drain and gate structure in recessed channel device fabrication was tried. Symmetric source / drain doping profile was obtained and highly symmetric electrical characteristics were observed. Drain current measured from 0.3 μm SOI devices with V_T of 0.77 V and Tox = 7.6 nm is 360 μA/μm at V_{GS} = 3.5 V and V_{DS} = 2.5 V. Improved breakdown characteristics were obtained and the BV_{DSS} (the drain voltage for 1 nA/μm of I_D at V_{GS} = 0 V) of the device with L_{eff} = 0.3 μm under the floating body condition was as high as 3.7 V. Problems for the new scheme are also addressed and more advanced device structure based on the proposed scheme is proposed to solve the problems.

I. Introduction

SOI MOSFET's have been studied extensively as candidates for low power and high speed integrated circuits mainly due to low parasitic capacitances. In addition, the devices have advantages in α-particle immunity, dielectric isolation, and so on[1].

Reduced BV_{DSS} (breakdown voltage between drain and source under the floating body condition) due to parasitic bipolar action under floating body condition is one of the disadvantages of SOI MOSFET's[2].

Another problem of SOI is the increase in the source / drain (S / D) resistance as the silicon film thickness is reduced, even if a silicide process is adopted[3, 4]. One of the methods to alleviate the problem is to adopt a recessed channel structure[5, 6]. However, one of the problems in the conventional recessed channel devices is that the polysilicon gate in the recessed channel structure is not self-aligned to the recessed region[5, 6], and the devices may have asymmetric characteristics.

In this paper, a new method to fabricate a SOI device with self-aligned polysilicon gate on the recessed channel region is proposed. New features in the device include self-alignment between S / D and polysilicon gate in the recessed channel scheme, low S / D resistance, and improved breakdown characteristics. Problems related to the new scheme will be shown and more advanced device structure based on the self-alignment scheme will be given to solve the problems.

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J. H. Lee is with School of Electrical Eng., Wonkwang Univ., Shinyong-Dong 344-2, Iksan Chonpuk 570-749, Korea.

II. Device Fabrication

Fig. 1 shows the schematic key process steps for the new SOI device fabrication. The starting SIMOX wafers have silicon film thickness of 211 nm and buried oxide thickness of 380 nm. Relatively thick Si film is selected by considering a possible incorporation of lateral SOI bipolar device in the future[8]. Active layer was defined by optical photolithography. A 510 nm field oxide was grown for device isolation and the silicon film in the isolation region was consumed completely. After the removal of the 160 nm thick nitride film and pad oxide for typical LOCOS, a new 22 nm thick pad oxide is thermally grown, followed by the deposition of a 82 nm thick nitride film. E-beam lithography was adopted to define the channel region as shown in Fig. 1 (a). The residual pad oxide was etched in a wet solution. Then a LOCOS-like oxide with thickness of 328 nm was grown (b), which consumed about 147 nm of Si. The recess oxide is etched in 7 : 1 BHF solution. Thin oxide (10 nm) was grown and followed by V_T implantation with energy of 35 keV and BF_2^+ dose of 1×10^{13} cm^{-2}, respectively, as shown in Fig. 1 (c). After the thin oxide was removed, gate oxide of 7.6 nm thick was grown and 295 nm thick polysilicon was deposited as shown in Fig. 1 (d). The polysilicon gate was formed in a self-aligned manner on the recessed channel region without any margin limited by layer-to-layer registration. The polysilicon film was doped by $POCl_3$ and the resultant sheet resistance measured from monitor wafer is 29 Ω/□. It is expected that the 'LOCOS-like' shape polysilicon gate has slightly larger sheet resistance than that of monitor wafer. Photolithography for the definition of

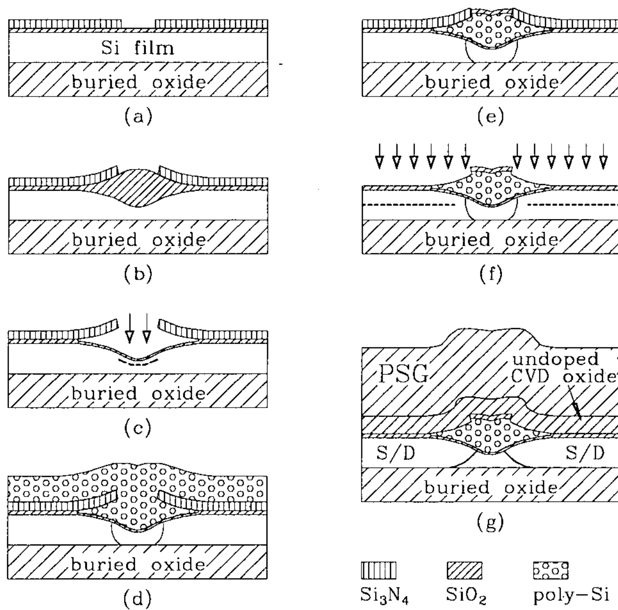

Fig. 1. Schematic cross-sectional view of key process steps for self-aligned recessed channel SOI device fabrication. Step (g) shows final cross section of the device.

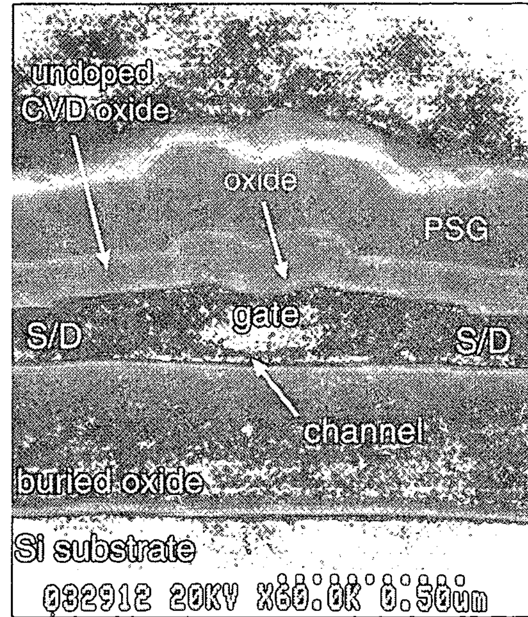

Fig. 2. SEM cross-sectional view of the fabricated self-aligned recessed channel SOI device. Polysilicon and silicon regions are stained in chemical solution for resolution enhancement. The severely stained polysilicon gate has LOCOS-like shape. All notations and structure of this figure can be compared to those of Fig. 1 (g).

polysilicon gate contact region was performed. Following process steps are adopted to protect the filled polysilicon in the recessed channel region when the polysilicon over nitride film is removed to just deposited thickness. Dry etching of 270 nm thick polysilicon film was performed, followed by complete wet oxidation of residual polysilicon over nitride film at 850℃ and oxide strip to remove oxidized polysilicon over nitride film only. Then a 40 nm thick oxide was selectively grown to protect the defined polysilicon gate region as shown in Fig. 1 (e). Fig. 1 (f) shows the S / D implantation after the nitride removal. Phosphorus ions were implanted first with a dose of 1.5×10^{14} cm^{-2} and an energy of 65 keV, followed by arsenic ion implantation with dose of 5×10^{15} cm^{-2} and 80 keV energy. Parts of implanted ions can pass through the taper polysilicon region to form the deep graded S / D doping profile. The S / D annealing was performed at 910℃ for 30 min. The rest of the process steps are similar to a typical CMOS process. Fig. 1 (g) shows a cross-sectional view of the final device structure.

Fig. 2 shows SEM cross-sectional view of the fabricated device. All notations and structure can be compared to those in Fig. 1 (g). The severely stained polysilicon gate has a 'LOCOS-like' shape. Effective gate length of the MOSFET in this figure is about 0.4 μm which is confirmed by process simulation based on the practical device structure obtained by SEM. Defined channel open length (L_{MASK}) for the L_{eff} of 0.4 μm is 0.35 μm, and the relation between L_{MASK} and L_{eff} can be changed by controlling lateral diffusion of S / D. To increase integration density and reduce overlap capacitance, the polysilicon in taper region of the gate (shown in Fig. 1 (e)) can be removed by anisotropic dry etching using top oxide as a self-aligned mask shown in Fig. 1 (f).

Fig. 3 shows the SEM top view of the fabricated self-aligned RC SOI device of L_{eff} = 0.3 μm. The picture was taken after the formation of contact hole. There is a step between gate and S / D regions in conventional CMOS devices. But it is not found in this new structure, since the polysilicon gate was recessed in the self-aligned manner. Polysilicon region for gate contact is shown in bottom side and the region is formed through not filling but masking. White particles with irregular size are just dust incorporated in SEM sample handling.

III. Device Characteristics

The fabricated SOI NMOSFET's have a final Si film thickness of about 200 nm in the S / D region and 50 nm in the channel region. Fig. 4 shows the I_D-V_{DS} characteristics of partially depleted SOI NMOS device with L_{eff} = 0.3 μm and V_T of 0.773 V. The I_D-V_{DS} curves were measured under floating body condition and showed the characteristics of partially depleted device, which is due to the high impurity concentration ($\sim10^{18}$ cm^{-3}) in the thin channel region. Since very symmetric S / D was formed as shown in Fig. 1 (f), perfectly symmetric I_D-V_{DS} characteristics were obtained. The device shows a fairly high current drivability and very good breakdown characteristics. The improvement of the breakdown characteristics is mainly due

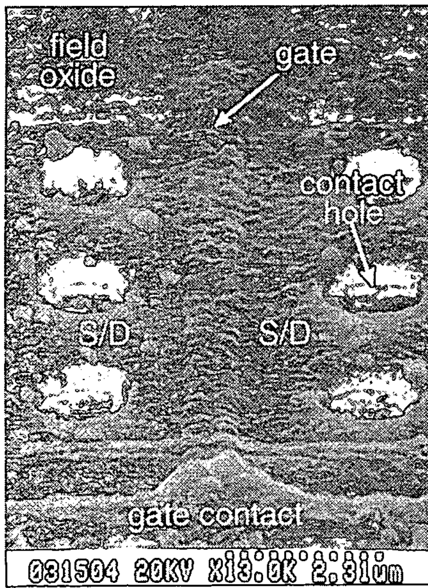

Fig. 3. SEM top view of the self-aligned recess channel device with effective channel length of 0.3 μm.

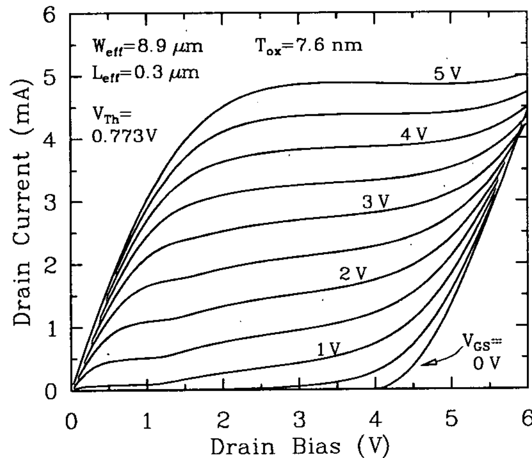

Fig. 4. Measured I_D-V_{DS} characteristics of self-aligned recessed channel SOI device with W_{eff} / L_{eff} of 8.9 / 0.3 and V_T of 0.773 V. The effective channel length was determined by simulating the device structure based on the practical SEM pictures.

to the gradually doped S / D formed by ion implantation through the taper polysilicon, which is formed in the birds beak region, shown in Fig. 1 (f) and selective V_T implantation into the channel region as shown in Fig. 1 (c). This gradual doping reduces both the impact ionization near the drain and the emitter injection efficiency of the parasitic bipolar transistor near the source [9]. It is also expected that the taper polysilicon gate may reduce the impact ionization. The drain voltage in which I_D reaches 1 nA/μm at V_{GS} =0 V under floating body condition is as high as 3.7 V

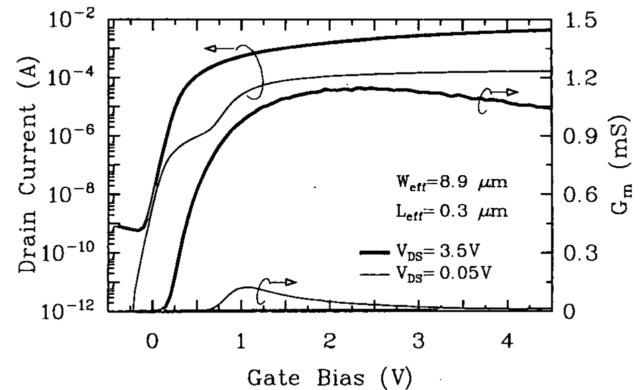

Fig. 5. Measured subthreshold and transconductance characteristics with gate bias under the floating body condition.

regardless of the parasitic side channel.

Fig. 5 shows measured subthreshold and transconductance (G_m) characteristics with gate bias under the floating body condition. The transconductance characteristics are reasonable. Subthreshold characteristics at V_{DS} of 0.05 V show the kink, which is due to the parasitic side channel formed in the channel width direction. Subthreshold swing of main channel was not extracted, since the parasitic channel characteristics affect strongly. The subthreshold at V_{DS} of 3.5 V shows very good characteristics but large GIDL current. Typical floating body SOI NMOS with L_{eff} of 0.3 μm shows the breakdown at V_{DS} = 3.5 V caused by parasitic bipolar action. But proposed device cannot show the breakdown at V_{DS} of 3.5 V, let alone nearly 4 V. Large GIDL current at V_{DS} of 3.5 V is due to the large overlap length ($\sim$0.4 μm) between gate and S / D, which can be small by reducing the overlap length as mentioned above.

Fig. 6 shows drain current and BV_{DSS} characteristics as a function of effective channel length. The BV_{DSS} data are very good and indirectly compared with those of references [2, 10] where off-state current limit is 0.1 $\mu A/\mu m$. In Fig. 6, the current limit is more tight and the value is 0.1 nA/μm. Drain current decreases as the channel length increases as expected. However I_D increases slightly from L_{eff} of 0.55 μm. BV_{DSS} increases with the increase of L_{eff} up to 0.5 μm and then decreases again. These anomalous phenomena can be explained in detail in Fig. 8.

Fig. 7 shows threshold voltage and $G_{m,max}$ characteristics with effective channel length. G_m decreases as the channel length increases. As the channel decreases, the threshold voltage decreases and the decrease at 0.3 μm is about 16% to the maximum value. The threshold voltage of devices with the channel length larger than 0.5 μm decreases, which will be explained in next figure.

The anomalous effects shown in Figs. 4, 5 and 6 can be explained by considering the relation between the channel open length (Fig. 1 (a)) and the thickness of deposited polysilicon gate (Fig. 1 (d)). Fig. 8 shows SEM cross-sectional view of the

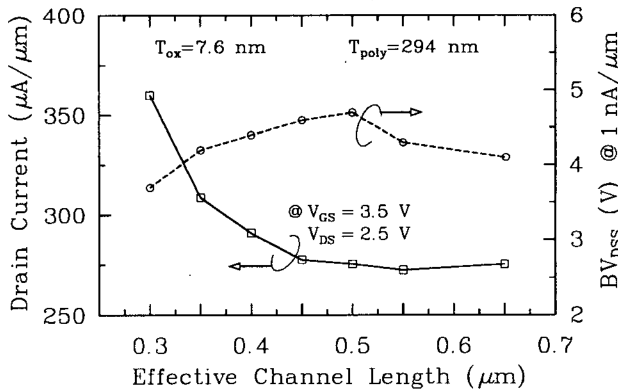

Fig. 6. Measured drain current and BV_{DSS} characteristics with effective channel length. The BV_{DSS} is defined as the drain voltage that drain current reaches at 1 nA/μm under floating body condition when gate bias is 0 V.

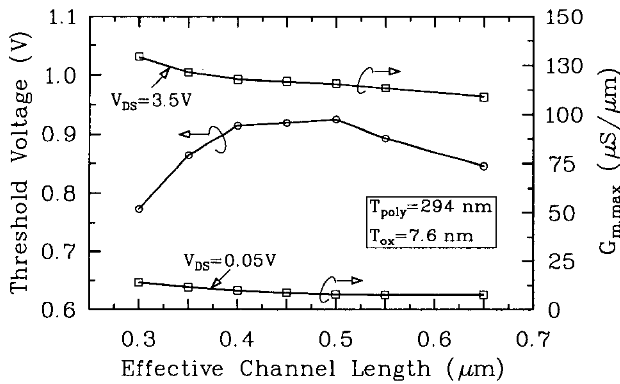

Fig. 7. Threshold voltage and maximum transconductance characteristics with effective channel length.

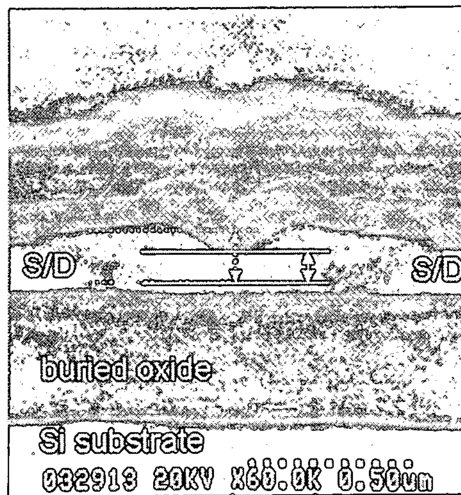

Fig. 8. SEM cross-sectional view of the 0.5 μm SOI device. Polysilicon gate thinning of center region is clearly seen. The dotted line represents the polysilicon thickness of the device with effective L_{eff} of 0.4 μm.

0.5 μm SOI device and can be compared with the Fig. 2. When the gate open length is large, there exists a thin polysilicon gate region over the center of the channel region after polysilicon etch-back (step (e) of Fig. 1). The thin polysilicon gate may not be able to block impurity ions during the source / drain implantation (step (f)). If we increase the polysilicon thickness in step (d), these anomalous effects will be observed at larger gate open length. On the other hand, if the device size scales down at fixed polysilicon gate thickness, we can observe good device characteristics at relatively long channel. According to the recent trend of device scaling, proposed self-aligned scheme will be guaranteed indeed and may have a potential in a 0.1 μm or less device size.

Ⅳ. Advanced Self-Aligned Recess Channel MOS Structure

Improved process sequence based on the self-aligned scheme is given in Fig. 9 to solve the announced problems without increasing process complexity.

Fig. 9 shows key process steps for the fabrication of the scaled self-aligned recess channel MOS devices. The improved process flow is based on the self-aligned scheme as mentioned previously. Overall process steps are nearly same as those of Fig. 1. Now we consider key features of the structure over one shown in Fig. 1. First the recess oxide (step (b)) can be optimized for best device performance. But the recess oxide thickness in Fig. 1 should be determined by process parameter, since the final 'LOCOS-like' gate thickness depends on strongly the

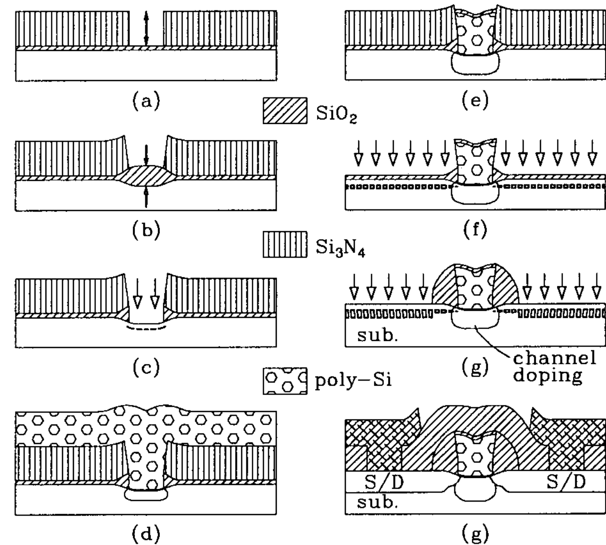

Fig. 9. Key process steps for the fabrication of the scaled self-aligned recess channel MOS device. Arrow marks in (a) and (b) represent the change of the nitride thickness and the recess oxide thickness, respectively.

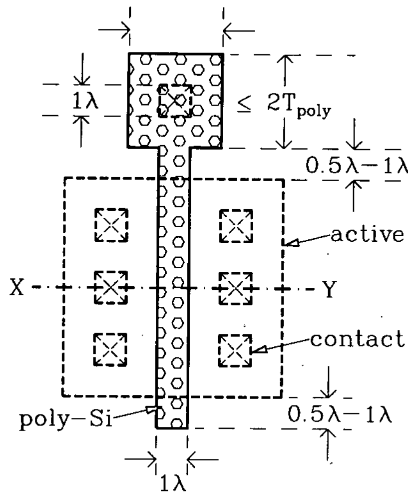

Fig. 10. Key layer layout and related design rule of the scaled self-aligned recess channel device.

recess depth. Second it is expected that only one mask step is used to define polysilicon gate. So added process complexity is not severe in implementing the self-aligned recess channel device.

Fig. 10 shows layout and related design rule of the self-aligned recess channel device. The design rule is based on polysilicon filling method for gate formation. The rule was determined by considering the open width of polysilicon pattern and the thickness of deposited polysilicon film. The polysilicon gate or pattern is formed by depositing and etching back the polysilicon. Maximum polysilicon pattern size must be less than two times polysilicon thickness to guarantee the filling method. For example, we adopt 200 nm thick of the polysilicon gate in 0.1 μm technology, maximum polysilicon pattern size should be less than 0.4 μm. In this case maximum channel length may be 0.4 μm and the length is long in 0.1 μm technology. If the device size is scaled down less than 0.1 μm, we can of course obtain relatively longer channel length.

V. Conclusion

We developed a new SOI device with a self-aligned polysilicon gate on the recessed channel region and obtained low source / drain resistance, symmetrical I-V characteristics and very high breakdown voltage (BV_{DSS}). For the first time, the self-alignment was achieved in both source / drain and gate structure in recessed channel SOI device fabrication. The device needs no margin in layer-to-layer registration due to the self-alignment. Drain current measured on SOI NMOSFET with L_{eff} = 0.3 μm and V_T of 0.773 V is 360 $\mu A/\mu m$ at V_{GS} = 3.5 V and V_{DS} = 2.5 V. BV_{DSS} (the drain voltage for 1 $nA/\mu m$ of I_D at V_{GS} = 0 V) of the device with L_{eff} = 0.3 μm under the floating body condition was as high as 3.7 V. Also problems related to the new device structure are addressed and analyzed. Improved process sequence for the self-aligned recess channel MOS was proposed to solve the problems without increasing severe process complexity. The self-aligned recess scheme become significant as device size scales down, since the scheme guarantees relatively low source/drain resistance without deteriorating integration density. The improved device structure based on the self-aligned scheme is expected to have a significant potential in future sub-0.1 μm technology.

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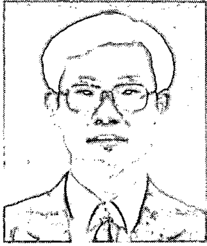

Jong-Ho Lee was born in Kyungnam, Korea, in 1966. He received the B.S. degree in electronic engineering from Kyungpook National University, Taegu, Korea, in 1987, and the M.S. and ph.D. degrees in electronic engineering from Seoul National University, Seoul, in 1989 and 1993, respectively. In 1993, he was a research engineer with ISRC (Inter-University Semiconductor Research Center) until February 1994, performing BiCMOS fabrication and characterization. In 1994, he joined Wonkwang University, Iksan, Chonpuk, where he is currently an assistant professor. He is also with ETRI (Electronics and Telecommunication Research Institute) quantum device laboratory as an invited member of engineering staff. His research interests include SOI for mixed signal processing, low power SOI circuits, deep submicrometer MOSFET's structure, integrated inductors for RF application, deep submicrometer isolation technology, transient simulation of low power devices.