A 3V-30MHz Analog CMOS Current-Mode Digitally Bandwidth Programmable Integrator

Kwang-Sub Yoon and Jai-Sop Hyun

Abstract

A design methodology of the analog current-mode bandwidth programmable integrator for a low voltage(3V) and low power application is developed and the integrator designed by this method is successfully fabricated by the 0.8㎛ CMOS n-well single poly / double metal standard digital process. The integrator ocuppies the active chip area of 0.3 ㎟. The experimental result illustrates a low power dissipation (1.0 mW~3.55 mW), 65dB of the dynamic range, and digitally bandwidth programmability(10MHz~30MHz) with an external digital 4 bit.

Ⅰ. Introduction

Bandwidth programmability of the analog integrator can be achieved by programming either a integration capacitor or transconductance of the driver. The design technique that employes a capacitance array and programmable switches[1] is capable of achieving a high resolution of the bandwidth programmability due to the precise capacitance mismatch less than 0.1% provided by a standard IC process without any extra process step. However, this technique requires a large silicon area to implement the capacitor array and a digital logic circuitry to control the switch connectivity. The bandwidth range is restricted to a few megahertz due to the inherent circuit structure of driving a large capacitance. Therefore this design methodology is not suitable for an application of processing an image signal.

Transconductance programmability can be achieved by programming a magnitude of the current in the integrator. The conventional transconductance programming methodology[2, 3] is based on the voltage-mode technique which requires a large power dissipation and a complex circuit with many internal nodes that prohibits the circuit from being operated at a high frequency. In order to overcome the drawbacks of the voltage-mode programming technique with either transconductance or capacitance, a simple but robust current-mode transconductance programming technique to program the bandwidth of the integrator is proposed in this paper.

In Section Ⅱ, the design technique of the current-mode bandwidth programmable integrator with a current bootstrapping circuit, a dynamic bias circuit, and a current-mode cascode integrator is described to program the bandwidth. The small signal analysis on the current-mode bandwidth programmable integrator is performed in Section Ⅲ. The experimental results are illustrated in Section Ⅳ. In Section Ⅴ, the conclusions are drawn.

Ⅱ. Design of the Current-Mode Digitally Bandwidth Programmable Integrator

This paper proposes an analog CMOS current-mode digitally bandwidth programmable integrator capable of operating at a high frequency. The bandwidth programmable integrator shown in Fig. 1 consists of a current-mode cascode integrator[4], a current boostrapping circuit with programmable switches, and a dynamic bias circuit. The current-mode cascode integrator[4] with a low input impedance and a high output impedance suitable for a power supply of 3V and a low power dissipation is employed to obtain a high dc current gain with a minimum phase distortion. The integrator has the differential current input terminals, Iin+ and Iin-, and the differential current output terminals, Iout+ and Iout-. The MOS transistors, M1 and M2, and the integration capacitor, C are the devices to determine the bandwidth(g_m/C) of the integrator. The integration capacitor, C is designed to be 0.2pF and laid out by a MOS capacitor. This proposed technique has an advantage over the conventional technique[4]. The proposed integrator employes the programmable current bootstrapping circuit such that the bandwidth can be digitally controlled. On the other hand, the bandwidth of the conventional one is analog controlled by knobing the reference current mirror. Therefore the conventional integrator is unable to control the bandwidth as coarse as the proposed one.

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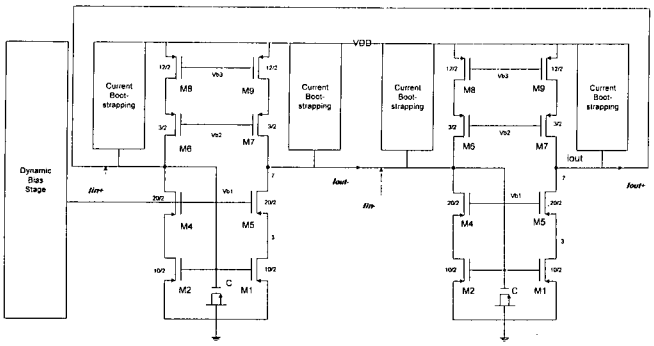

Fig. 1. Circuit diagram of the analog CMOS bandwidth programmable current-mode integrator.

The current boostrapping circuit, as shown in Fig. 2, to provide a programmable current is capable of controlling a magnitude of the current in the cascode current mirror with 4 bit switches.

The number of bit-switches can be extended to the n bit to improve the resolution of the bandwidth programmability of the integrator with a sacrifice of a frequency response, as described in section Ⅲ. This current bootstrapping circuit is connected to the node #7 of the integrator to minimize the interference of the frequency response and the output impedance between the bootstrapping circuit and the integrator. The programmable switches (MS1, MS2, MS3, MS4) are implemented by p-channel MOS transistors with multiple device aspect ratios of 1x(3u / 2u), 2x (6u / 2u), 4x(12u / 2u), and 8x(24u / 2u). These four switches are serially connected to the four programmable current mirror p-channel MOS transistors(MC1, MC2, MC3, MC4) with device aspect ratio of 1x(12u / 2u), 2x(24u / 2u), 4x(48u / 2u), and 8x(96u / 2u). The maximally 16 times programmable current can be feeded to the driver MOS transistors, M1 and M2 such that the transconductance(gm) of M1 and M2 can be programmed from 1x to 4x, namely, the bandwidth can be programmed from 1x to 4x. The total current in M1 can be expressed by (1):

$$I_{M1} = I_{M6} + \sum_{k=1}^{n} 2^{(K-1)} I_u \qquad (1)$$

where n is equal to 4 and I_u is the unit current of $70\,\mu$A flowing through the MC1(12u / 2u).

As the programming current is flowing into the cascode current mirrors consisting of M1, M2, M3, and M4, all these MOS transistors should be always operating in a saturation region at any current level. In order to make these transistors guarantee to operate in a saturation region, the bias voltage, V_{BI} applied to the gate of M3 and M4 should be changed properly. The dynamic bias circuit, as shown in Fig. 3, is designed to properly bias V_{BI}. The structure of the dynamic bias circuit is basically identical to the current bootstrapping circuit except MB2 and MB4. The device aspect ratio of MB2 and MB4 is K times of that of M1 and M3. In order to optimize the value of K, the sensitivity analysis of V_{BI} over V_{DSATI} as a function of K

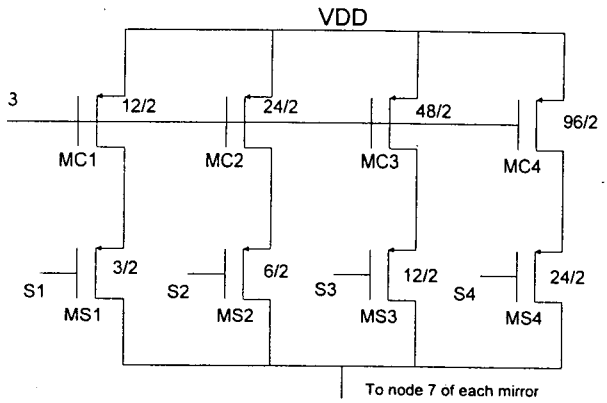

Fig. 2. Circuit shematic of the current bootrapping circuit.

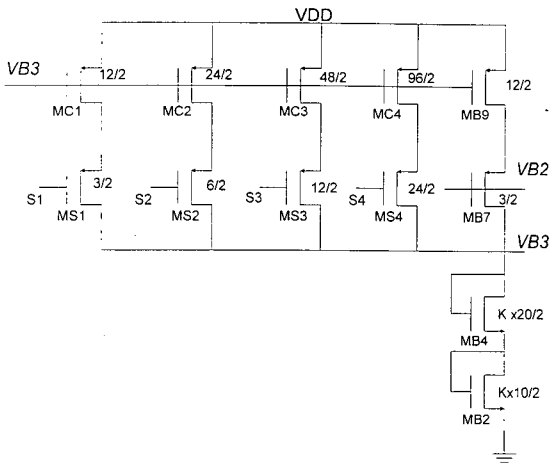

Fig. 3. The Dynamic bias circuit diagram.

is performed. V_{BI} can be described as a function of V_{DSATI} by (2):

$$V_{B1} = V_{DS1} + V_{THO} + \gamma(\sqrt{\varphi_F + V_{DS1}} - \sqrt{\varphi_F}) + V_{DSAT3} \qquad (2)$$

where V_{THO} and φ_F is a threshold voltage and a bulk potential, respectively. $V_{BI,MIN}$ and $V_{BI,MAX}$ can be derived as (3) and (4) to guarantee MOS transistors, M3 and M4 to operate in a saturation region.

$$V_{B1,MIN} \geq V_{DSAT1}(1 + \frac{1}{\sqrt{N}}) + V_{THO} + \gamma(\sqrt{\varphi_F + V_{DS1}} - \sqrt{\varphi_F}) \qquad (3)$$

$$V_{B1,MAX} \leq V_{DSAT1} + 2V_{THO} + \gamma(\sqrt{\varphi_F + V_{DSAT1}(1 - \frac{1}{\sqrt{N}}) + V_{THO}} - \sqrt{\varphi_F}) \qquad (4)$$

where N(= S3 / S1) is the ratio of the device aspect ratio of M3 to that of M1 and Si is the i^{th} device aspect ratio(W/L). The detailed derivation of the equations (3) and (4) are described in the appendix. In order to determine the optimal K, V_{BI} is calculated as a function of V_{DSATI}, K, and N. For $N \neq 2$, V_{BI} deviates the range between $V_{BI,MIN}$ and $V_{BI,MAX}$, regardless of any value of K.

The voltage tracking operation of the dynamic bias circuit

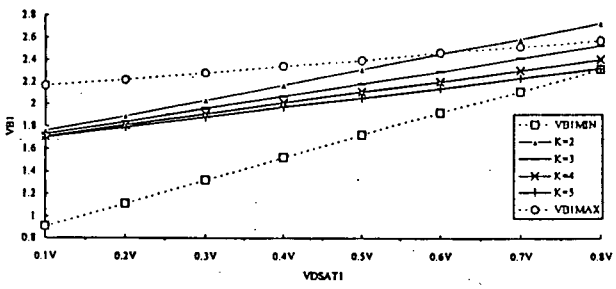

Fig. 4. Voltage tracking operation of the dynamic bias circuit.

from the sensitivity analysis is shown in Fig. 4 to illustrate that V_{BI} with the range of K from 3 to 5 is bounded between $V_{BI,MIN}$ and $V_{BI,MAX}$. The K = 3.3 is found to be optimum so that V_{BI} centers between $V_{BI,MIN}$ and $V_{BI,MAX}$.

III. Small Signal Analysis

In order to analyze the small signal characteristic of the designed current-mode integrator, a half of the small signal equivalent circuit, as presented in Fig. 5, is only considered because of the circuit symmetry. All the parasitics except R_S, R_D, and C_{GB} are included in the derivation of the current gain transfer function, as obtained in (5).

$$\frac{I_{out}}{I_i} \approx \frac{g_{m2} - sC_7 - s^2\frac{2C_2C_7}{g_{m1}}}{2g_{out} + s(C+C_7) + s^2\frac{C_3(C+C_7)}{g_{m1}}} = \frac{g_{m2}}{2g_{out}} \frac{(\frac{s}{Z_1}-1)(\frac{s}{Z_2}-1)}{(\frac{s}{P_1}-1)(\frac{s}{P_2}-1)} \quad (5)$$

The output conductance(g_{out}), the first pole(P_1), the second pole (P_2), the first zero(Z_1), and the second zero(Z_2) of the integrator are written by (6), (7), (8), (9), and (10), respectively.

$$g_{out} = \frac{g_{ds7}g_{ds8}}{g_{m7}} + \frac{g_{ds1}g_{ds4}}{g_{m4}} \quad (6)$$

$$Z_1 = \frac{-C_7 - \sqrt{C_7^2 - 4\frac{g_{m2}}{g_{m1}}C_3C_7}}{2C_3C_7} g_{m1} \quad (7)$$

$$Z_2 = \frac{-C_7 + \sqrt{C_7^2 - 4\frac{g_{m2}}{g_{m1}}C_3C_7}}{2C_3C_7} g_{m1} \quad (8)$$

$$P_1 \approx \frac{2g_{out}}{C} \quad (9)$$

$$P_2 \approx \frac{2g_{m1}}{C_3} \quad (10)$$

The gain-bandwidth product, ω_o is calculated by the multiplication of the dominant pole(P_1) by the dc current gain ($A=g_{m2}/2g_{out}$), as expressed by (11).

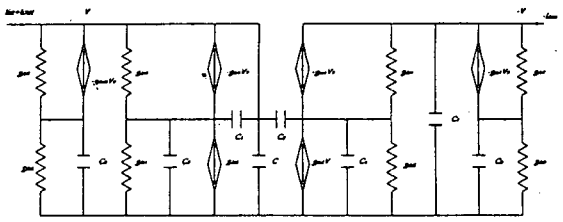

Fig. 5. The small signal equivalent circuit of the current-mode integrator.

$$\omega_o \approx P_1 A = \frac{2g_{out}}{C}\frac{g_{m2}}{2g_{out}} = \frac{g_{m2}}{C} \quad (11)$$

The typical values of Z_1, P_2, and Z_2 are approximately 300MHz, 400MHz, and 500MHz, respectively. The programmable gain-bandwidth product is achieved by programming the transconductance, g_{m2} through the drain current of the MOS transistor, M2. A resolution of the bandwidth programmability of the integrator can be enhanced by increasing the number of the controlling bit. However, it results in shifting the location of Z_1, P_2, and Z_2 to the lower frequency and consequently, degrades the overall frequency response of the integrator.

IV. Experimental Results

The designed analog CMOS current-mode bandwidth programmable integrator is fabricated by the 0.8㎛ CMOS n-well single poly/double metal standard digital process and the chip photograph is shown in Fig 6. The chip size of the integrator occupies 0.3㎟. The measured power consumption and bandwidth variation as a function of the digital 4 bit are illustrated in Fig. 7 and Fig. 8. The simulated power dissipation slope(0.243mW /bit) differs from the measured power dissipation slope(0.207mW /bit). The slope difference between the simulated and measured power dissipation is mainly due to the channel length modulation effect on the MOS transistors, M1 and M2 and a capacitive loading effect at the output node. The fabricated integrator dissipates up to the power of 3.55mW/pole at the 1111 of the switch state. The exprimental bandwidth programmability of the integrator shown in Fig. 8 ranges from 10MHz to 30MHz, which deviates from the simulated behavior of the integrator (10MHz~34.6MHz). It results in the maximum error of 13.4% on the bandwidth. Fig. 9 illustrates the measured transient step responses of the integrator with the bit status of (0000) and (0010). The top, middle, and bottom waveforms show the input signal waveform, the output signal with the bit status of (0000), and the output signal with the bit status of (0010), respectively. The rising slew rates of (0000) and (0010) are measured to be 12mV/㎲ and 28mV/㎲, respectively. Table 1 shows the summary of the experimental results on the integrator.

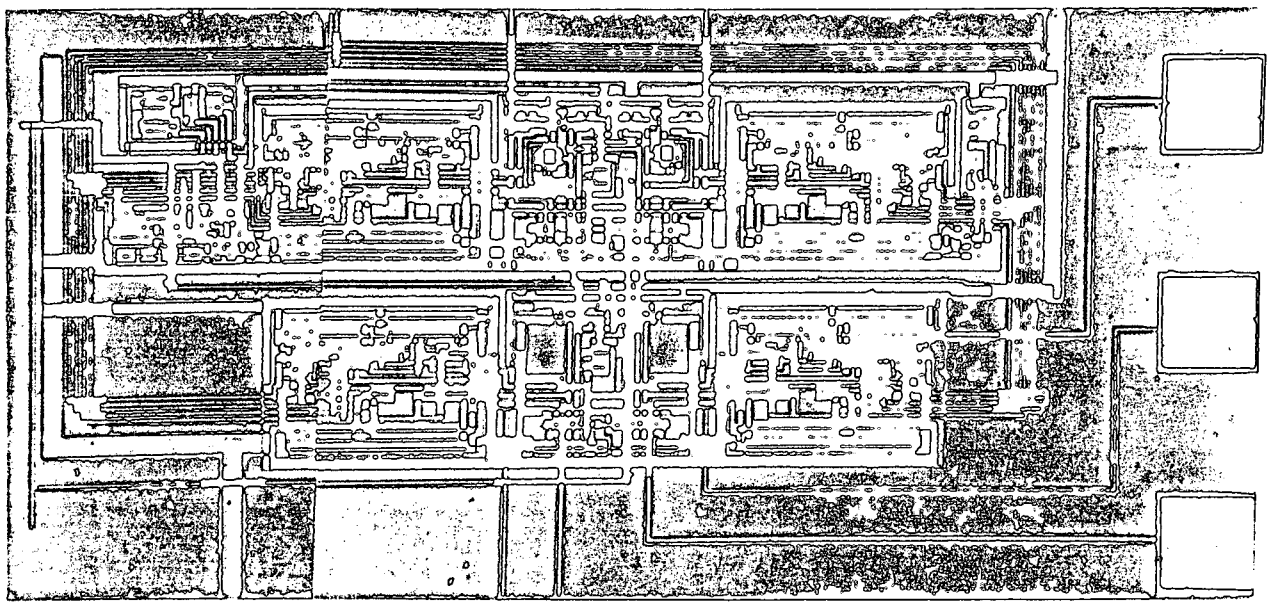

Fig. 6. The fabricated chip photograph of the bandwidth programmable integrator.

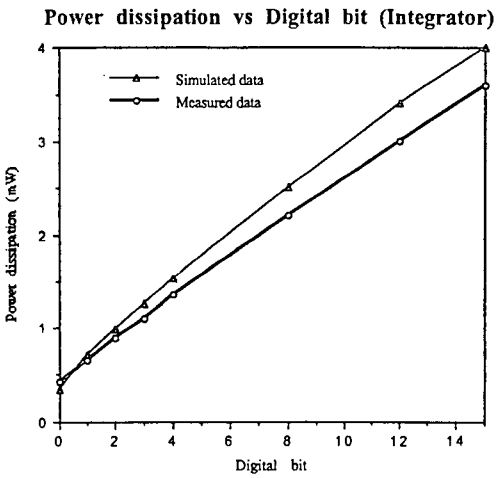

Fig. 7. Plot of the measured power dissipation of the integrator as a function of the external digital bit.

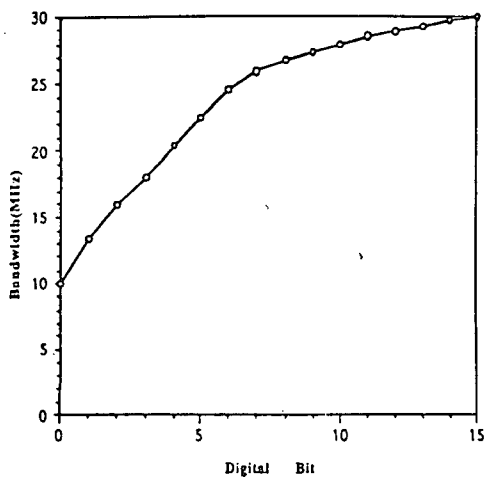

Fig. 8. Plot of the measured bandwidth programmability of the integrator as a function of the external digital bit.

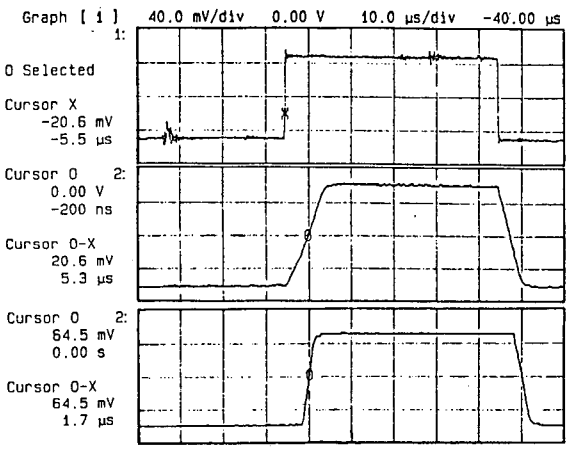

Fig. 9. The measured transient step response of the current-mode bandwidth programmable integrator with the bit status of (0000) and (0010).

Table 1. A summary of the measured results on the bandwidth programmable integrator.

Measured parameters	Measured value
Programmable bandwidth	10MHz - 30MHz
Power dissipation	3.55mW/pole
Dynamic range	65dB
Power Supply	3V
Active chip area	0.3mm^2
Technology	0.8 μm CMOS n-well single poly/double metal

V. Conclusions

In conclusion, a design methodology of the current-mode bandwidth programmable integrator for a low voltage(3V) and low power application(3.55mW/pole) is developed and the integrator is successfully fabricated by the 0.8㎛ CMOS n-well single poly/double metal standard digital process and measured to obtain the low power dissipation(3.55mW) and bandwidth programmability (10MHz~30MHz) with an external digital 4 bit. This design methodology can be further generalized to be able to program the bandwidth with a fine resolution by utilizing an external n-bit digital switches.

Acknowledgment

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Appendix

Derivation of the equation (3)

In order to derive $V_{B1,MIN}$, the condition, $V_{DS1} \geq V_{DSAT1}$ should be met. It results in

$$V_{B1,MIN} \geq V_{DSAT1} + V_{THO} + \gamma(\sqrt{\varphi_F + V_{DS1}} - \sqrt{\varphi_F}) + V_{DSAT3} \quad \textbf{(A.1)}$$

or

$$V_{B1,MIN} \geq V_{DSAT1}(1 + \frac{V_{DSAT3}}{V_{DSAT1}}) + V_{THO} + \gamma(\sqrt{\varphi_F + V_{DS1}} - \sqrt{\varphi_F}) \quad \textbf{(A.2)}$$

Since $V_{DSAT,i} = \sqrt{\frac{I_D}{0.5K' S_i}}$ where K' and Si are a device transconductance parameter and device aspect ratio(W/L), respectively, the equation (A.2) becomes

$$V_{B1,MIN} \geq V_{DSAT1}(1 + \frac{1}{\sqrt{S_3/S_1}}) + V_{THO} + \gamma(\sqrt{\varphi_F + V_{DS1}} - \sqrt{\varphi_F}) \quad \textbf{(A.3)}$$

where it is equivalent to the equation (3).

Derivation of the equation (4)

In order to derive $V_{B1,MAX}$, the condition, $V_{GS1} \geq V_{DS1} + V_{DSAT3}$ should be satisfied. It can be rewritten by $V_{DSAT1} + V_{THO} - V_{DSAT3} \geq V_{DS1}$. If this equation is plugged into (3), it results in

$$V_{B1,MAX} \leq V_{DSAT1} + 2V_{THO} + \gamma(\sqrt{\varphi_F + V_{DSAT1} + V_{THO} - V_{DSAT3}} - \sqrt{\varphi_F}) \quad \textbf{(A.4)}$$

It can be rewritten as

$$V_{B1,MAX} \leq V_{DSAT1} + 2V_{THO} + \gamma(\sqrt{\varphi_F + V_{DSAT1}(1 - \frac{1}{\sqrt{N}}) + V_{THO}} - \sqrt{\varphi_F})$$

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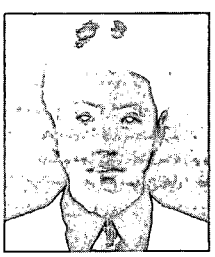

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