# Design of Single-Stage AC/DC Converter with High Efficiency and High Power Factor for Low Power Level Applications

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## Abstract

Design of single stage AC/DC converter with high power factor for low power level applications is proposed. The proposed converter gives the good power factor correction, low line current harmonic distortions, and tight output voltage regulations. This converter also has a high efficiency by employing an active clamp method and synchronous rectifiers. To verify the performances of the proposed converter, a 90W-converter has been designed. The modelling of this proposed converter is performed using an averaging technique and based on this model, a detailed analysis is carried out. This prototype meets the IEC555-2 requirements satisfactorily with nearly unity power factor and high efficiency.

## I. Introduction

IEC555-2 and several national standards requires that the harmonics of the line current of the power distribution system stay below certain level. To meet above requirements, an active current wave shaping technique has been developed[1]. This technique is accomplished by the addition of a dedicated AC/DC front-end converter which controls its switching devices in such a manner that the input current follows a sinusoidal reference. In contrast to the input, additional DC/DC converter must be needed to obtain a desrired DC output. Such a power system has two independent control loops to regulate the output voltage and make the input current follow a sinusoidal reference, which are bulky and inefficient[2]. This converter structure is not desirable in medium or low power level converters.

Recently, many efforts have been made to integrate these two power stages into a more compact and efficient architecture. For a single stage PFC converter, the flyback topology is available. This simple topology has advantages that the desired output voltage can be obtained with the isolated DC output and converter has an advantage of not requiring any inductor. However, this flyback topology has the high EMI noise of the line current which requires the large input filters and produces the large low frequency output voltage ripple[3]. To overcome these drawbacks, several topologies are proposed. Among them, the most eminent topologies are SEPIC[4] and BIFRED[5] in a discontinuous conduction mode (DCM) and are possible to construct a single stage converter containing a single switch. Unfortunately SEPIC and BIFRED have a large low frequency output voltage ripple and cannot obtain a high efficiency due to switching loss and rectification loss.

In this paper, a schematic design prodcedure of AC/DC PFC converter for low power level applications based on the forward topology is introduced. The modelling employing the averaging method[6] and detailed analysis are performed to derive design equations and show that the output voltage ripple of the proposed converter is much smaller than that of BIFRED. This converter is capable of drawing a high quality AC line current waveform and a pure DC output voltage without a significant voltage ripple at twice the line frequency. Futhermore it employs the active clamp method[7] to improve the efficiency by accomplishing the ZVS of switches and transformer reset performance. In converters with low power supply voltages, it is quite difficult to achieve a high efficiency due to rectifier diodes of the output stage. Rectification loss in a conventional 100W DC/DC converter is about 50% of total loss. Therefore, the best way to keep the efficiency at a desirable level is to substitute rectifier diodes by synchronous rectifiers[8]. In this way, the almost constant voltage drop is substituted by a resistance type($R_{DSON}$) voltage drop, which reduces the loss of the output rectifier. So synchronous rectifiers are adopted as rectification method.

To validate the performance, a prototype is designed according to design guidelines and its experimental results are presented.

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## II. Operation Principles

Fig. 1 shows the circuit diagram of the AC/DC converter with high power factor and high efficiency. This converter can be understood as a cascade connection of a boost converter followed by a forward converter. As can be seen in this figure, the two converters share the same switch. An active clamp method and synchronous rectifiers are shown in a dotted line to a improve a efficiency and transformer reset performance. As shown in Fig. 2, each switching period is subdivided into six modes, each of them correspondent to different equivalent circuits (see Fig. 3). Before describing the operation, the following assumptions are made:

- *The DC link capacitor, $C_{link}$ is so large that $V_{link}$ is assumed to be a constant DC voltage.*
- *The switches, $Q_1$ and $Q_2$, are ideal except for output capacitances and internal diodes.*
- *The parasitic capacitances of the transformer are ignored.*
- *Magnetizing current $i_{tr}$ and input inductor current $i_{Lin}$ are assumed to be constant during dead-time.*

***Mode 1 ($T_0 \leq t < T_1$)***

This is an ON_state interval of $Q_1$. At $T_o$, the main switch $Q_1$ is turned on and the current flowing through the inductor $L_{in}$ increases with the slope of $|V_{in}|/L_{in}$, which is expressed as

$$i_{Lin} = \frac{|V_{in}|}{L_{in}} t \tag{1}$$

Since boost stage and forward stage share the same switch $Q_1$, the current stress of $Q_1$ is the sum of the output current reflected to the primary $I_{LO}/n$, input inductor current $i_{Lin}$ and magnetizing current $i_{tr}$ given in eq. (2)

$$i_{tr} = \frac{V_{link}}{L_p + L_{lkg}} t - i_{tr}(0) \tag{2}$$

where $-i_{tr}(0)$ means the initial condition of $i_{tr}$.
Therefore, $i_{Q1}$ can be obtained as follows:

$$i_{Q1} = \frac{|V_{in}|}{L_{in}} t + \frac{V_{link}}{L_p + L_{lkg}} t - i_{tr}(0) + \frac{I_{LO}}{Dn} \tag{3}$$

Since $i_{tr}$ increases to $i_{tr}(0)$ in steady state, $i_{tr}(0)$ becomes

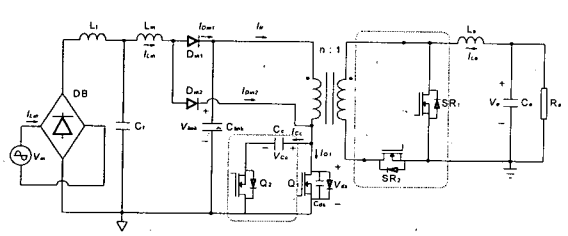

**Fig. 1.** Schematic of the proposed converter.

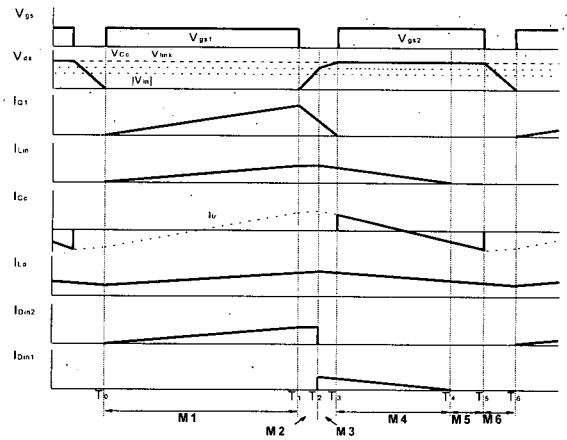


**Fig. 2.** Key waveforms for mode analysis.

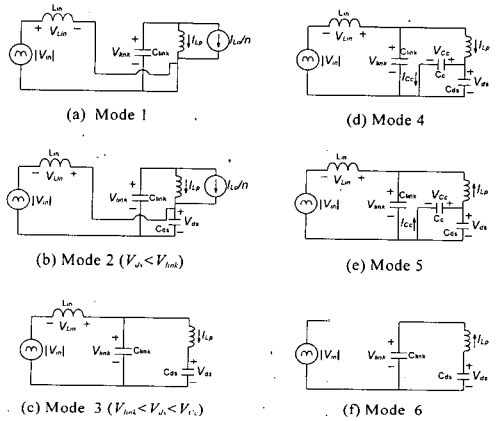


**Fig. 3.** Equivalent circuits of the proposed converter.

$$i_{tr}(0) = \frac{V_{link} D T_s}{2(L_p + L_{lkg})} \tag{4}$$

from eq. (2).

***Mode 2 ($T_1 \leq t < T_2$)***

Mode 2 begins when the MOSFET $Q_1$ is turned off at $T_1$. Since the dotted side of the transformer is positive with respect to the undotted end and diode $D_{in2}$ is still forward biased, the output capacitance of $Q_1$, $C_{ds}$ is charged by $i_{tr}(T_1)$, $i_{Lin}(T_1)$ and $I_{LO}/n$. Thus $v_{ds}$ rises steeply as shown in eq. (5)

$$v_{ds} = \frac{i_{Lin}(T_1) + i_{tr}(T_1) + I_{LO}/Dn}{C_{ds}} t \tag{5}$$

Mode 2 stops when $v_{ds}$ reaches $V_{link}$.

***Mode 3 ($T_2 \leq t < T_3$)***

When $v_{ds}$ is increased up to $V_{link}$, the diode $D_{in1}$ is forward biased and the diode $D_{in2}$ reverse biased, respectively. The stored

energy of the inductor $L_{in}$ is transferred to the link capacitor $C_{link}$. Since the dotted end of the primary side of the transformer is negative with respect to the undotted end, the output stage is separated during this mode. The voltage $v_{ds}$ is more gradually increased than that of the mode 2 because only the small magnetizing current remains to charge the output capacitance of $Q_1$. $i_{Lin}$ and $v_{ds}$ are represented as

$$i_{Lin} = i_{Lin}(T_1) + \frac{|V_{in}| - V_{link}}{L_{in}} t \tag{6}$$

and

$$v_{ds} = \frac{i_{tr}(T_1)}{C_{ds}} t \tag{7}$$

respectively during this mode.
When $v_{ds}$ is increased to $V_{Cc}$, the magnetizing current flows to the clamp capacitor $C_c$ and mode 3 stops.

***Mode 4 ($T_3 \leq t < T_4$)***

This mode is an interval that the clamp capacitor $C_c$ absorbs the magnetizing energy of the transformer. The drain to source voltage of $Q_1$, $v_{ds}$, reaches the clamp capacitor voltage $V_{Cc}$ and the anti-parallel diode of the auxiliary switch $Q_2$ starts to conduct, which results in a reduction of the voltage stress of $Q_1$. The magnetizing current flows in a resonant manner by the clamp capacitor $C_c$ and the sum of the magnetizing inductance and leakage inductance of the transformer $L_p+L_{lkg}$. This current is approximately

$$i_{Cc} = i_{tr}(T_1) + \frac{V_{link} - V_{Cc}}{L_p + L_{lkg}} t \tag{8}$$

***Mode 5 ($T_4 \leq t < T_5$)***

After mode 4, the discontinuous conduction mode(DCM) occurs. When $i_{Lin}$ reduces to zero, $D_{in1}$ is reverse biased. The magnetizing current flows from $C_c$ to the transformer through the auxiliary switch $Q_2$ which has been in ON_state from mode 4. In order to achieve the ZVS of $Q_2$, the device must be turned on before the clamp capacitor current $i_{Cc}$ reverses its direction to the transformer. This mode stops when the auxiliary switch $Q_2$ is turned off and $i_{Cc}$ decreases to $i_{tr}(T_5) = -i_{tr}(0)$.

***Mode 6 ($T_5 \leq t < T_6$)***

In this mode, the energy dissipation of $C_c$ stops and $C_{ds}$ starts discharging by the stored energy in $L_p+L_{lkg}$. $C_{ds}$ is so small that it leads to an approximately linear discharging characteristic and the discharging time is very brief. $v_{ds}$ can be expressed as

$$v_{ds} = V_{Cc} - \frac{i_{tr}(0)}{C_{ds}} t \tag{9}$$

When $v_{ds}$ reduces to zero, the ZVS condition of $Q_1$ is able to be achieved.

It is noted that during modes 3, 4, 5, and 6, the output stage is not influenced by the rectified input voltage because the MOSFET synchronous rectifier $SR_1$ is switched on and the output current freewheels through $SR_1$. Hence, this converter has an independence of the output voltage regulation and power factor correction, which is impossible in BIFRED. As a result, the output voltage ripple at twice the line frequency which appears in BIFRED can be eliminated.

## Ⅲ. Modelling and Output Ripple Analysis

### *1. Modelling*

Averaging of one switching cycle provides a large signal model of the proposed converter[5]. The resulting large signal modelling equations can be obtained from Fig. 4 as follows:

$$i_{Lin} = \frac{1}{R_e}\left[|v_{in}| + \frac{v_{in}^2}{v_{link} - |v_{in}|}\right] \tag{10}$$

$$\frac{dv_{link}}{dt} = \frac{1}{R_e C_{link}}\left[\frac{v_{in}^2}{v_{link} - |v_{in}|}\right] - \frac{D}{nC_{link}} i_{LO} \tag{11}$$

$$\frac{di_{LO}}{dt} = \frac{v_{link}}{nL_o} D - \frac{v_o}{L_o} \tag{12}$$

$$\frac{dv_o}{dt} = \frac{i_{LO}}{C_o} - \frac{v_o}{R_o C_o} \tag{13}$$

where $R_e \equiv \frac{2L_{in}}{D^2 T_s}$ and $D$ is a duty ratio.

These modelling equations are similar to those of BIFRED expressed in eqns. 2a-d[5]. The major difference is that the output

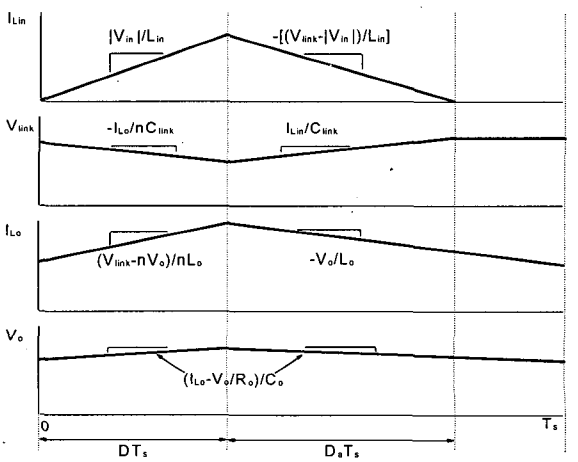


**Fig. 4.** Switching waveforms of various currents and voltages with their slopes.

voltage of BIFRED is related to the current which flows in $L_{in}$ when the switch is turned off. After multiplying by $n$, this current is transferred to the output stage through the transformer and causes the output voltage ripple at twice the line frequency to occur as the first term of eqn. 2d in Madigan's paper. However, the output voltage regulation of the proposed converter is not affected by the power factor correction performed in the boost stage because eq. (13) does not have a term like that.

*2. Output Voltage Ripple*

As shown in equations (14)-(16), the output voltage ripple of the proposed converter is obtained by filtering the link capacitor voltage with the output filter $L_o$ and $C_o$. However, in BIFRED, the output voltage ripple is directly influenced by the rectified input voltage as shown in eq. (17).

$$\Delta v_{o1} = \frac{D}{n}\frac{\beta R_{eq}}{1+(2\omega C_{link})^2}\frac{R_o}{(R_o-4\omega^2L_oC_oR_o)^2+(2\omega L_o)^2}[\{(R_o-4\omega^2L_oC_oR_o)-4\omega^2R_{eq}L_oC_{link}\}\cos 2\omega t+\{2\omega L_o+2\omega R_{eq}C_{link}(R_o-4\omega^2L_oC_oR_o)\}\sin 2\omega t] \quad (14)$$

$$\Delta v_{o2} = \frac{D}{n}\frac{\gamma R_{eq}}{1+(4\omega C_{link})^2}\frac{R_o}{(R_o-16\omega^2L_oC_oR_o)^2+(4\omega L_o)^2}[\{(R_o-16\omega^2L_oC_oR_o)-16\omega^2R_{eq}L_oC_{link}\}\cos 4\omega t+\{4\omega L_o+4\omega R_{eq}C_{link}(R_o-16\omega^2L_oC_oR_o)\}\sin 4\omega t] \quad (15)$$

$$\Delta v_o = \Delta v_{o1} + \Delta v_{o2} \quad (16)$$

where $R_{eq} = \frac{n^2}{D^2}R_o$,

and

$$\Delta v_o^B(t) = \frac{R^B{}_o n^B V^B{}_{inpk}}{R_e}\left[\frac{\beta^B}{1+(2\omega R^B{}_o C^B{}_o)^2}\{\cos 2\omega t+(2\omega R^B{}_o C^B{}_o)\sin 2\omega t\}+\frac{\gamma^B}{1+(4\omega R^B{}_o C^B{}_o)^2}\{\cos 4\omega t+(4\omega R^B{}_o C^B{}_o)\sin 4\omega t\}\right] \quad (17)$$

where 'B' means BIFRED.

The computer simulations of the output voltage with equations (10)-(13) and eqns. 2a-d in Madigan's paper, are depicted in Fig. 5 for a 60Hz input line frequency and Fig. 6 shows the comparison of the peak to peak output voltage ripple between the proposed converter and BIFRED. From these figures the output voltage ripple of the proposed converter is much smaller than that of BIFRED.

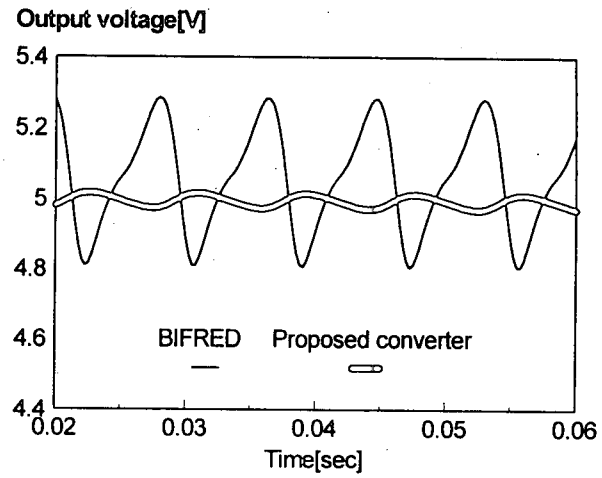


**Fig. 5.** Output voltage ripples of BIFRED and proposed converter.

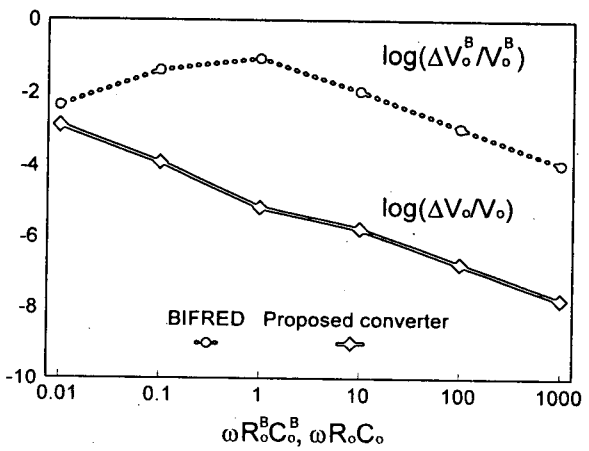


**Fig. 6.** Comparison of the output voltage ripple between the proposed converter and BIFRED under load variation with following parameters: $f_s$=100kHz, $R_e$=353.0Ω, $R_{eq}$=1430Ω, D=0.238, M($M^B$)=0.308, $L_{in}$($L_o^B$)=10μH, $C_o$($C_o^B$)=320μH, $C_{link}$($C_{link}^B$)=320μH.

## Ⅳ. Design Equations

*1. Inductor $L_{in}$ and Transformer Turns Ratio n*

The steady state equations of link voltage $V_{link}$ and output voltage $V_o$ are obtained by averaging the modelling equations (10)-(13) over half of a line cycle. The solutions are

$$V_{link} = \frac{V_{inrms}}{\sqrt{2}}\left(1+\sqrt{1+\frac{0.852n^2R_o}{L_{in}f_s}}\right) \quad (18)$$

and

$$V_o = \frac{DV_{link}}{n} \quad (19)$$

To maintain a sinusoidal input current, the converter must operate

in DCM over entire cycle. This condition requires that $i_{Lin}$ reaches zero before the end of switching period $T_s$. Thus DCM condition is

$$D_a \le D \tag{20}$$

where $D_a$ is a time ratio from the time when switch $Q_1$ is turned off to the time when $i_{Lin}$ reaches zero and given as

$$D_a = \frac{\sqrt{2}V_{inrms}}{V_{link}-\sqrt{2}V_{inrms}} D \tag{21}$$

From equations (18)-(19) the link voltage is

$$V_{link} = \frac{\sqrt{2}V_{inrms}L_{in}f_s V_o^2}{L_{in}f_s V_o^2 - 0.426D^2R_oV_{inrms}^2} \tag{22}$$

So, transformer turns ratio $n$ as a function of $L_{in}$ can be yielded as

$$n = \frac{\sqrt{2}V_{inrms}L_{in}f_s V_o^2 D}{L_{in}f_s V_o^3 - 0.426D^2R_oV_oV_{inrms}^2} \tag{23}$$

The maximum input inductance to meet DCM condition can be obtained as in inequality (24) using eq. (22) and DCM condition (20).

$$L_{in} \le \frac{0.426DR_oV_{inrms}^2}{f_sV_o^2} \tag{24}$$

If we choose a $L_{in}$ which satisfies inequality (24) at the worst-case of DCM which occurs with maximum load and minimum peak line voltage, $n$ can be determined using eq. (23).

*2. Switch $Q_1$ and $Q_2$*

The relationship of voltage stress on the switch and link capacitor voltage is given as

$$V_{Q1} = V_{Q2} = \frac{V_{link}}{(1-D)} \tag{25}$$

Therefore voltage stress on switches $Q_1$ and $Q_2$ becomes

$$V_{Q1} = V_{Q2} = \frac{\sqrt{2}V_{inrms}L_{in}f_sV_o^2}{(1-D)(L_{in}f_sV_o^2 - 0.426D^2R_oV_{inrms}^2)} \tag{26}$$

Another factor to select switches is the current stress. Since the clamp switch carries only a small magnetizing current, the choice of a clamp switch $Q_2$ is less critical and the same kind of the main switch can be used for a clamp switch. Therefore selection of switch is focused on $Q_1$. Current flowing in $Q_1$ is given as eq. (3) from the mode analysis. If the dead-time is so small to be negligible, the peak current flowing in $Q_1$ is as follows:

$$I_{Q1} = \frac{\sqrt{2}V_{inrms}D}{L_{in}f_s} + \frac{V_o}{DnR_o} + \frac{V_{link}D}{2(L_p+L_{lkg})f_s} \tag{27}$$

Also, $D$ can be found from eqns. (18) and (19) with predetermined values of $L_{in}$ and $n$. This equation is

$$D = \frac{-\sqrt{2}V_oL_{in}f_s + \sqrt{2V_o^2L_{in}^2f_s^2 + 1.704n^2V_o^2R_oL_{in}f_s}}{0.852nR_oV_{inrms}} \tag{28}$$

From equations (26), (27) and (28) it can be found that maximum voltage stress happens at minimum load and maximum peak line voltage and maximum current stress at maximum load and maximum peak line voltage. Therefore, designer must choose a switch at this worst condition with predetermined values of $L_{in}$ and $n$.

In order to improve the efficiency of the converter, the synchronous rectifiers are added in parallel with the schottky diodes. The on_resistance of MOSFET used for the synchronous rectifiers $R_{DSON}$ must be chosen to satisfy the following limitation:

$$I_{LO}^2R_{DSON} < I_{LO}V_{ON} \tag{29}$$

where $V_{ON}$ is the diode voltage drop and $I_{LO}$ is the average output current.

*3. Clamp Capacitor $C_c$ and Output Inductor $L_o$*

The value of the clamp capacitor is determined by the clamp voltage ripple $\Delta V_{Cc}$ which affects the peak voltage stress of the switches. The clamp capacitor is designed to meet the following condition:

$$C_c \gg \frac{[(1-D)T_s]^2}{\pi^2(L_p+L_{lkg})} \tag{30}$$

And the output inductor can be selected with

$$L_o = \frac{(V_{link}-nV_o)DT_s}{n\Delta I_{LO}} \tag{31}$$

where $\Delta I_o$ is the desired output current ripple.

*4. Dead-time*

To maintain a ZVS condition of main switch, the dead-time of main switch $Q_1$ must be longer than the discharging time of the output capacitance of $Q_1$, $C_{ds}$. From eqnuations (4) and (9) with $v_{ds}$ equaling to zero, the discharging time can be calculated as

$$t_{dischrging} = \frac{2C_{ds}(L_p+L_{lkg})}{D(1-D)T_s} \tag{32}$$

The maximum discharging time of $C_{ds}$ happens at the minimum duty ratio(maximum line voltage and minimum load). Thus dead-time selection guideline is

$$\Delta d \ge \frac{2C_{ds}(L_p+L_{lkg})}{D_{min}(1-D_{min})T_s^2} \tag{33}$$

However, $\Delta d$ may be excessively large relative to duty ratio $D$ at a high switching frequency operation. In this case it lies with a designer to select $\Delta d$ with the consideration of input line voltage and load variations to meet ZVS.

# V. Experimental Results

## 1. Design Example

To prove the validity of design guidelines a 90W-converter has been designed. The design specifications are

*Rms line voltage $V_{inrms}$ : 75-135Vrms*
*Output voltage $V_o$ : 5V*
*Output power $P_o$ : 25-90W*
*Switching frequency $f_s$ : 100kHz*
*Maximum duty ratio $D_{max}$ : 0.5 at $V_{inrms}$=75Vrms and $P_o$=90W.*

Fig. 7 shows $V_{link}$, $n$ and $D_a$ using equations (21), (22) and (23) with $V_{inrms}$=75$V_{rms}$ and $P_o$=90W($R_o$=0.278Ω) as the function of $L_{in}$. The critical value of $L_{in}$ to meet DCM is calculated as 133.2μH from inequality (24). Thus we have selected 130μH for $L_{in}$ in this design. Based on this value, $n$=21 is able to be obtained with $V_{link}$=217.5V

Voltage and current stresses on switch at various input line voltage according to $R_o$ are depicted in Fig. 8 using equations (26), (27) and (28). From this figure, the maximum voltage stress and maximum current stress are 743.9V and 8.72A respectively. In the selection of switches, additional voltage from ringing effect caused by transformer leakage inductance must be considered. A possible choice is *2SK1816* which has $BV_{DSS}$=900V and $I_{D(ON)}$=10A.

Rectification power loss and output current ripple should not pass over 5W and 4A at rated condition($V_{in}$=110$V_{rms}$, $P_o$=90W) respectively. Then 10μH and 12.5mΩ are obtained as the minimum $L_o$ and the maximum $R_{DSON}$. In this design clamp capacitor $C_c$ is chosen to be 3.3μF. This value is large enough to is satisfied with inequality (31).

From inequality (33) the minimum dead-time calculated with measured value of $L_p$+$L_{lkg}$ and output capacitance $C_{ds}$ of *2SK1816* is 0.0182. Table 1 lists the components for experiment.

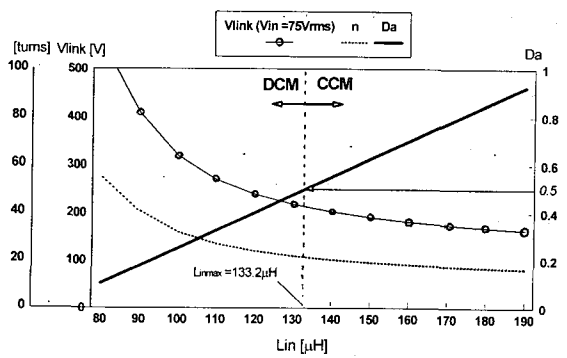


**Fig. 7.** Link voltage $V_{link}$, transformer turns ratio n, Da versus $L_{in}$ at the worst-case of DCM ($V_{in}$=75$V_{rms}$, $P_o$=90W, D=0.5): Maximum $L_{in}$ to meet DCM condition is 133.2μH.

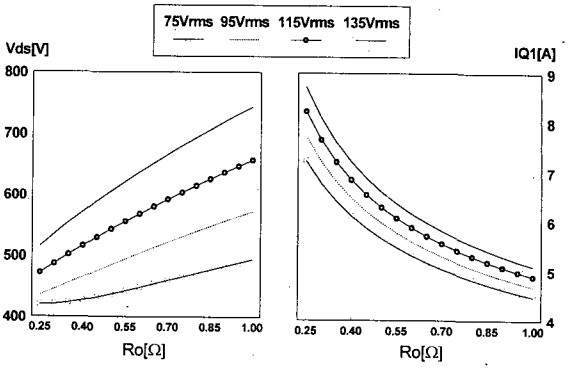


**Fig. 8.** Voltage and current stress on the main switch $Q_1$ under load and input variations.

**Table 1.** Components list.

| | |
|---|---|
| Main switch($Q_1$) | 2SK1816(MOSFET) |
| Auxiliary switch($Q_2$) | 2SK1816(MOSFET) |
| Synchronous Rectifiers(*SR1,SR2*) | SMP60N03-10L($R_{DSON}$=10mΩ) |
| Input inductor($L_{in}$) | 130μH |
| Clamp capacitor($C_c$) | 0.33μF |
| Link capacitor($C_{link}$) | 220μF |
| Output inductor($L_o$) | 10μH |
| Output capacitor($C_o$) | 320μF |
| Diodes($D_{in1}$, $D_{in2}$) | S20L60 |
| Bridge diode(*DB*) | D6SB60L |
| Filter inductor($L_f$) | 70μH |
| Filter capacitor($C_f$) | 0.1μF |
| Transformer turns ratio n:1 | 21:1 |
| Transformer magnetizing inductance($L_p$) | 430μH |
| Transformer leakage inductance($L_{lkg}$) | 8μH |

Fig. 9 shows the measured key waveforms for a 60$V_{DC}$ input voltage and Fig. 10 shows the drain to source voltage of the main switch $Q_1$ superimposed on the current flowing in $Q_1$. It can be seen that all the waveforms are agree well with the theoretical analysis and the ZVS condition of the main switch $Q_1$ is achieved. The experimental waveforms of the input current/voltage, output voltage, boost inductor current as well as the link voltage under the condition of 110$V_{rms}$ input voltage are depicted in Fig. 11. It can be seen in this figure that the envelope of the boost inductor current follows the rectified input voltage waveform and the filtered input current which has a near sinusoidal waveform flows without phase difference to the input voltage. From these waveforms, it is clear that the power factor is assumed to be unity. The output voltage has no low frequency harmonics but contains small voltage spikes which come from the reverse recovery of the rectifiers.

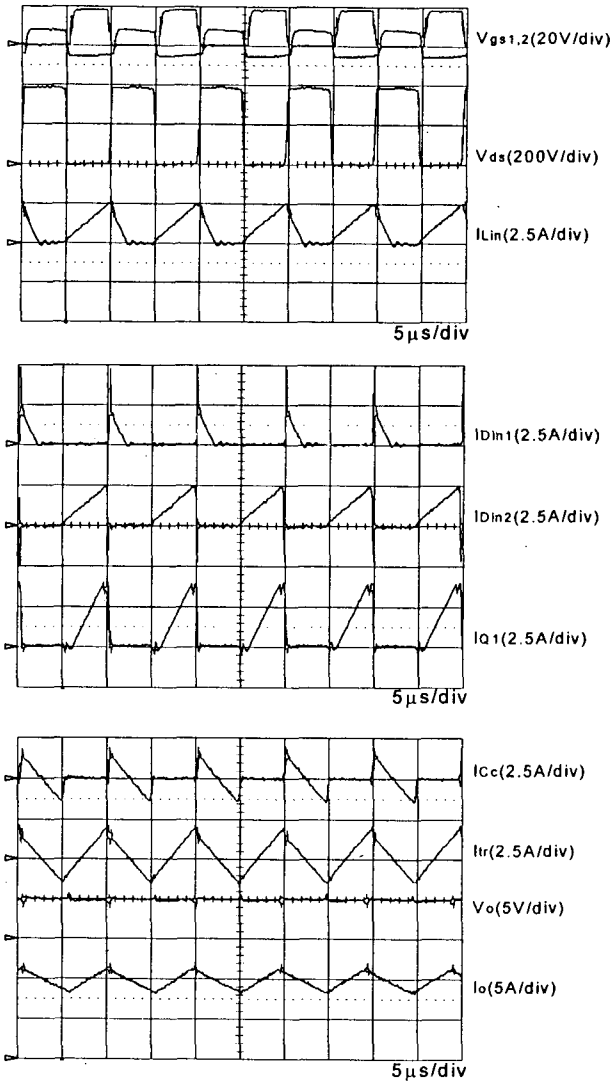


**Fig. 9.** Experimental waveforms for a $60V_{DC}$ input voltage.

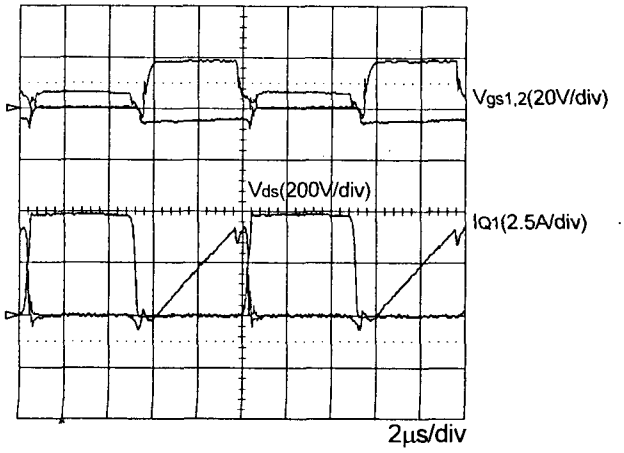


**Fig. 10.** Experimental waveforms of drain to source voltage of main switch Q1 superimposed on the current flowing in Q1 for a 60VDC input voltage: Zero voltage switching is achieved.

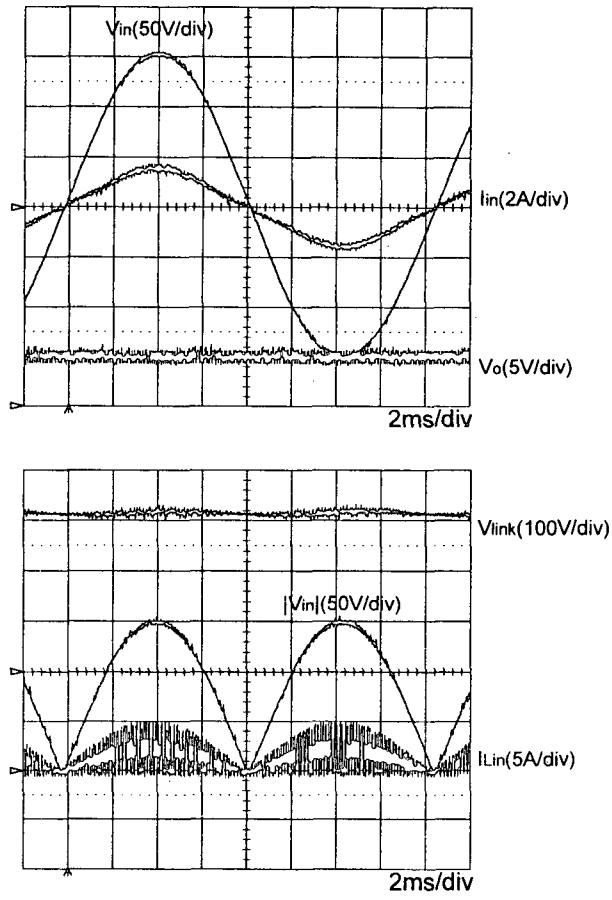


**Fig. 11.** Experimental waveforms of an input/output voltage, input current, input inductor current, and link voltage under $V_{in}$=110$V_{rms}$ and $P_o$=90W.

*2. Power Factor and Harmonic Distortion*

As the input current waveform is not purely sinusoidal, there is harmonic distortion. This distortion can be expressed as a function of the ratio of the peak line voltage($V_{inpk}$) to the link voltage($V_{link}$) as follows [9]:

$$PF=\frac{\sqrt{\frac{2}{\pi}}\int_0^{\pi}\sin\omega t\frac{G\sin\omega t}{1-G\sin\omega t}\,d\omega t}{\sqrt{\int_0^{\pi}\frac{(G\sin\omega t)^2}{(1-G\sin\omega t)^2}\,d\omega t}} \tag{34}$$

where $G\equiv V_{link}/V_{inpk}$.

Figures 12 and 13 show the plots of the calculated power factor using eq. (34) and measured power factor under the load and input variations, respectively. This power factor stays relatively high for the wide range of the input voltage and load. Also the measured power factor is above 0.965. Fig. 14 shows the measured harmonics superimposed on specified IEC 555-2 class D limits. As shown in Fig. 14 the proposed converter meets the harmonic regulations. The experimental waveforms of the input current/voltage under the load variations and their FFT results are shown in Fig. 15.

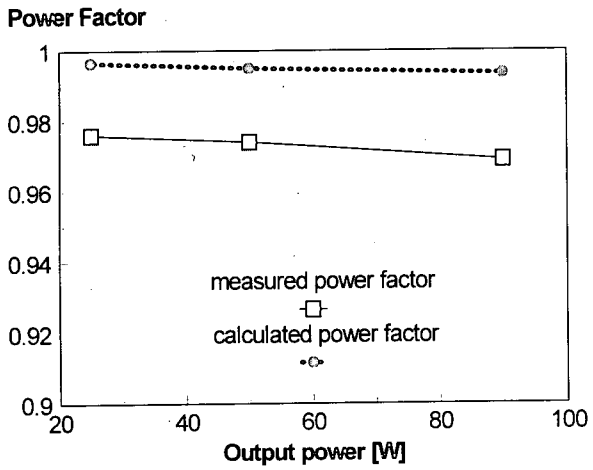


**Fig. 12.** Power factor under load variations.

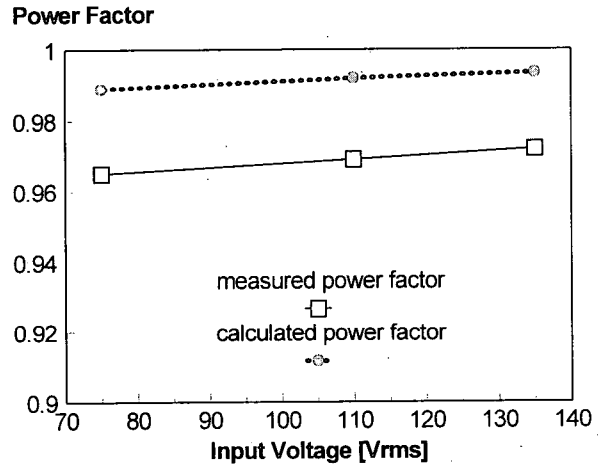


**Fig. 13.** Power factor under input variations at $P_o$=90W.

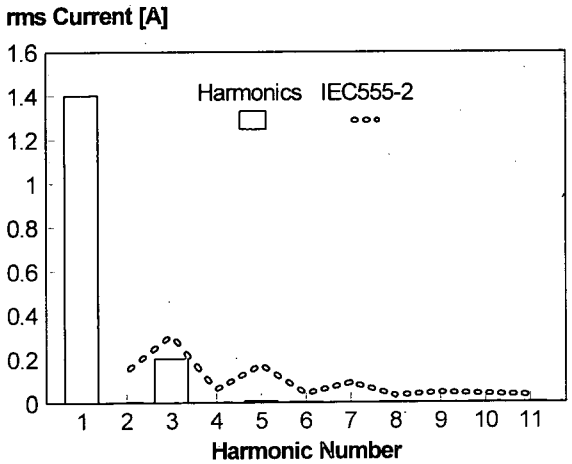


**Fig. 14.** The measured line current garmonics superimposed on IEC 555-2 class-D limits.

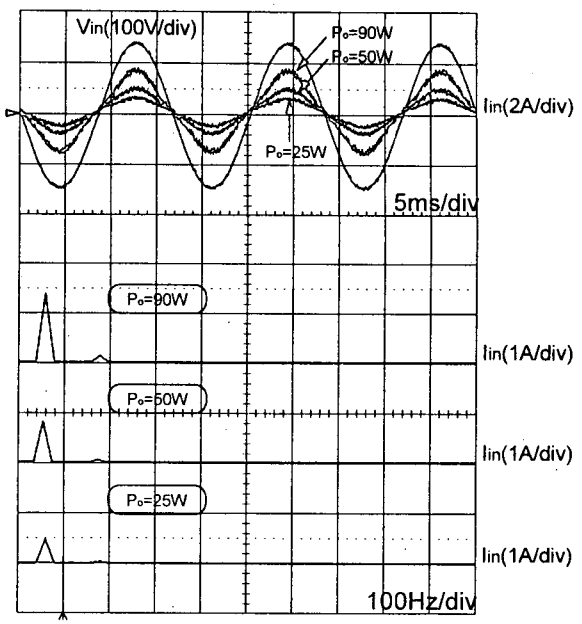


**Fig. 15.** Experimental waveforms of input current/voltage under load variations and their FFT results, at $V_{in}$=110$V_{rms}$.

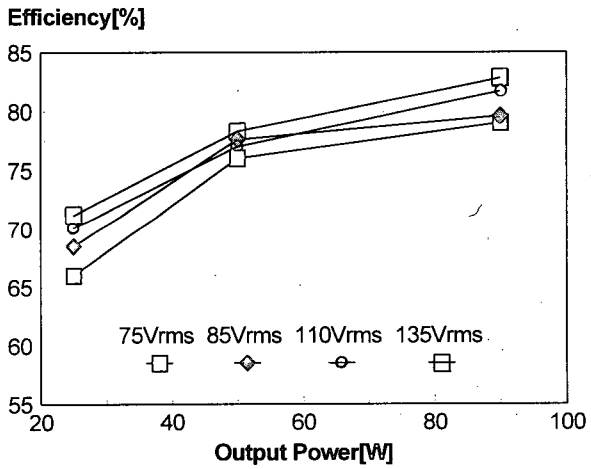


**Fig. 16.** The efficiency of the prototype converter under input voltage and load variations.

*3. Efficiency*

Fig. 16 shows the efficiency of the prototype converter, which is presented as a function of the output power. As can be seen in this figure, the efficiency of the proposed converter can be obtained around 80% in a normal operation. As can be seen in Fig. 17, the loss in the rectifiers is decreased to 9.8% and this loss is reduced considerably by employing MOSFET synchronous rectifiers.

## VI. Conclusions

In this paper, design guidelines of AC/DC converter for power factor correction is proposed. It gives the good power factor, lowharmonic distortion, and high efficiency in a single stage. To

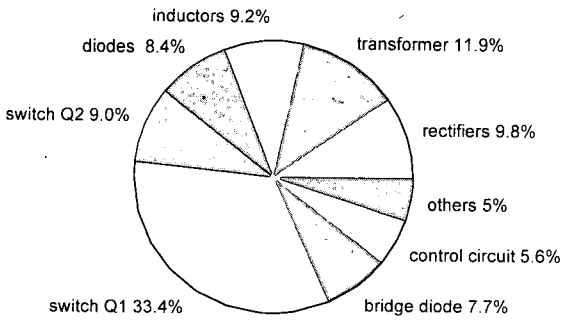


**Fig. 17.** Loss distribution of the proposed converter.

the improve the efficiency and transformer reset performance, the active clamp method and MOSFET synchronous rectifiers are employed. The experimental results show that the prototype of the proposed converter successfully meets the IEC555-2 requirements. The power factor is obtained above 0.965 and the efficiency around 80% in a normal operation. Based on the averaging-modelling method, the modelling and analysis are performed to obtain the output voltage ripple, which shows that the peak to peak magnitude of the output voltage ripple is much smaller than that of BIFRED.

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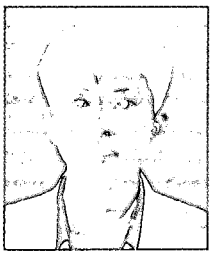

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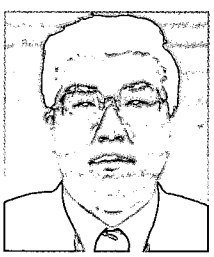

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