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Mobility Determination of Thin Film a-Si:H and poly-Si

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Abstract

Thin film Si has been used in sensors, radiation detectors, and solar cells. The carrier mobility of thin film Si influences the device behavior through its frequency response or time response. Since poly-Si shows the higher mobility value, a-Si:H films on Mo substrate were subjected to various crystallization treatments. Consequently, we need to find an appropriate method in mobility measurement before and after the anneal treatment. This paper investigates the carrier mobility improvement with anneal treatments and summarizes the mobility measurement methods of the a-Si:H and poly-Si film. Various techniques were investigated for the mobility determination such as Hall mobility, HS, TOF, SCLC, TFT, and TCO method. We learned that TFT and TCO method are suitable for the mobility determination of a-Si:H and poly-Si film. The measured mobility was improved by 2~3 orders after high temperature anneal above 700°C and grain boundary passivation using an RF plasma rehydrogenation.

1. Introduction

The amorphous silicon enjoys a broad range of electronic device applications such as sensors, radiation detectors, photovoltaic (PV) devices, thin film transistors (TFTs), display devices, and memory device applications. However, a-Si:H detectors and TFTs show some limitations because of the low carrier mobilities. The low field effect mobility of a-Si:H TFT leads to slow response of liquid crystal displays (LCDs) and to installation of external drive circuits. On the other hand, the field effect mobility for poly-Si TFTs is sufficiently high to permit implementation of on-board drive circuit (1). For a region of low electric field, the carrier velocity is proportional to the mobility. Therefore, a higher mobility material is likely to have a higher frequency response. Seven different techniques were employed to decide the carrier mobilities of thin film Si. The investigated techniques were Hall mobility (2), Haynes and Shockley (HS) method (3), conductivity mobility (4), time of flight (TOF) (5-8), space charge limited conduction mechanism (SCLC) (9-15), TFT (16-18), and transient current observation (TCO) with step volt application (19-21). This paper covers briefly on TOF, SCLC, TFT and other methods. TOF method employs two pulse generators; a master generator triggers laser operation and the slave generator supplies dc pulse to the sample. An applied dc bias forms an electric field across the amorphous sample and the field swept out photo-generated carriers. This photo-generated carrier movement was observed by 5ns digitized oscilloscope. The delay time was figured out where a photo-current drops by 50% in linear scale or slope changing point in log-log scale graph. For SCLC mobility determination, current-voltage characteristics of Schottky diode

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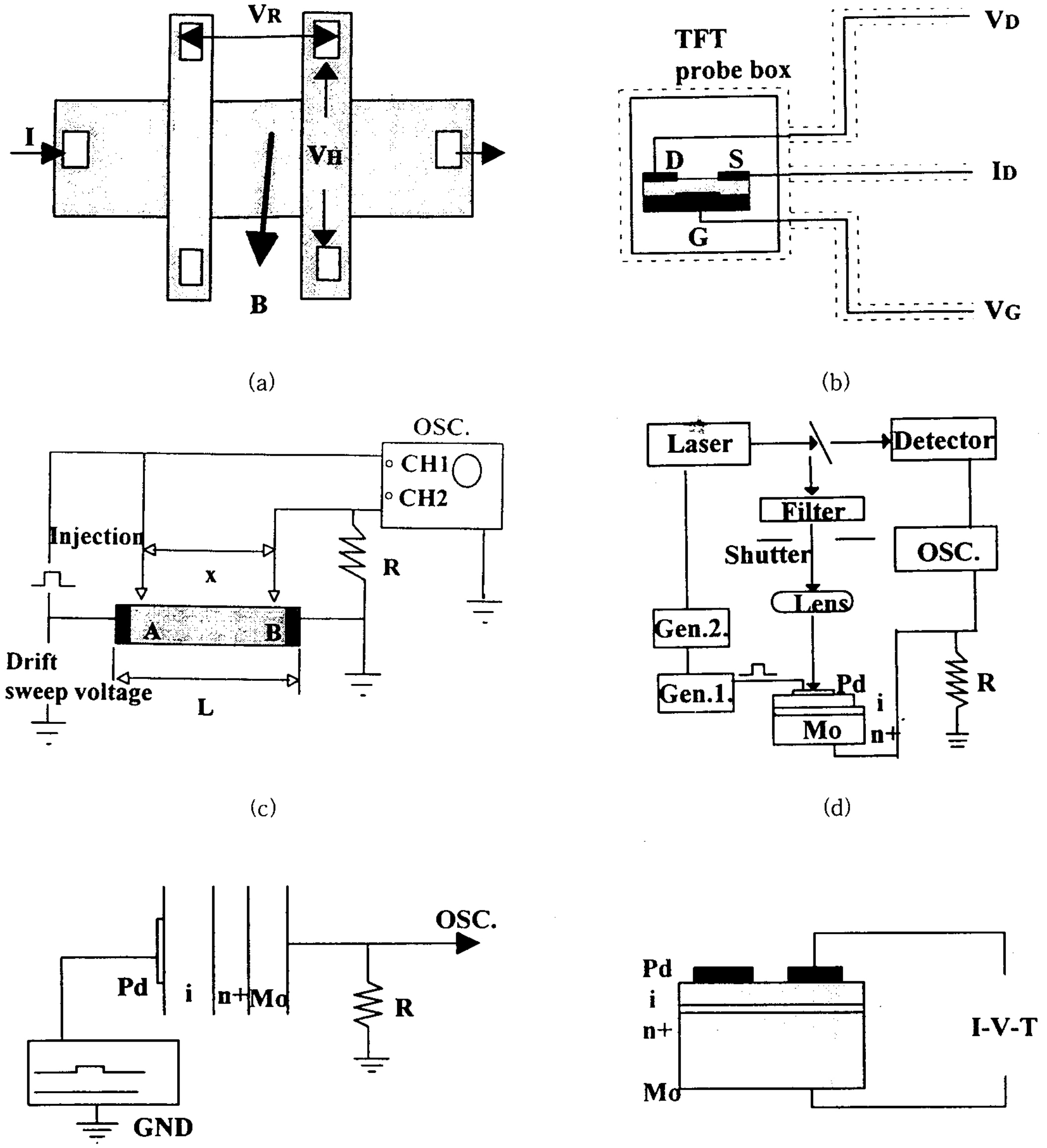
were examined. A cathode injects non-equilibrium density of electronic charge that populates the empty gap states above the Fermi-energy level. When the applied voltage is large enough, extra charge extends across the entire sample thickness and the current collected by the anode becomes space charge limited. Almost all the charges are trapped, but exponentially small fractions are thermally promoted to the conduction band. Transient current observation with small step voltage application utilizes charge variation because of a step voltage. A small additional voltage ΔV is superimposed onto a device already subjected to a forward bias V. By observing current rise time, mobility is calculated from $\mu = d/(E \cdot t_t)$ where d is the electrode distance, E the applied electric field, and t_t the transit time. The traps in thin film Si were assumed to be filled by an applied bias. Mobility measurement using TOF and HS method take the same formula as in transient current observation with step volt application. The field effect mobility was calculated from the transconductance method for a-Si:H and poly-Si TFTs.

2. Experiment

Due to the importance of poly-Si for the device applications, substantial experimental effort has been directed toward different crystallization conditions and subsequent characterizations of thin film Si. The employed crystallization techniques were furnace anneal in nitrogen atmosphere, anneal in a vacuum, and RTA. Partial or the whole Mo layer was removed to characterize the mobility of thin film Si (22). Van der Pauw resistivity, Hall effect mobility, Haynes-Shockley method, and field effect mobility were measured after the partial Mo substrate removal. Figure 1 shows the sample structure and mobility measurement set-up for the various methods. A Schottky diode was fabricated to examine TOF, SCLC mobility, and transient current observation with step volt application. The silicon samples were cleaned using an organic cleaning method. The buffered HF solution was used to remove the native thin oxide. Schottky barrier forming metals were evaporated using a Denton DV502 evaporator. The metal Pd or Au was employed to form a Schottky barrier on intrinsic and n-type Si. The metal Cr was evaporated to make the Schottky diode on p-type Si. Current-voltage-temperature (I-V-T) characteristics were examined on the sample structures of Pd/i/n^+/Mo, Pd/n/n^+/Mo, and Cr/p/p^+/Mo. Modified Hall effect system of Keithley 80A was employed to measure van der Pauw resistivity and Hall mobility of the thin film Si.

A novel TFT fabrication process was developed by using the Mo substrate as source and drain contact. Dry oxygen gas introduction during SiO evaporation was effective to achieve a high quality insulator. The base pressure for SiO evaporation was low 10^{-7}Torr. An oxygen gas flow maintained at a pressure of low 10^{-4}Torr gave a slow deposition rate of 130Å/min. The evaporated SiO with oxygen gas introduction exhibited low surface states, low mobile oxide charges, comparable leakage current, and dielectric constant of about 5. Mainly, SiO, SiO_2, and Si_3N_4 insulators were investigated because of their low leakage current characteristics. Thickness of the insulator measured by α-step, SEM, and thickness monitor ranged from 50nm to 1000nm. The Mo substrate was used as an electrical contact pad of drain and source. Forty-second wet etching in diluted Sirtl etchant removed the n^+ layer between drain and source contacts. Optical microscope and SEM were employed to examine the fabricated TFT structure. Current-voltage characteristics were measured by using an HP4145B semiconductor parameter analyzer and computer data acquisition system. TFT output influencing factors were examined such as anneal temperature, optical, gate dimension,



(a) (b) (c) (d) (e) (f)

Fig. 1. The employed set-up and sample structure in mobility measurement.
(a)Hall effect, (b)TFT, (c)HS, (d)TOF, (e)Transion current observation, and (f)SCLC.

Si film thickness, insulator thickness, and grain boundary passivation.

3. Results and Discussions

Conductivity method can be used if carrier concentration is known (μ_n=1/qnρ). Assuming the carrier density of intrinsic a-Si:H as 10^{14}cm^{-3} the mobility is calculated to be 6.25x10^{-4}cm^2/V.s. This method requires to know exact number of conduction carriers which was not easy for both a-Si:H and poly-Si. For intrinsic a-Si:H film a

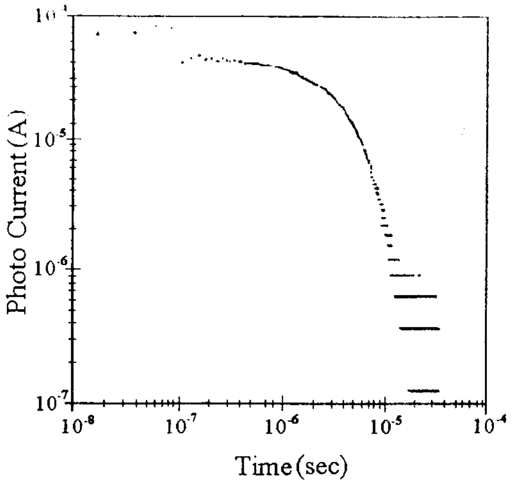


Fig. 2. The transient response for the n-type 5μm thick as-grown a-Si:H.

Table 1. Mobility of the As-deposited A-Si:H.

Sample	Electric Field (kV/cm)	Transit Time (s)	Mobility ($cm^2/V \cdot s$)
Pd/i/n^+/Mo	14.5	3.0×10^{8}	1.15
Cr/n/n^+/Mo	4.0	2.5×10^{-6}	0.05

measured resistivity was ranged over $10^8 \Omega$-cm. This high resistivity of a-Si:H in Hall measurement system made the constant current to be maintained less than 10^{-12} amperes for a sample size of 1cm × 1cm. High fluctuations in mobility value were observed for the high resistivity of a-Si:H. The measured mobility by Hall effect was ranged from 1 to $10 cm^2/V.s$ for anneal treated intrinsic poly-Si film. The HS mobility can be calculated from $\mu = x/E \cdot t_d$ where x is defined as distance between two probes, E applied electric field, and t_d delay time between the pulse injection and collection. An anneal treatment of 850℃, 4h gave the HS mobility of $3.3 cm^2/V.s$ with x=0.05cm, L=1cm, V=15V, t_d=1ms. However, HS method requires either lower probe distance or higher electric field to determine the mobility of a-Si:H films. The TOF result is shown in Fig. 2 for the as-grown n-type, 5μm thick a-Si:H. The carrier transit time was 2.5×10^{-6}s for an electric field of 4.0kV/cm. Table 1 shows the calculated mobility values $1.15 cm^2/V.s$ for intrinsic a-Si:H and $0.05 cm^2/V.s$ for n-type a-Si:H. Increased doping density in n-type a-Si:H may have contributed to reduce the carrier mobility via impurity scattering process. The advantage of the TOF method is that electron and hole mobility can be decided by reversing the applied field. However, the TOF method exhibited difficulties in mobility measurement of poly-Si because of a large leakage current.

Most of the prior mentioned methods were good for only either a-Si:H or poly-Si. SCLC, TFT, and transient current observation with step volt application permitted a mobility determination for both a-Si:H and poly-Si. A plot of I versus V^2 gives a straight line when the SCLC mechanism is dominant. Dark I-V-T measurements on a-Si:H Schottky barrier diodes have been interpreted as evidence for the SCLC process. Figure 3 shows the straight lines on I-V^2 graph for the 850℃ annealed intrinsic 5μm sample. The SCLC method can deduce the mobilities for both a-Si:H and poly-Si. The space charge limited current density, J_{SCLC} is given by

$$J_{SCLC} = Q_{inj}/t_t = F\varepsilon_s\varepsilon_o\mu V^2/L^3 \qquad (1)$$

where F is an experimental correction factor and t_t the carrier transit time.

Using equation (1), the calculated mobility changed from $0.039 cm^2/V.s$ for a-Si:H to $5.5 cm^2/V.s$ for the 850℃ annealed intrinsic 5μm sample. The mobility was increased by 140 times after the 850℃ anneal treatment with and without using the correction factor. Limitation of SCLC method is that this technique is valid only for the intrinsic Si films where SCLC mechanisms were observed. The Schottky diode structure of Pd/n/n^+/Mo

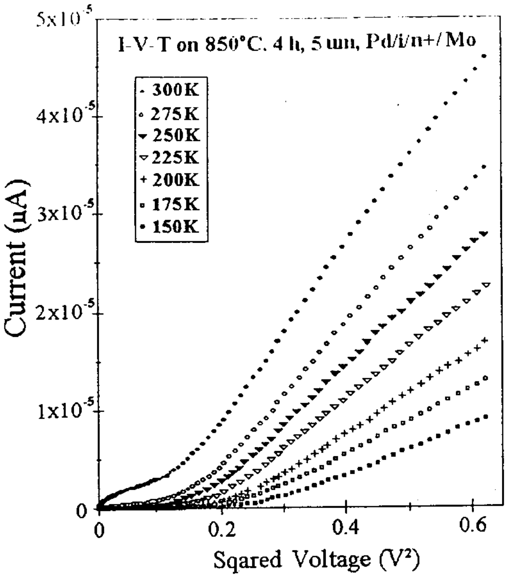


Fig. 3. I-V^2 plot for intrinsic 5μm thick silicon after 850℃, 4h.

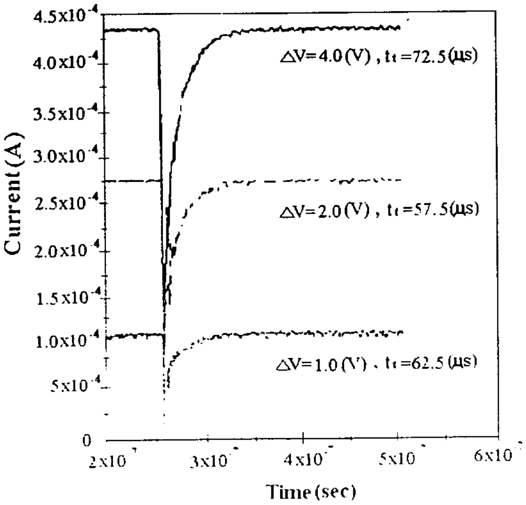


Fig. 4. The current transient characteristics of intrinsic 5μm thick a-Si:H after 850℃, 4h anneal.

and Cr/p/p^+/Mo showed different conduction mechanisms such as Frankel-Poole emission or field emission mechanism.

Figure 4 shows observed current transition time on an intrinsic 5μm thick, 850℃, 4h anneal treated sample. As the amplitude of step volt (ΔV) varies from 1.0V to 4.0V, the transit time increased from 62.5μs to 72.5μs. Table 2 shows calculated mobility result for as grown a-Si:H and 850℃, 4h anneal treated poly-Si. Figure 5 summarizes the measured mobilities as a function of anneal temperature. Mobility increases from 0.1 for a-Si:H to 15cm²/V.s for 850℃ annealed poly-Si sample. Reduction in mobility after 400℃ annealing can be explained by the increased defect density due to the evolution of weakly bonded hydrogens. Mobility increases at high temperature anneal because of the improvement in

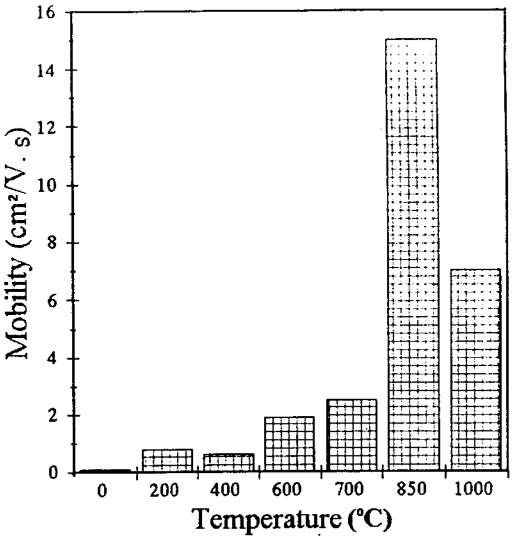


Fig. 5. Mobility versus anneal temperature on intrinsic 5μm thick Si film (Pd/i/n^+/Mo).

Table 2. Mobility of the As-grown Intrinsic a-Si:H and 850℃, 4h annealed intrinsic 5μm thick (Pd/ i/n+/Mo).

Anneal (℃)	V_{step} (V)	V (V)	t_t ($\times 10^{-9}$s)	μ (cm²/V · s)
As-grown	1	10	62.5	0.400
	2	11	57.5	0.390
	4	13	72.5	0.265
850℃, 4h	0.5	5	3.0	16.0
	1.0	6	2.5	16.5
	2.0	7	2.2	16.2

crystallinity. Increased mobility can contribute to increase short circuit current of the PV device and increase switching speed of the TFT. Decreased mobility after 1000℃ anneal may be related to the structural degradation of the Si film. Silicon interacted with the Mo substrate for the anneal temperature above 1000℃. X-ray diffraction detected strong molybdenum silicide peaks for anneal temperature above 1000℃.

The last method in mobility examinations deals with TFT characteristics as a function of anneal temperature. Transconductance (g_m) and field effect mobility (μ_{FE}) can be given as in equation (2) and (3).

$$g_m = \frac{W}{L}\mu_{FE}C_i V_{DS} \quad (2)$$

$$\mu_{FE} = \frac{Lg_m}{WC_i V_{DS}} \quad (3)$$

where C_i is an insulator capacitance and V_{DS} drain to source voltage. Inverted staggered type TFT output is strongly influenced by series resistance from source to channel and drain to channel. A film thickness less than 0.5μm was employed for the study. As Si film thickness is increased, the series resistance was increased very high and the drain current level stayed in the order of 10^{-12} ampere region. A relatively high turn-on voltage (V_T) of 12V was observed for the TFT on as-grown intrinsic a-Si:H. The TFT on as-grown a-Si:H exhibited a field effect mobility of $1.6\times10^{-3}cm^2/V\cdot s$ with evaporated SiO gate insulator layer. Oxygen introduction during SiO evaporation was very effective in reducing interface trap density and mobile oxide charge. Sameshima et al. reported very low interface density of $5\times10^{10}cm^{-2}eV^{-1}$ using the oxygen introduction method during SiO evaporation (23). This indicates that low interface state density can be achieved by this method. TFT output characteristics after RTA 600℃, 2min. exhibited well-saturated drain current (I_D), improved g_m, and reduced V_T. A further improvement of TFT device performance was observed on high temperature (>700℃) annealed intrinsic Si film with high ON current and low OFF current. The I_{ON}/I_{OFF} ratio of 10^6 was achieved after RTA 850℃, 2min. An increased I_D and g_m contributed to improve field effect mobility after hydrogen grain boundary passivation as shown in Fig. 6. Mobility stays in the order of $10^{-3}cm^2/V.s$ for the anneal temperature below 600℃. An anneal treatment higher than 700℃ gave about three-order improvement in field effect mobility. Some of the sample exhibited very high field effect mobility to $20\sim67cm^2/V.s$ after the high temperature anneal and grain boundary passivation using the RF plasma rehydrogenation. A summary of the field effect mobility for the various anneal temperatures is shown in Fig. 7. The optimized conditions of the RF plasma rehydrogenation are the substrate temperature of 300℃, exposure time of 6h, and electrode distance of 1.2cm spacing from the substrate holder. The drain current ratio in light and dark was reduced from 31 for as grown

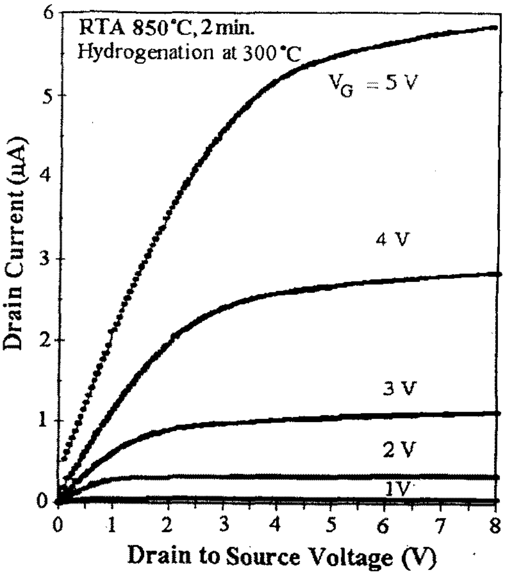


Fig. 6. The inverted staggered type TFT on RTA 850℃, 2min. and RF rehydrogenated at substrate temperature of 300℃, 4h.

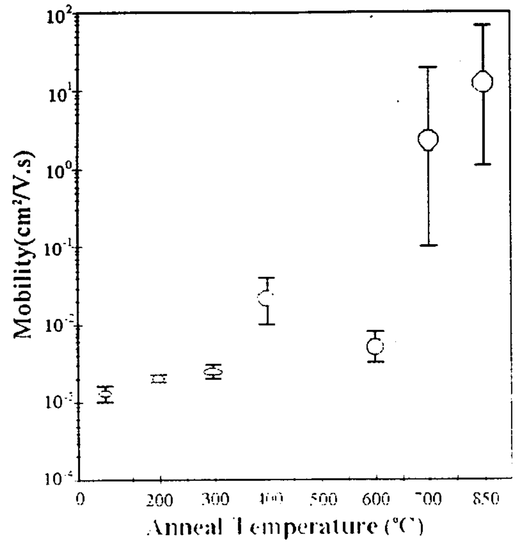


Fig. 7. The summary of field effect mobility as a function of anneal temperature.

a-Si:H to 3.6 after 600℃ and 1.3 after 850℃, 4h vacuum anneal. The light response study indicates that the poly-Si TFT is stable when exposed to external light bias.

4. Conclusions

The results from the various methods of mobility measurements indicate that TFT, SCLC, and transient current observation methods could be used for a-Si:H and poly-Si. Hall mobility and HS method are not readily applicable to highly resistive a-Si:H films. TOF method is recommended for the mobility determination of a-Si:H films. All of the investigated method exhibited some limitations to a certain degree. TFT method showed some limiting factors such as the film thickness of Si and insulator, TFT structure, and interface state between silicon and insulator. The measured mobilities in a-Si:H exhibited large differences partly because of the measurement resolution and partly the high resistivity of a-Si:H film. Deviations of the mobility values from the various methods are mostly within an order difference for poly-Si. Because of the surface states and insulator quality of TFT, the field effect mobility showed lower values than that of SCLC and current transient observation method. We recommend crystallization temperature of 850°C, because TFT fabricated after 850°C anneal and grain boundary passivation gave mobility as high as $67cm^2/V \cdot s$. Our study was only focused on Mo substrate, however, further study will be directed to the low cost substrate that could withstand high temperature anneal. Since our investigation was focused on mobility determination after the various anneal treatments, we recommend either TFT or transient current observation method for the future analysis of thin film Si.

References

[1] J. Ohwada, M. Takabataka, Y. Ono, A. Mimura, K. Ono, and N. Konishi, IEEE Trans. on Elect Dev., Vol. 30, No. 9, p.1923, 1989.

[2] D. C. Look, Electrical Characterization of GaAs Materials and Devices, John Wiley & Sons, NY, p.2, 1989.

[3] L. Solymar and D. Walsh, Lectures on the Electrical Properties of Materials, Oxford University Press, NY, p.170, 1985.

[4] B. J. Streetman, Solid State Electronic Devices, Prentice-Hall, NJ, p.80, 1980.

[5] R. I. Dalven and E. A. Sciff, J. of Non-Cryst. Solids, Vol. 141, p.106, 1992.

[6] J. M. Marchall , R. A. Street, and M. J. Thompson, Phil. Mag. B, Vol. 54, No. 1, p.51, 1986.

[7] H. M. Wentinic and W. Crans, IEEE Trans. on Elect. Dev. Vol. 36, No. 12, p.2803, 1989.

[8] R. A. Street, Physical Review B, Vol. 27, No. p.8, 1983.

[9] A. Madan and M. Shaw, The Physics and Application of Amorphous Semiconductor, Academic Press, Boston, p.199, 1988.

[10] S. Demnda and M. A. Nicolet, J. of Appl. Phys., Vol. 37, No. 6, p.2412, 1966.

[11] H. Kakinuma, M. Mouri, and H. Sawai, J. Appl. Phys., Vol. 67, No. 1, p.558, 1990.

[12] S. Nespurek and J. Sworawoski, J. Appl. Phys., Vol. 51, No. 4, p.2098, 1980.

[13] R. M. Dawson, C. R. Wronski, and M. Bennett, Appl. Phys. Lett, Vol. 58. No. 3, p.272, 1991.

[14] A. A. Grinberg and N. Schryer, IEEE Trans. on Elect. Dev., Vol. 36, No. 6, p.1162, 1989

[15] Richard H. Jarman, J. Appl. Phys., Vol. 60, No. 3, p.1210, 1986.

[16] A. C. Trickle, Thin Film Transistors, John Wiley & Sons, NY, 1969.

[17] L. Kazamerski, Polycrystalline and Amorphous Thin Film and Devices, Academic Press, NY, p.201, 1980.

[18] J. Choi and G. Neudeck, IEEE Trans. on Elect. Dev., Vol. 39, No. 11, p.2525, 1992.

[19] E. Snow and M. Silver, J. of Non-Cryst. Solids, Vol. 77, p.451, 1985.

[20] M. Silver and D. Adler, Phil. Mag. B, Vol. 53, No. 4, p.L-89, 1986.

[21] F. Shapiro, and M. Silver, IEEE Trans. on Elect. Dev., Vol. 36, No. 12, p.2785, 1989.

[22] J. Yi, Engineering and Science Letters in Sung Kyun Kwan University, Vol. 47, No. 2, p.57, 1996.

[23] T. Sameshima, A. Kohono, M. Sekiys, M. Hara, and Sano, Appl. Phys. Lett., Vol. 64, p.1018, 1994.

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