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APPLICATIONS OF SOI DEVICE TECHNOLOGY

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ABSTRACT

The progress of microelectronics technology has been requiring agressive developments of device technologies. Also the requirements of the next generation devices is heading to the limits of their functions and materials, and hence asking the very specific silicon wafer such as SOI(Silicon On Insulator) wafer. The talk covers the dome stic and world-wide status of SOI device developments and applications. The presentation will also touch some predictions such as SOI device prgress schedules, impacts on the normal wafer developments, market sizes, SOI wafer prices, and so on. Finally it will cover technical aspects which are silicon oxide conditions for bonding, point defects and, surface contaminations. These points will be hopefully overcome by involved people in microelectronics industry.

INTRODUCTION

The progress of microelectronic technology has kept facing the very limited technology requirements especially of silicon wafer quality. The trend of the recent wafer reqiurements proceeds toward the so called revolutionary directions of wafer diversification. First, the settlement of wafer issues at Semicon/Japan94 is to install the mass production facilities of 12 inch wafers in 1998 and to start mass production in 1999[1]. Hence before this century, 12 inch wafer like laser disc would appear in the market. Second, some specifications such as warp, flatness, and roughness being now applied for 8 inch wafers will no longer be applied for 12 inch wafers. Therefore, along with increasing wafer diameter, the appearance of superflattening technologies like CMP(Chemomechanical Polishing) is required for the higher device integration. Third, two types of the next generation wafers mentioned above can be said to be on the extrapolation of the existing device technology requirements, and hence other newly concepted wafers have been pushed to be developed in the research and application areas so that at last the next generation wafer called SOI(Silicon On Insulator) wafer appears for the next generation devices. SOI device can be manufactured by inserting a dielectric film such as silicon oxide forming three layers which are a substrate silicon layer for the mechnical support, a dielectric layer for the electrical insulation, and a very thin silicon layer for the device fabrication as shown in Fig. 1. This SOI devicing technology has become very meaningful technology-wise, process-wise, and characteristic-swise because of its influential potential on the mic-

roelectronics technology and must be given a special attention.

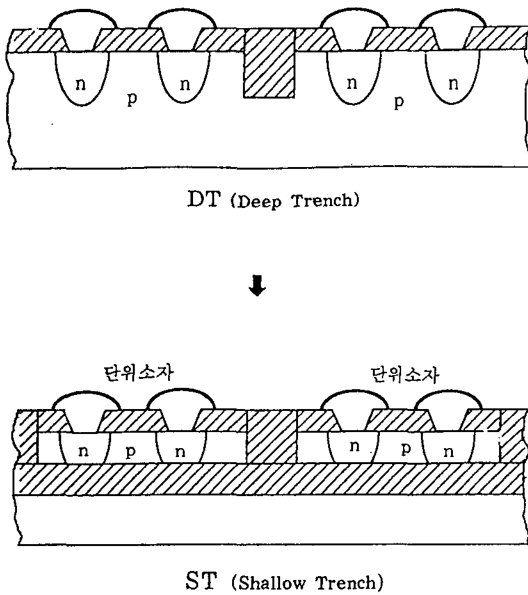


Fig 1. Cross Section Views of Bulk and SOI Devices

STATUS OF SOI TECHNOLOGY DEVELOPMENT

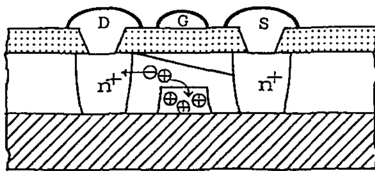
Domestic status are moving quickly even though many aspects are still very primitive. Three major device makers are interested in device fabrication using SOI substrates, but unitil now the supply of SOI substrates is not massive, facing a stability problem in quantity and a reliability problem in quality. Hence they operate their own laboratories for SOI substrate development as well as SOI device development or are planning SOI projects. Samsung is focusing on wafer bonding for SOI development and searching for any likely ways to acquire and to establish the related manufacturing technology and equipments. At the end of April, 1995, Samsung finally announced the 16 MDRAM development using 6 inch bonded SOI wafers[2]. Hyundai Electronic also announced its development of 64MDRAM with SOI wafers in the middle of 1996. LG Electronic is not so much as others in progress so far. Meanwhile, LG siltron as a wafer manufacturer is driving a project of SOI wafer technology establishment and looking for channels as many as possible to secure the technology establishment. More importantly as usual,international market is moving fast. In 1986 Lasky of IBM first announced BESOI technology which utilized a epi-layer for a chemical etch stop at the inferface of the epi-layer and the substrate[3]. Applications of SOI wafers for device fabrication were mostly taken place 80th and at the end of 1994 Nishihara of SONY developed a unit cell for 1 GDRAM using SOI wafers[4]. In this development process some inherent characteristics belonging only to SOI devices have been observed, studied, and evaluated from the view point of their mass production potential[5-6]. However, above all, the most important point has been the stable, reliable, and massive supply of SOI wafers of which technologies have been converged to three majors of SIMOX, BESOI and PESOI technologies. The possibility of mass production of SOI wafers will impact the 12 inch device market development, and hence be a control factor for the next generation device technology trends.

SOI DEVICE TECHNOLOGY

ULSI SOI devices can be divided into two categories. One is that the silicon layer thickness is about 1,000 A or less and hence the fabricated device is assumed to be fully de-

pleted(FD) as in (a) of Fig. 2. The other is that the silicon layer thickness is more than 1,000 A so that some neutral region is left and the device is not fully depleted but partially depleted(PD) as in (b). In any case, trenching and imbeding silicon oxide or other insulators can isolate each SOI device electrically completely. Also, any noise that may be induced from the device environments such as alpha particles can be minimized. Also due to their structures, SOI devices are characteristic with very low parasitic capacitances as well as low leakage current at OFF state. Therefore SOI devices can be operated at 1.5 V which is the pursuing goal of portable personal computer operation. Actually SOI devices can realize the miniaturization and low power operation of the future integrated de vices.

Seperating two cases of Fig. 2(a) and (b)



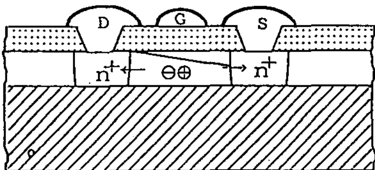


Fig. 2 Difference between Partially Depleted and Fully Depleted Devices

also provides very a intersting point due to their thickness differences. In case of PD in (b), electrons generated in the depletion region by many reasons drift towards the drain (D) region while holes enter the neutral region and are accumulated there. The accumulated holes build up the voltage which is equivalent to some intentional voltage application across the gate(G). Hence, it causes changes of the gate voltage for the designed operation, which is called floating body effect. However, in case of FD in (a), there is no neutral region left and no hole accumulation, no gate voltage changes and no floating body effect. Again, the phenomenon affects the source(S)-to-drain(D) current to change suddenly to a burst fashion, which is called the kink effect for PD SOI devices. Another specific property of FD SOI devices is that they show the ideal value of 60 mV/decade in the current-voltage curve. Hence in many aspects, FD SOI devices are concluded to be superior to PD SOI devices. With the above mentioned characteristics of SOI devices, it is expected that the device process steps can be reduced up to 40% causing process cost cuts and tremendous yield improvement. Also by the process elimination such as formation of LOCOS and deep trench which occupy rather larger wafer surface area and cause other problems and additional processes, more integration can be realized using the present device technology. Eventually the present 8 inch line may accommodates the next generation device fabrications beyond 256 MDRAM.

Other application areas than ULSI are MEMS(Micro-Electro Mechnical System), MOMS (Micro-Opto Mechanical System), LIGA(Lithographic Galvano Formung &

Abformung), and so on. These areas are getting intensively attentions recently because the present ULSI device technology can be directly applided to fabricate easily MEMS devices as well as integration of MEMS devices with their control devices as in Fig. 3[7]. LIGA components which are practically larger in size than MEMS devices can also be fabricated with very minor modifications of ULSI fabrication concepts. Accelarometers, pressure or gas sensors, and micro gears are examples of SOI device applications. Here using SOI technology has two major advantages over the conventional device technology. Sacrificial layer of silicon oxide is embedded in a starting material so that the necessary components can easily be isolated or seperated from the substrate, and the top devicing layer thickness can be controlled in any scale which gives tremendous release to the device designers and process people.

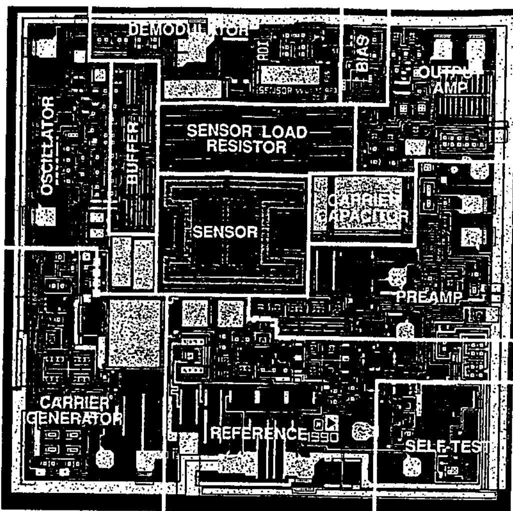


Fig. 3 Integrated Accelarometer with control

CONCLUSIONS

For SOI wafer application arguement for the next generation device fabrication, two points must be considered, which are the investment costs of the next generation device fabrication facility and the comparison of prices between 8 inch SOI wafers and 12 inch bulk wafer except for the above mentioned technical merits of SOI wafers. Hence 8 inch SOI wafers may influnce the presence of 12 inch bulk wafers in 1999 by some ways. Timing of 8 inch SOI wafer presence also match well with 12 inch bulk presence. In 1994, 0.1 μm thick SOI wafers were developed and 0.5 μm SOI wafers are in the market as a sample scale. Size-wise, 8 inch SOI wafers appeared in 1994 and 8 inch 0.1 μm thick SOI wafers are forcasted to be produced massively by the year of 2000. The present price of a 8 inch SOI wafer which is more than 500 dollars must be about 200 dollars by the year of 2000. It is not easily predictible to estimate the total market sizes by now by lack of market analysis data. However, the international market demand that will be about 100 million dollars by the end of 1995 is expected to grow up to 2-4 billion dollars by the end of this century and the domestic market size is expected to be one tenth of the world market based upon the present share of wafer market. Also considering the related businesses such as SOI equipment market, the domestic market is expected to be about 300 million dollars by that time.

The most critical point to manufacture SOI wafer is to polish large wafers leaving behind 1,000 A thick silicon layers on the top of silicon oxide layer. By now the most promising technology to manufacture 8 inch SOI wafer fulfilling this requirement is to apply plasma system to etch large area very quickly for massive production. This plasma technology can provide the fast throughput as well as the required uniformity and thickness control.

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