A Novel Multi-Level Inverter Configuration for High Voltage Conversion System

Bum-Seok Suh, Yo-Han Lee, and Dong-Seok Hyun

Abstract

This paper deals with a new multi-level high voltage source inverter with GTO Thyristors. Recently, a multi-level approach seems to be the best suited for implementing high voltage conversion systems because it leads to harmonic reduction and deals with safe high power conversion systems independent of the dynamic switching characteristics of each power semiconductor device. A conventional multi-level inverter has some problems; voltage unbalance between DC-link capacitors and larger blocking voltage across the inner switching devices. To solve these problems, the novel multi-level inverter structure is proposed.

I. Introduction

The highest power GTO Thyristor presently available blocks 4500V while switching-off 3000A. Considering minimal stress margins, conventional GTO inverters has a limitation of its DC-link voltage about 2000V. So series connection of GTOs is needed to cover the high voltage and often used to reduce the device voltage stresses in such high power conversion systems. Synchronizing the switching is very difficult because of the inherent differences in the switching characteristics of each device possibly causing stresses on individual devices. Therefore, it requires that large snubber capacitors should be used to minimize transient voltage unbalance and large resistors in parallel with each switch should be used to achieve static balancing. These elements increase switching losses and switching time, therefore multi-level inverters are more suitable for mitigating these issues in high power conversion systems [1-3]. Multi-level inverters clamp the blocking voltage of each switch to divided voltage levels and also reduce the harmonic components from those obtained with conventional two-level inverters at the same switching frequency. However, multi-level inverters have some drawbacks such as voltage unbalance between the DC-link capacitors and a higher blocking voltage across the inner switching devices [2, 3].

In this paper, we first describe, in detail, the problems of a conventional multi-level inverter and then propose a new multi-level inverter topology that can reduce these problems.

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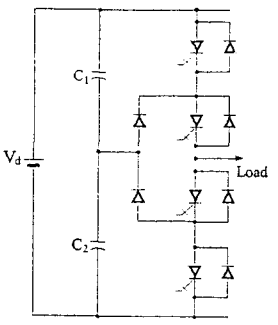
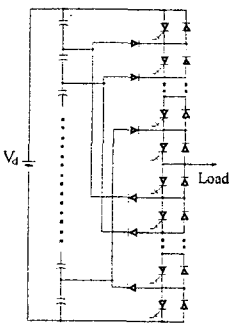
The authors are with Department of Electrical Engineering, Hanyang University, Seoul, Korea.

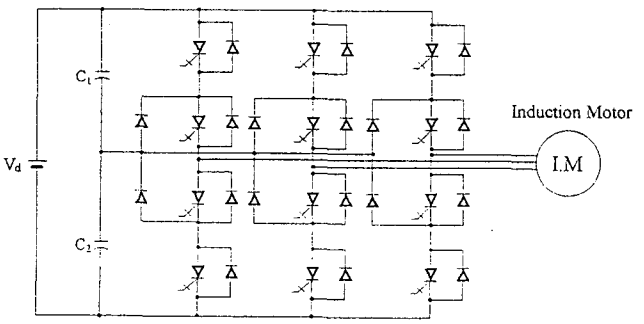
II. Conventional Multi-Level Inverter



(a) Three-level leg



(b) Multi-level leg



(c) Schematic diagram of a conventional three-level GTO inverter

Fig. 1. Conventional multi-level inverters.

Fig. 1 shows the structures of the conventional three- and multi-level inverter. From now on, we treat only three-level inverter structure for better understanding.

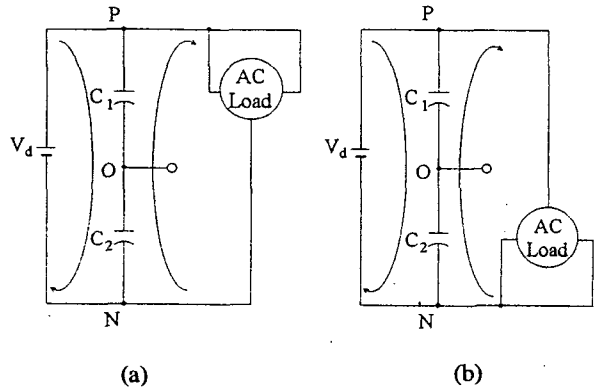
1. Voltage unbalance between DC-link capacitors

Switching states of each phase of the conventional three-level inverter are listed with symbols in Table I [4, 5]. Since three kinds of switching states exist in each phase, a three-level inverter has $27(=3^3)$ switching states. Fig. 2 shows the load connections of each power in a three-level inverter. Fig. 2 (a) and (b) have no effect on the unbalance of the DC-link capacitors because the load is not connected between neutral point and the upper/lower rail. Fig. 2 (c) is somewhat effective in reducing voltage unbalance. Fig. 2 (d), (e), (f) and (g) have most effect on the balancing because either upper or lower capacitor as an energy tank is used to supply power to the load. The capacitor C_2 voltage increases in case (d) and (e) and decreases in case (f) and (g) according to charging/discharging action. Since states (d), (f) and states (e), (g) generate the same inverter output voltages, various space vector PWM techniques controlling the duration times of (d), (f) and (e), (g) have been studied in order to suppress the fluctuations of neutral point voltage [4, 5, 8]. However, the limitations of the operating speed and frequency of power semiconductor devices render these prior art schemes ineffective in suppressing these fluctuations which then result in the inverter output current varying, in time, with the output voltage waveform. This output therefore contains second and higher order even harmonics, which are damaging to AC drives [8]. By maintaining the inverter output waveforms in half-wave symmetry, the technique proposed in this paper eliminates the above concern. This is achieved by maintaining the two DC-link capacitors in a balanced condition which guarantees true three-level operation over the entire range of the output voltage waveform.

Table 1. Switching States of a Conventional Three-Level Inverter

(x = u, v, w)

Switching symbols	Switching conditions				Output voltages
	G_{1x}	G_{2x}	G_{3x}	G_{4x}	
P	ON	ON	OFF	OFF	V_d
O	OFF	ON	ON	OFF	$V_d/2$
N	OFF	OFF	ON	ON	0



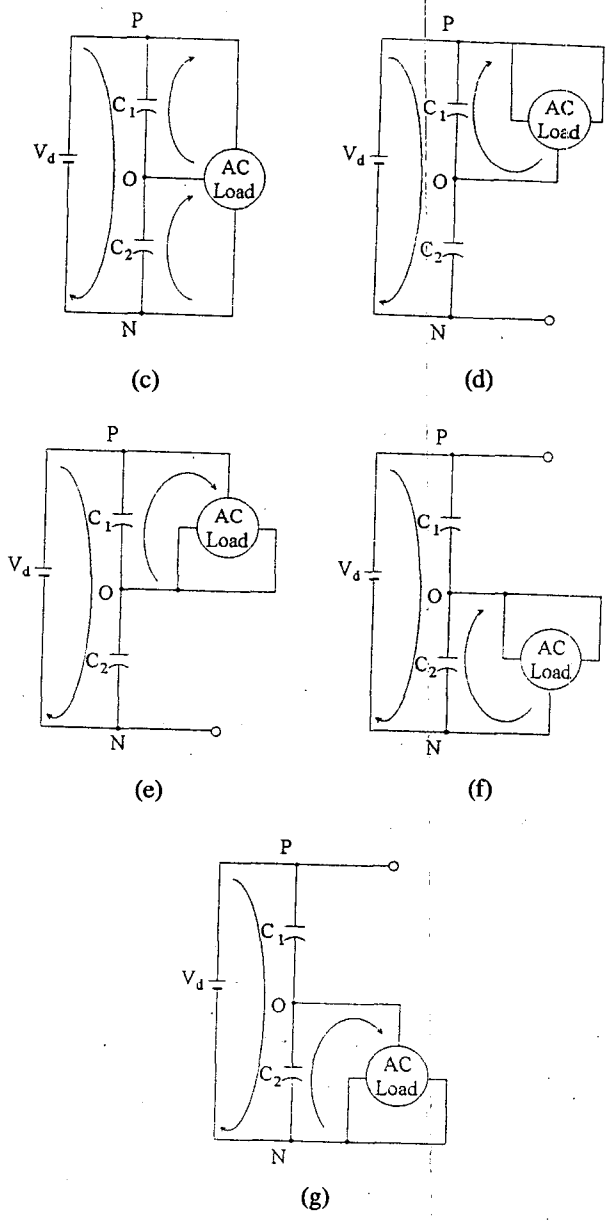
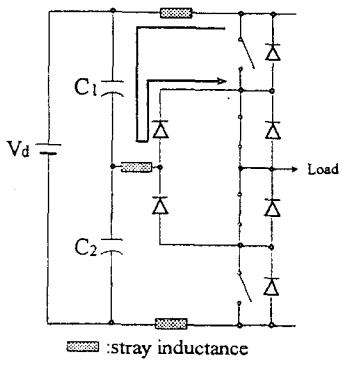


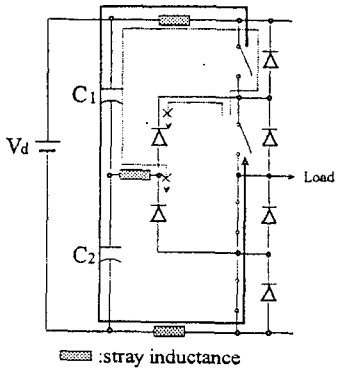
Fig. 2. Load connections of each power. (a) switching states: PPN, PNP, NPP. (b) switching states: PNN, NPN, NNP. (c) switching states: PON, PNO, OPN, ONP, NPO, NOP. (d) switching states: PPO, POP, OPP. (e) switching states: POO, OPO, OOP. (f) switching states: OON, ONO, NOO. (g) switching states: ONN, NON, NNO.

2. Unbalance of voltage sharing between switches at turn-off

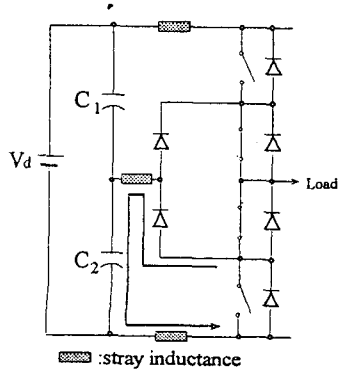
The phase voltage of a conventional three-level inverter changes only as much as one step voltage. That is, a change of phase voltage from 0 to V_d and vice versa never happens. This means that there is no need to turn off two switches simultaneously while turning on the other two in a three-level inverter. Therefore, voltage sharing, which is the reason for series connection of semiconductor devices, does not matter in a three-level inverter[2-3]. But each switch has over-voltages spikes during the turn-off transient state due to inductance elements in the inverter circuit. When this situation occurs, the outer switches can be clamped to half the DC-link voltage by the independent overvoltage discharge paths shown by solid lines in Fig. 3 (a) and (c). In case of turn-off of the inner switches, however, the overvoltages caused by energy stored in stray inductances cannot be perfectly discharged to half the DC-link voltage because independent discharge paths aren't as shown by dotted lines in Fig. 3 (b), (d) and the overvoltages are discharged to DC-link voltage with the voltages across the outer switches turned off as shown by solid lines in Fig. 3 (b), (d). Hence, the blocking voltages across the inner switches become larger than half the DC-link voltage[3, 7]. Fig. 3 (e) shows the unbalance of voltage sharing between the switches and power dissipation comparisons during a GTOs turn-off transient state in a three-level GTO inverter.



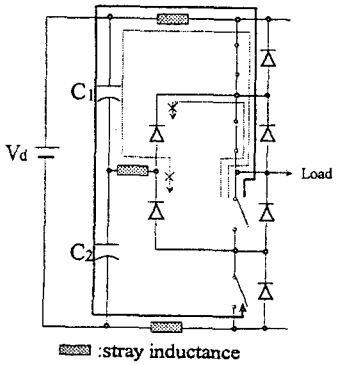
(a) Upper outer switch



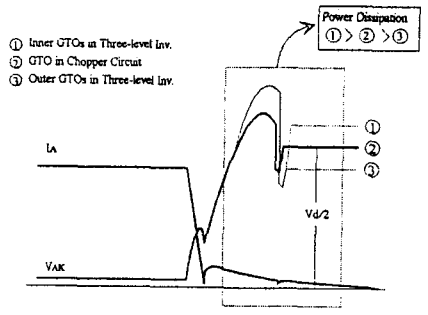
(b) upper inner switch



(c) lower outer switch



(d) lower inner switch



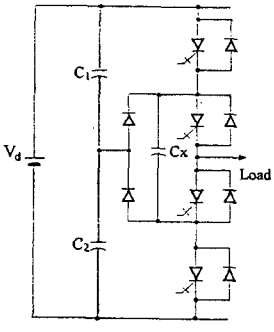
(e) Unbalanced blocking voltage and power dissipations at turn-off

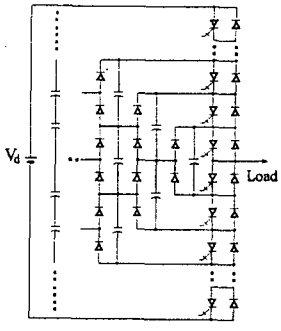
Fig. 3. Discharge paths of the overvoltage across each dissipations at turn-off.

III. New Multi-Level Inverter

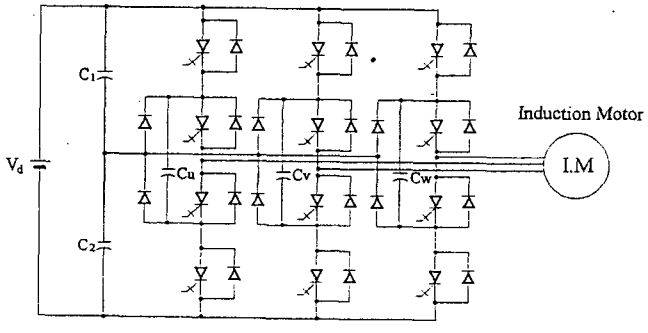
1. Topology

Fig. 4 (a) and (b) show one leg of a new three- and multi-level inverter structure. In Fig. 4 (a), note that there is an inner clamping capacitor C_x, not found in a conventional three-level inverter structure shown in Fig. 1 (a). The





(a) Three-level leg(x=u, v, w) (b) Multi-level leg



(c) Schematic diagram of a new three-level GTO inverter

Fig. 4. New multi-level inverters.

DC-link voltage sources supply power to the loads. Fig. 4 (c) shows a schematic diagram of the new three-level GTO inverter. The branch diodes are connected to the neutral point 'o' of DC capacitors. Switching states of each phase of the inverter are listed in Table Ⅱ.

Table 2. Switching States of a New Three-Level Inverter

(x = u, v, w)

Switching modes	Output levels	Switching conditions				Output voltages
		G1x	G2x	G3x	G4x	
1	1	ON	ON	OFF	OFF	V_d
2A	1/2	OFF	ON	OFF	ON	$V_d/2$
2B	1/2	ON	OFF	ON	OFF	$V_d/2$
3	0	OFF	OFF	ON	ON	0

At each switching mode, current paths are formed as follows:

1) Mode 1

In this mode, the operating principle is shown in Fig. 5 (a). Output voltage becomes V_d through G_1-G_2 turned on and a bidirectional current path for AC load is achieved through free-wheeling diodes D_{f2}-D_{f1} as shown by solid paths. If the voltage of capacitor C_x is higher than $V_d/2$, it will be discharged along with the load current as shown by dotted path ①. On the contrary, if the voltage of the capacitor C_x is lower than $V_d/2$, it will be charged to $V_d/2$ by discharging capacitor C_1 as shown by dotted path ②. This means that DC-link capacitors' voltages are adjusted evenly while a desirable output voltage is achieved.

2) Mode 2A

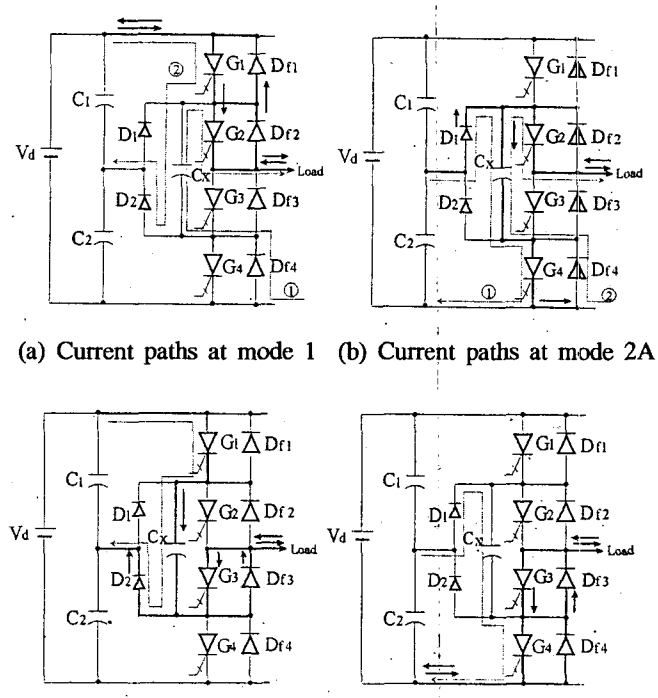
Current paths are shown in Fig. 5 (b). Output voltage $V_d/2$ is formed by the capacitor C_2 voltage that is discharged through branch diode D_1 and switch G_2, and a bidirectional current path for AC load is D_{f2}-C_x-G_4 as shown by solid paths. The voltage of the capacitor Cx can be charged (dotted path ①) or discharged (dotted path ②) through D_1-C_x-G_4, D_{f4}-C_x-G_2 respectively according to voltage difference between C_2 and C_x.

3) Mode 2B

Current paths are shown in Fig. 5 (c). Output voltage $V_d/2$ is achieved through a current path C_2-C_1-G_1-C_x-D_{f3} and a bidirectional current path is formed through G_3-D_2-C_2 as shown by solid paths. If the capacitor C_x voltage is lower than the capacitor C_1 voltage, the capacitor C_x can be charged through C_1-G_1-C_x-D_2 shown by dotted path.

4) Mode 3

Current paths are shown in Fig. 5 (d). Output voltage is 0 and D_{f4}-D_{f3} forms a bidirectional current path as shown by solid paths. If the voltage of capacitor C_2 is higher than $V_d/2$, it will be discharged to the capacitor C_x as shown by dotted path.



(a) Current paths at mode 1 (b) Current paths at mode 2A

(c) Current paths at mode 2B (d) Current paths at mode 3

Fig. 5. Current paths at each switching mode.

From Fig. 5, we can see that the voltage of the capacitor C_x charged to the voltage $V_d/2$ at the beginning can be always kept to $V_d/2$ by charging or discharging action with C_1 and C_2. The effect of the capacitor C_x is as follows:

1) C_x serves as the blocking voltage of the inner devices at turn-off.
2) Bidirectional current is achieved through C_x.
3) DC-link voltage balance can be satisfied by C_x.

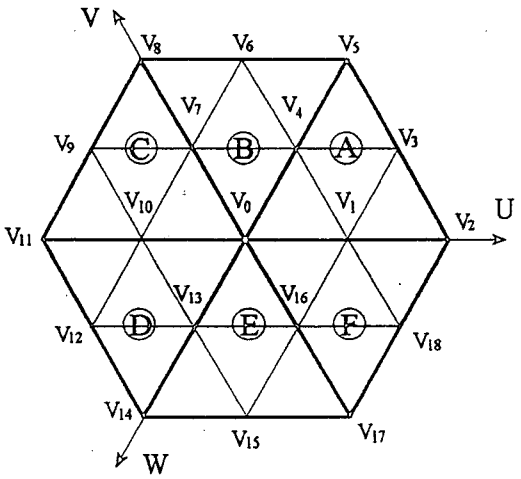
Essentially, the unbalance of the DC-link capacitor voltages is solved by charging or discharging capacitor C_x with capacitors C_1 and C_2.

2. PWM Method

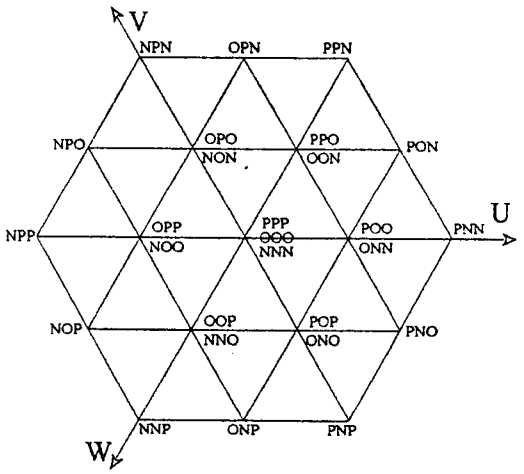
The space vector PWM technique is very useful for generating desirable output waveforms. If the three-level inverter is controlled by the space vector PWM technique, we can choose two alternative switching modes at the middle voltage vectors in order to control the average voltage of DC-link capacitors [4, 5, 8].

Fig. 6 (a) shows the space vector representation of the output voltages [4, 5], and Fig. 6 (b) shows switching states of each vector. Table Ⅲ shows the relation between the voltage vectors V_0 to V_5 and the switching states of each phase. There are three switching states for the zero voltage vector V_0 and two switching states for the middle voltage vectors corresponding to the apexes of the smaller hexagon (V_1, V_4, V_7, V_{10}, V_{13}, V_{16}) and one switching state for the

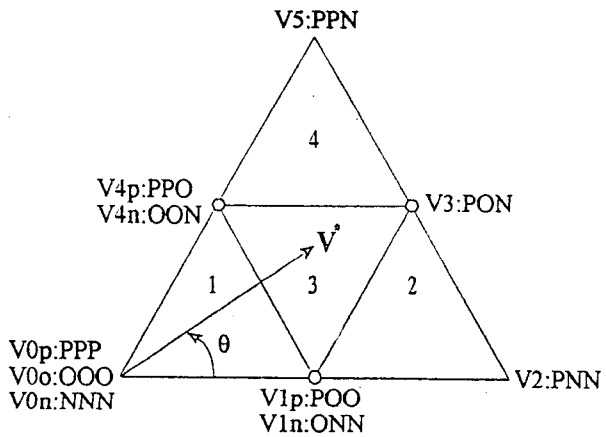
large voltage vectors (V_2, V_3, V_5, V_6, V_8, V_9, V_{11}, V_{12}, V_{14}, V_{15}, V_{17}, V_{18}). The middle voltage vectors control the neutral point DC voltage. The middle voltage vectors V_{xp} (x=1, 4, 7, 10, 13, 16) are concerned with charging or discharging of the upper DC capacitor C_1 in Fig. 4 (c). On the other hand, the voltage vectors V_{xn} (x=1, 4, 7, 10, 13, 16) are concerned with charging or discharging of the lower DC capacitor C_2.



(a) Space vector representation



(b) Space voltage vectors with their switching states



(c) Voltage vector: section A

Fig. 6. Space voltage vectors for a three-level inverter.

Fig. 6 (c) shows a triangle formed by the voltage vectors V_0, V_2 and V_5. This triangle can be divided into four smaller triangles 1, 2, 3 and 4. The apexes of these triangles correspond to the voltage vectors in Table Ⅲ.

Table 3. Switching States of the Voltage Vector V_0 to V_5
(( )=switching mode, y=A, B)

Voltage vectors		Phase U	Phase V	Phase W
V_0	V_{0n}	0	0	0
	V_{0o}	1/2(2y)	1/2(2y)	1/2(2y)
	V_{0p}	1	1	1
V_1	V_{1n}	1/2(2A)	0	0
	V_{1p}	1	1/2(2B)	1/2(2B)
V_2		1	0	0
V_3		1	1/2(2A)	0
V_4	V_{4n}	1/2(2A)	1/2(2A)	0
	V_{4p}	1	1	1/2(2B)
V_5		1	1	0

Referring to Fig. 6 (c), and using the space vector PWM technique, generally, three voltage vectors corresponding to the apexes of the triangle that includes the reference voltage vector are selected to minimize the harmonic components of output line-to-line voltage. The duration of these three voltage vectors is obtained as follows: for example, if the reference voltage vector V* falls into the triangle 3, the duration of the voltage vector V_1, V_3 and V_4 which correspond to the apexes of the triangle 3 can be calculated by the following equations (see Appendix A).

$$V_1 \cdot t_1 + V_3 \cdot t_3 + V_4 \cdot t_4 = V^* \cdot T \quad (1)$$

$$t_1 + t_3 + t_4 = T \quad (2)$$

$$V_1 = \frac{1}{2},\ V_3 = \frac{\sqrt{3}}{2} e^{j\frac{\pi}{6}},\ V_4 = \frac{1}{2} e^{j\frac{\pi}{3}},\ V^* = V \cdot e^{j\theta} \quad (3)$$

where, T = sampling time for reference voltage vector

The calculation results are as follows:

$$t_1 = T(1 - 2k\sin\theta)$$

$$t_3 = T[2k\sin(\theta + \tfrac{\pi}{3}) - 1] \quad (4)$$

$$t_4 = T[2k\sin(\theta - \tfrac{\pi}{3}) + 1]$$

where, $k = 2V/\sqrt{3}$: modulation amplitude

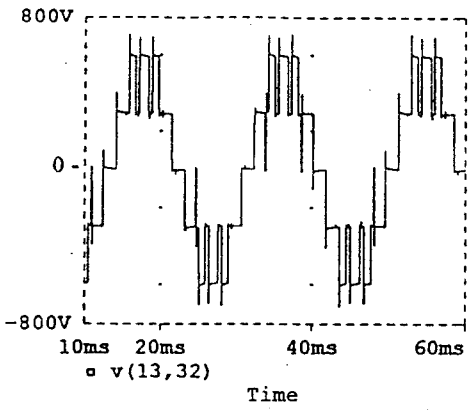
In the case of a conventional inverter, DC-link voltage unbalance caused by V_1, V_4 can be reduced only with the control of the duration of V_{1n}, V_{1p} and V_{4n}, V_{4p} respectively. However, in the new inverter topology, DC-link voltage balance can be satisfied by controlling Vcx (voltage of C_x), by modulating the durations of V_0, V_2, V_3 and V_5.

IV. Simulation and Experimental Results

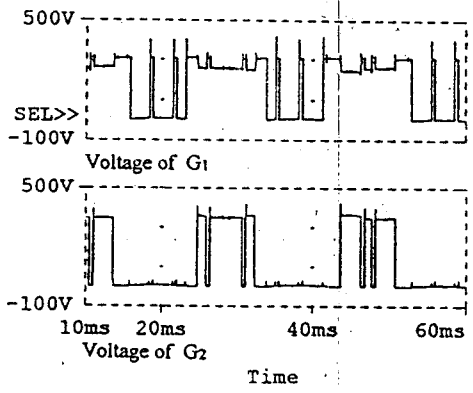
Fig. 7 shows Pspice simulation results of the conventional three-level inverter shown in Fig. 1 (c) with space vector PWM control and Table IV as the simulation conditions. Fig. 7 (a) is the output line-to-line voltage waveform, distorted due to the unbalanced voltage between capacitors. Fig. 7 (b) and (c) are blocking voltages across each switching device at turn-off. The blocking voltages across the outer devices G_1 and G_4 vary from about 245V to 310V excluding the overvoltage, and the voltages across the inner devices G_2 and G3 are about 365V which is about 18% higher than the expected value. This is proportional to the peak value of the overvoltage across the inner devices. Fig. 7 (d) is harmonic spectrum of the output line-to-line voltage.

Table 4. Simulation Conditions

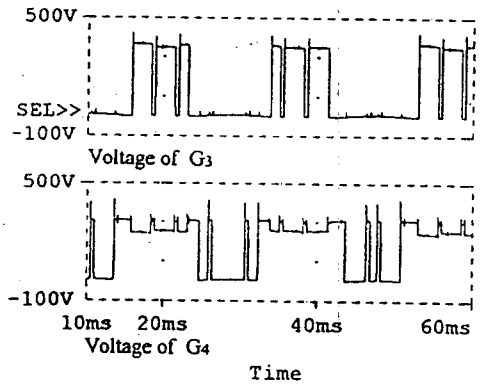
	Conventional	New
V_d	620V	620V
$V_d/2$	310V	310V
C1	4700μF	2200μF
C2	4700μF	2200μF
Cx(x=u, v, w)	-	2200μF
Load R	35.1Ω	35.1Ω
Load L	21.1mH	21.1mH
Each stray inductance (show Fig. 3)	1.5uH	1.5uH



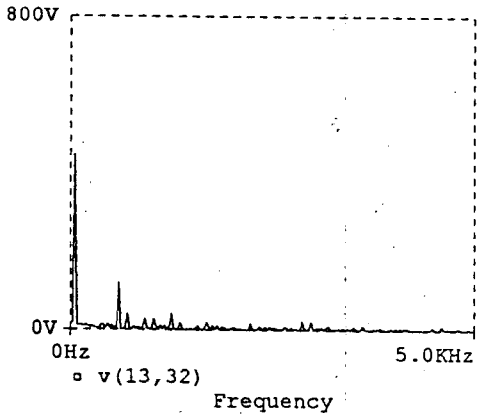
(a) Output Voltage



(b) Voltages of G_1 and G_2



(c) Voltages of G_3 and G_4



(d) Harmonic spectrum

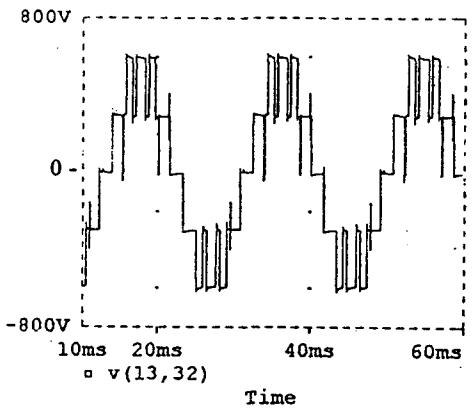
Fig. 7. Simulation results in case of a conventional three-level inverter. (a) Output line-to-line voltage. (b) Voltages across G_1 and G_2 at turn-off. (c) Voltages across G_3 and G_4 at turn-off. (d) Harmonic spectrum of output line-to-line voltage.

Fig. 8 is the simulation results of a new three-level inverter shown in Fig. 4 (c), with space vector PWM control. At each middle voltage vector, the switching states selected

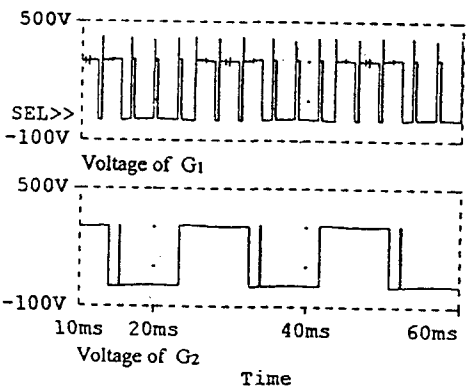
are listed in Table V. The distortion of output voltage and unbalance of the blocking voltage are greatly improved because the blocking voltages across the inner and the outer switches are much the same value of about 310V which is $V_d/2$.

Table 5. Switching States of Each Middle Voltage Vectors.

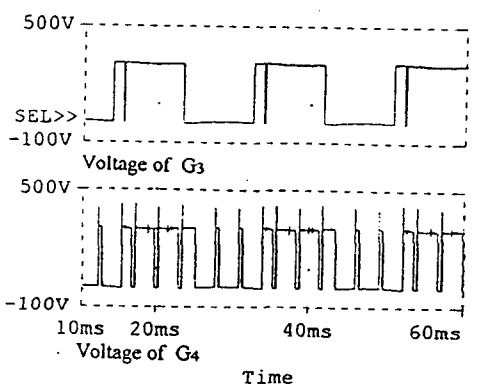
Middle voltage vectors	V_1	V_4	V_7	V_{10}	V_{13}	V_{16}
Selected switching states	V_{1n}	V_{4p}	V_{7n}	V_{10p}	V_{13n}	V_{16p}



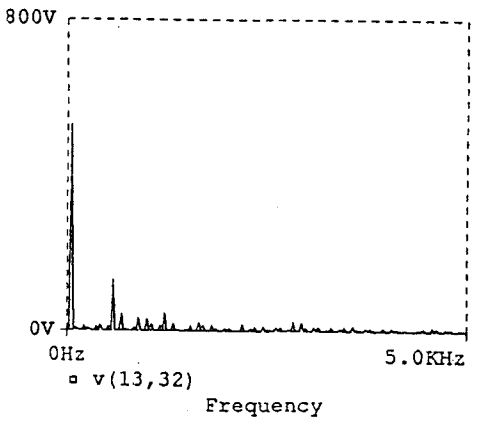
(a) Output Voltage



(b) Voltages of G_1 and G_2



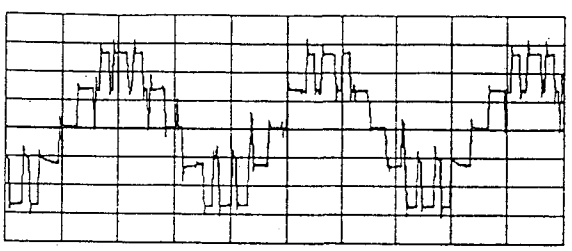
(c) Output Voltages of G_3 and G_4



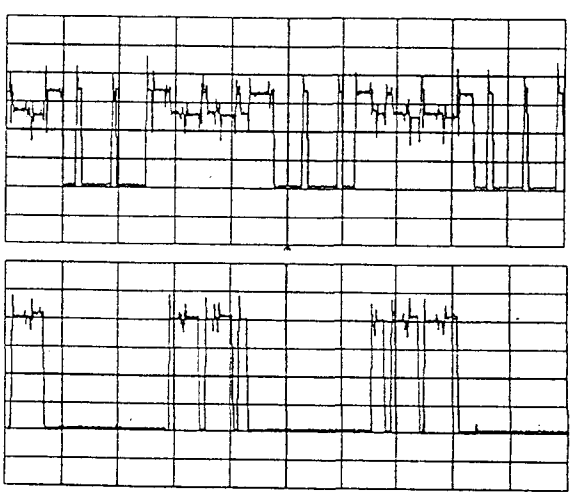
(d) Harmonic spectrum

Fig. 8. Simulation results in case of a new three-level inverter. (a) Output line-to-line voltage. (b) Voltages across G_1 and G_2 at turn-off. (c) Voltages across G_3 and G_4 at turn-off. (d) Harmonic spectrum of output line-to-line voltage.

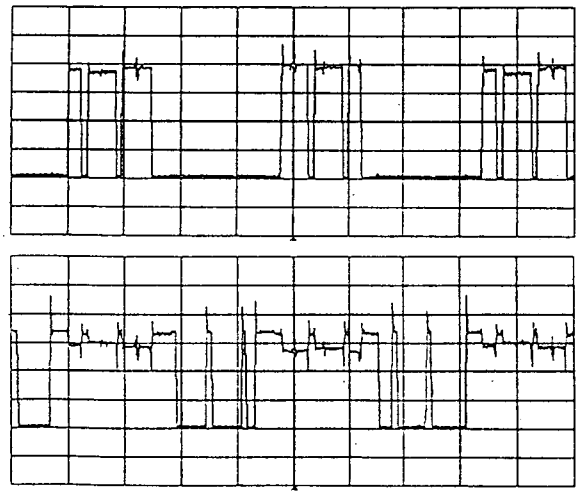
Fig. 9 and Fig. 10 are experimental results of the conventional and the new three-level inverter, respectively. In the case of the new three-level inverter, these results conform to those obtained by simulation.



(a)

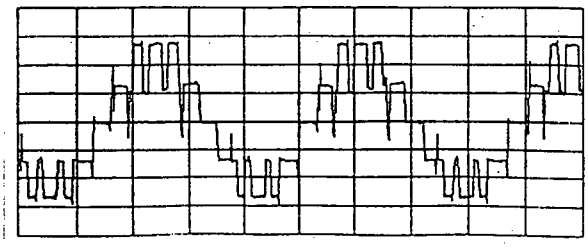


(b)

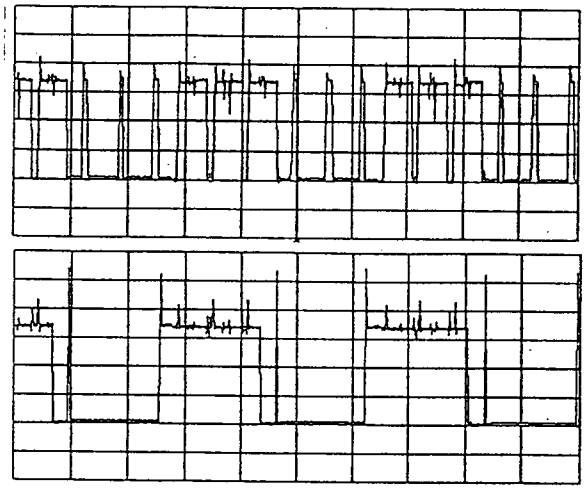


(c)

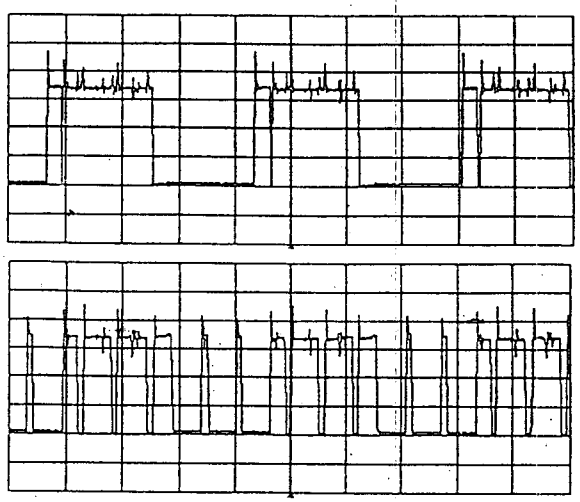
Fig. 9. Experimental results in case of a conventional three-level inverter(time 5ms/div). (a) Output line-to-line voltage(200V/div). (b) Voltages across G_1 and G_2 at turn-off (80V/div). (c) Voltages across G_3 and G_4 at turn-off(80V/div).



(a)



(b)



(c)

Fig. 10. Experimental results in case of a new three-level inverter (time 5ms/div). (a) Output line-to-line voltage(200V/div). (b) Voltages across G_1 and G_2 at turn-off (80V/div). (c) Voltages across G_3 and G_4 at turn-off(80V/div).

V. Conclusions

This paper demonstrates a multi-level high voltage inverter operating with a DC-link voltage of 4000V. It guarantees equal voltage sharing of series connected GTOs', hence harmonic components of the output voltage are less than those of conventional inverters at the same switching frequency; e. g. the inverters paralleled with a reactor.

A new multi-level PWM inverter topology is proposed and investigated. The analyzed new three-level inverter has advantages compared with the conventional three-level inverter as follows:

1) Reduced fluctuations of the neutral point DC voltage.
2) Maintenance of balanced blocking voltages across each device at turn-off.

Therefore, as shown in experiment, even without special measures to maintain the balance of the DC-link voltage, this voltage can be naturally achieved. In addition, the maintenance of operation with rated voltage and calculation of power dissipations due to the leakage current and the anode tail current can be done precisely, since the blocking voltages across the switches are always kept at $V_d/2$. Although voluminous capacitor bank C_x is added in realizing new multi-level system, reliability and performance of the inverter system can be improved. This topology, therefore, is expected to be effectively applied to high voltage GTO

inverters for high power AC drive systems.

Appendix A

THE DERIVATION OF EQUATIONS 1, 2, 3, AND 4 [see Fig. 6 (c)]

If vector V_2 is set to reference axis and its magnitude is set to unity, each space voltage vector and the reference voltage vector can be expressed by the exponential form as follows:

$$V_1 = \frac{1}{2} \tag{A1}$$

$$V_3 = \frac{\sqrt{3}}{2} e^{j\frac{\pi}{6}} \tag{A2}$$

$$V_4 = \frac{1}{2} e^{j\frac{\pi}{3}} \tag{A3}$$

$$V^* = V \cdot e^{j\theta} \tag{A4}$$

Next, the following two equations should be satisfied as space vector PWM for the two-level inverter.

$$V_1 \cdot t_1 + V_3 \cdot t_3 + V_4 \cdot t_4 = V^* \cdot T \tag{A5}$$

$$t_1 + t_3 + t_4 = T \tag{A6}$$

where, T = sampling time for the reference vector

Substituting (A1-A4) for (A5) and changing (A5) to trigonometric form,

$$\frac{1}{2} t_1 + \frac{\sqrt{3}}{2}(\cos\frac{\pi}{6} + j\sin\frac{\pi}{6}) \cdot t_3 + \frac{1}{2}(\cos\frac{\pi}{3} + j\sin\frac{\pi}{3}) \cdot t_4 = V(\cos\theta + j\sin\theta) \cdot T \tag{A7}$$

Separating real part and imaginary part from (A7),

$$\frac{1}{2} t_1 + \frac{\sqrt{3}}{2}(\cos\frac{\pi}{6}) \cdot t_3 + \frac{1}{2}(\cos\frac{\pi}{3}) \cdot t_4 = V(\cos\theta) \cdot T \tag{A8}$$

$$\frac{\sqrt{3}}{2}(\sin\frac{\pi}{6}) \cdot t_3 + \frac{1}{2}(\sin\frac{\pi}{3}) \cdot t_4 = V(\sin\theta) \cdot T \tag{A9}$$

From (A6), (A8), and (A9), t_1, t_3 and t_4 can be calculated and the results are as follows:

$$t_1 = T(1 - 2k\sin\theta) \tag{A10}$$

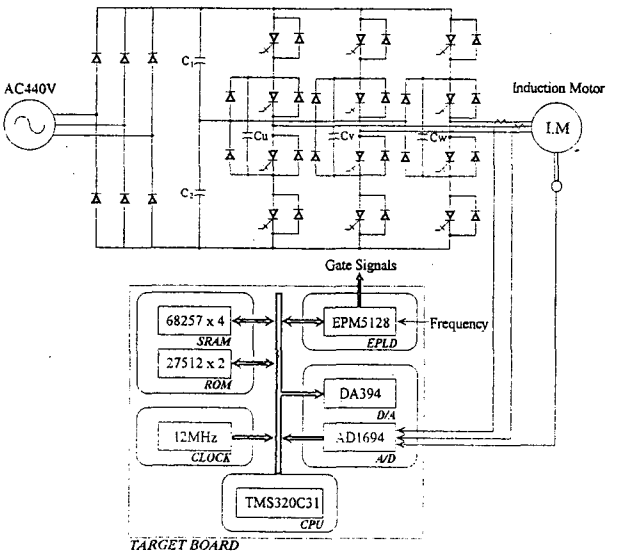
$$t_3 = T[2k\sin(\theta + \frac{\pi}{3}) - 1] \tag{A11}$$

$$t_4 = T[2k\sin(\theta - \frac{\pi}{3}) + 1] \tag{A12}$$

In other regions(1, 2, 4), the durations of each voltage vector can be calculated in the same way. And also, in other sections (B, C, D, E and F), vectors V_5, V_8, V_{11}, V_{14} and V_{17} are set to reference axes.

Appendix B

ACTUAL THREE-LEVEL INVERTER SCHEMATIC



EXPERIMENT CONDITIONS

	Conventional	New
Input	440Vac	440Vac
C_1	4700μF	2200μF
C_2	4700μF	2200μF
Cx(x=u, v, w)	-	2200μF
Induction Motor	440V-5.5kW	440V-5.5kW
Output Frequency	0-60Hz	0-60Hz

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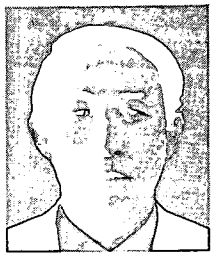
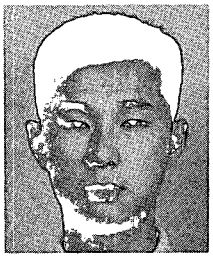
Yo-Han Lee was born in Seoul, Korea, in 1970. He received the B.S. and M.S. degree in electrical engineering from Hanyang University, Seoul, Korea, in 1993 and 1995, respectively. He is working toward the Ph.D. degree in electrical engineering at the same university in the area of power electronics. His research interests are in static power converters, their control and adjustable speed ac drives.



Dong-Seok Hyun received the B.E. and M.E. degrees in electrical engineering from Hanyang University, Seoul, Korea, in 1973 and 1978, respectively, and the Ph.D. Degree in electrical engineering from Seoul National University, Seoul, Korea, in 1986. From 1976 to 1979, he was with Agency of Defense Development, Korea, as Researcher. He was a Research Associate in the Department of Electrical Engineering at the University of Toledo during 1984 - 1985, and a visiting Professor in Electrical Engineering at Technical University Munich during 1988 - 1989. Since 1979, he has been at Hanyang University, where he is now a Professor in the Department of Electrical Engineering and Director of the Advanced Institute of Electrical Engineering and Electronics(AIEE). Prof. Hyun is the author of more than 70 publications in electric machine design, high power engineering, power electronics, and motor drives. His research interest include power electronics, motor drives, digital signal processing, tractions, and their control system. He is a member of the KIEE, the IEE, and the IEEE(PES, IAS, CSS, EDS).



Bum-Seok Suh was born in Seoul, Korea, in October 1966. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from Hanyang University, Seoul, Korea, in 1989, 1991 and 1996, respectively. Since 1991, he has been with the Research Institute of Industrial Sciences at Hanyang University, where he is engaged as a researcher. His main research interests are modeling and application of power semiconductor devices, static power conversion systems for high power induction motor drive, power converter topologies for high frequency inverter systems, and power electroncis.