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USEFUL REDUNDANT TECHNIQUES FOR BUILT-IN-TEST RELATED SYSTEM*

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Abstract

This research paper describes several possible suggestions which are essential to develop for Built-In-Test(BIT) related systems, such as more precise BIT parameter analysis, sensitivity analysis of the impact of BIT on redundant systems, statistical inference of field data for BIT performance parameters, methods of reducing BIT false alarms, BIT application in industrial automation and remote control, prevent the system from the impact of BIT failure, undetections and false alarms, life cycle cost analysis for BIT. And, it is mainly focused on redundancy technique for solving BIT diagnostic problems. Algorithms for redundant systems: overlapping technique, flexible redundant BITs are presented and case study will be shown based on various experiment.

1. Introduction

1.1 General Concept and Assumption of BIT

The term "Built-In-Test" refers to a subsystem whose major purpose is to test the operating state of the primary system. Briefly, BIT is the hardware and software that are integrated into a system to perform fault detection, diagnosis and isolation, and failure recording, along with possible reconfiguration or failure management[15].

BIT has attractive advantages, but some shortcomings as well. Today's technology cannot assure a perfect BIT. In fact, the improvements in BIT over the last decade and

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a half have, to a great extent, been canceled out by the increasing complexity of systems.

In addition, BIT is disastrously inefficient when applied to a high-reliability system; the high false alarm probability harasses maintenance personnel and designers a great deal.[30]

1.2 Purpose and Scope of the Research

As an important automatic testing equipment and a kind of controller, BIT has found wide application in aviation and space technology, electronics and other commercial and military systems as well.

A number of research papers have been published [1-11,13,14,16-25,28,29,30] and the basic concepts and analysis approaches have been defined. However, there are still many problems with BIT performance, application in commercial systems, false alarms, standards and specifications, cost-benefit analysis, design parameter analysis, etc.

This paper discusses some of the essential tasks to develop for BIT related systems in brief. We present the problems, the possible research methods and the conditions we need. It is helpful to decide the direction for our research in the area of BIT technique.

One of the momentous interests is the method of preventing the system from the impact of BIT mistakes in this paper. Several original approaches which are applied to BIT related systems will describe in order of significance and system effectiveness. A systematic and integrated approach on redundancy technique for BIT(: such as overlapping BIT technique and flexible redundant BITs) will also describe with results of various experiment.

2. Essential Tasks to Develop for BIT Related Systems

2.1 More Precise BIT Parameter Analysis

Lamberson & Shao, and Bozic & Shaw, have developed approaches to analyze BIT performance parameters and the impact of them on systems RAM(Reliability, Availability, Maintainability)[2,15,26]. These approaches mainly are for early design phase and for a new system for which there are little field data available. Consequently, these methods are approximate ones.

However, during production and operation phases, we need more precise prediction and estimation for BIT systems. And it is possible if the field data of a similar system are available or the real field data of the system are obtained.

In this case, we improve or extend the BIT parameter analysis approaches presented in the literature as follows :

(1) Propose more consistent definitions for fault detection and fault isolation probabilities (F_d and F_i) respectively. In[26], Shao and Lamberson defined F_d and F_i as either of two Boolean values, "Yes" or "No", for each failure mode, while in fact, BIT has a certain detection and isolation probabilities for every failure mode. Hence a more reasonable definition is possible.

(2) Considering and excluding the non-relevant circuits, parts, and part failure modes from the fault detection analysis, one can obtain more accurate results of the fault detection predictions for a system's Built-In-Test design [22].

(3) When a Line Replaceable Unit(LRU) is down with different failure modes the repair requirements should be different.

(4) Intermittent and Instantaneous failures have not been considered.

(5) To match more precise BIT parameter analysis, we treat BIT operation as a stochastic model, hence Markov process method can be applied as a mathematical tool.

(6) So far, the math models for BIT are good for only sensitivity analysis, it is attractive to improve existent analysis approach such that quantitatively calculating the impact of BIT on systems RAM becomes possible.

To do these tasks, we need the updated military standards about Built-In-Test, Testability, Automatic fault diagnosis and some real field data to demonstrate the new math models to be developed.

2.2 Sensitivity Analysis of the Impact of BIT on Various Redundant Systems

When BIT is incorporated to redundant systems, it plays a very active role. BIT will not only monitor the system, detect and diagnose a fault, but also control and manage the redundancy. Particularly, BIT false alarms will cause a rejection of a good unit and useless maintenance activities. Hence the impact of BIT on redundant systems is very complicated. In addition, a false alarm is an active factor, it happens randomly.

Lamberson & Shao have developed comprehensive Markov models for various redundant systems with BIT[15,26]. The logical further work would be programming the math models, and make sensitivity analysis. We can input some typical data combinations(real field data are preferable) and get corresponding reliability, maintainability and availability results of cold-standby, k-out-of-n, majority voting and shared load systems.

The algorithms would be very applicable for engineers, designers and reliability analysts of redundant systems. In addition, this is a good way to validate and refine upon the math models if necessary. It can also be extended as a commercial software package because we have not seen a satisfied math model which represents a redundant system considering both undetection and false detection.

2.3 Statistical Inference for BIT Performance Parameters Using BIT Field Data

Most of the literature only uses assumed data. The today's practical varying ranges for BIT performance parameters are not definite. In existent contracts, both too high and lower requirements are not unusual [10]. And basic BIT parameter standards are not well developed. Moreover, the approach to handle BIT

field data is not available because the behavior of some BIT performance is different from general failure modes.

If we can get enough field data of BIT, it is valuable to develop a method to deal with the field data of BIT, and to make some statistical inference. Likely it will be helpful to establish or improve the standards for BIT performance parameters if these standards are not available or not complete.

The field data of BIT should be collected by customers with strict maintenance data base systems. If possible, U.S. Navy's 3M system or U.S. Airforce's maintenance data system are preferable. It is also acceptable if an avionics supplier or an electronics company can transfer the strict field data of BIT from their customer's maintenance data base.

2.4 Methods of Reducing BIT False Alarms

Considerable attention has been focused to BIT false alarms, which cause series problems, such as decrement of mission reliability, great amount of waste with manpower, time and resources. There are several ways to reduce BIT false alarms.

(1) More complete FMECA and FTA to find out as many failure modes as possible, and more reasonable specifications for the threshold values of BIT.

(2) Fully utilize the prior failure data to improve or modify the Built-In-Testing result. A Bayesian analysis technique is able to be applied in diagnostics. We derived some math models and develop an applied comprehensive Bayesian method to estimate BIT performance parameters and the reliability of a system with BIT[27,30].

(3) Appropriate BIT redundancy and more reasonable testing logic are a practical method as well. Shao and Lamberson has introduced some schemes[26].

(4) The ultimate and complete approach is self-adapting diagnosis based on Artificial Intelligence(AI), which will enable us to obtain ideal BIT equipment-so called Smart BIT[25].

2.5 BIT Application in Commercial Systems

Nowadays, commercial systems are becoming increasingly more complex and automatic self-testing and maintainability are becoming more and more important and necessary.

BIT, which actually is an intelligent self-testing device, has been not only applied in sophisticated military systems, but also appears in many commercial systems, such as computer networks, electronic and electric equipment, airliners, automobiles, machine tools, and so on.

Automobiles now have some crude diagnostics incorporated into their on-board microcomputers, such as digital indication for speed, fuel, door lock status, cooling water and transmission oil temperatures.

Future automobiles will become an all computer action vehicle. There will be no mechanical linkage between the driver and the

fuel management system and brake system. Only action completed by a driver probably is to press some buttons, then a computer-based controller will take care of whole the driving process from starting the engine, acceleration, keep an optimal speed, deceleration and stop.

Technique evolution will see even totally blind driving that is very helpful in dark night, heavy fog and severe storm. An on-board radar system will detect the target in front of the vehicle and avoid crashing. It is also possible to recognize traffic signals with a TV system, then the controller takes reactions.

For this advanced all computer action vehicle, real-time self-testing system is absolutely necessary. Without BIT, a failure of this automatic vehicle will cause serious problem, even a catastrophe. Also BIT is necessary for maintenance as manual testing and diagnosing a modern sophisticated system becomes very difficult and time-consuming.

Therefore, BIT will play two important roles in commercial systems, one role is monitoring and testing the system health status, detecting faults, diagnosing and isolating the faults to a component and record all of the fault information, the other role is rapidly testing the system for maintenance and repair.

Lamberson & Shao[15] have presented how to systematically apply the BIT technique to commercial systems, such as to configurate a BIT system(a network) which composed of sensors, processors, data base, maintenance and monitoring panel and display, to analyze the effect of BIT performance parameters on the commercial system, to trade-off the advantages and shortages of BIT.

2.6 Prevent a System from the Impact of BIT Undetection, False Detection and the Failure of BIT Itself

It is an interesting task because nobody can assure BIT does not have fault. In the case that BIT made a mistake, what can we do to protect the primary system, to avoid mission abortion and to avoid waste of time and resources for useless maintenance?

In order to improve system reliability and maintainability. We have to develop some BIT design approaches that can compensate for BIT mistakes and hardware failure such that a system can continue full of partial operation.

The following approaches are possible :

(1) Overlapping BIT technique

Assign two different BITs for each of important subsystems like Figure 1. Only when two different BITs indicate a same failure, the failure will be diagnosed and isolated. Otherwise, no responses will be taken.

(2) Flexible redundant BITs

Suppose the subsystem to be tested by a BIT is very important. Very high detection probability and very low false alarm probability are required. Here, three different BITs are used to detect a subsystem fault. BIT-1 is designed for regular purposes; BIT-2 is specially designed for reducing the non-detection proba-

bility, while BIT-3 is specially designed for reducing the false alarm probability.

(3) BIT condition assessment technique

Developing a special software to self-test the BIT system cyclically during the mission. Fault insertion is simulated by the software and the self-test result will be indicated on the display. For off-line maintenance, a real fault injection applies when a BIT fault is found, this BIT must be disconnected with the primary system.

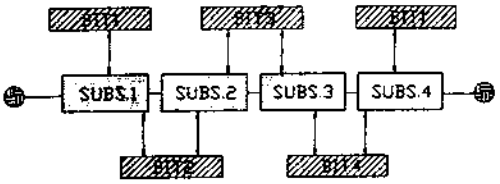

Figure 1. General Case of the Overlapping BIT Structure

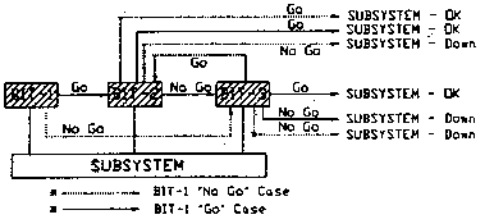

Figure 2. General Case of the Flexible Redundant BIT

(4) Not responding to a diagnostic mistake

The system should be designed such that if the self-test recognizes a BIT fault, the system will not response to the failure indication issued by that BIT.

(5) BIT indication analyzer

A predetermined logic is used to create a BIT indication analyzer which refuses unreasonable BIT test results and tracks and switches out the failed BIT. For instance, if a BIT indicates all of the parallel units are failed simultaneously, the BIT itself is likely broken. If a BIT monitors system's output or other performance parameters, since the expected range of value are known in advance, a large deviation from the expected value usually represents a malfunction of the BIT itself.

2.7 Life Cycle Cost Analysis for Built-In-Test

Life Cycle Cost(LCC) analysis is a well-known concept for system's cost-benefit analysis. When BIT is incorporated into a repairable primary system, certain aspects of LCC are involved with BIT. And actually BIT technique will much affect the LCC of the total system. However, very little work can be found in the open literature[16,23].

Investigation for BIT Life Cycle Cost is very important for BIT conception definition. Generally speaking, the costs of BIT during the total life include: BIT research and development cost, BIT acquisition cost, logistic support cost for BIT, the maintenance cost with BIT versus without BIT and the effect of BIT on system operation readiness and the total number of the products to be purchased. A great deal of maintenance data and cost data which are referred to BIT are needed to realize the BIT LCC analysis.

3. Redundancy Technique for BIT

Redundancy is a popular technique in system reliability design. When a single BIT cannot satisfy the diagnosis requirements, the redundancy technique is also helpful. In this subsection, two kinds of distinct redundant structures are introduced. There are obviously many other possible redundant configurations which could be considered in or on the BIT related systems. The BIT diagnosis parameter definitions and notations used in this paper, are shown in Table 1.

3.1 Overlapping Technique for BIT

In Figure 1., a system under test is partitioned into several subsystems. A family of BIT units tests the system. Each BIT is attached to two subsystems, while each subsystem is subjected to testing by two pieces of BIT equipment whose circuits and softwares are different. The results given by two overlapped BITs will be shown on the display upon request, so that the operator has the option to intervene in the system.

When an overlapping BIT is applied to an automatic control system or a self-reconfiguration system, no response will be made unless two different BITs report the same failure. In other words, as long as one BIT gives a negative result, the system will be considered as functioning. However, a pair of BITs that have issued different test results may be further tested to determine (a) which BIT made a mistake, and (b) whether the faulty BIT must be turned off.

The overlapping BIT technique is much different from the Bayesian processor[30], which statistically analyzes multi-test results performed by the same BIT. When the primary system is very important and the Bayesian processor does not work well, the overlapping BIT technique is a good alternative and it is very capable of reducing false alarms.

Let us consider a numerical case study, as follows.

〈Case study of the Overlapping BIT technique〉

Assuming the reliability function for subsystems 1, 2, 3, 4 and BITs 1, 2, 3, 4 are $R_{1(t)}$, $R_{2(t)}$, $R_{3(t)}$, $R_{4(t)}$, $R_{B1}(t)$, $R_{B2}(t)$, $R_{B3}(t)$ and $R_{B4}(t)$, respectively, and the false alarm rates for BITs 1, 2, 3, 4 are λ_{FA1}, λ_{FA2}, λ_{FA3}, and λ_{FA4} respectively, it is desired to estimate the false alarm probability for both non-overlapping and overlapping BIT systems.

Consider that the primary system is a series system. For the non-overlapping case, BIT i tests subsystem i, where $i=1, 2, 3, 4$. Then the probability that a false alarm will occur for this system is

$$P_1 = \prod_{i=1}^{4} R_i(t) \cdot R_{Bi}(t) \cdot \left\{ 1 - e^{-\sum_{i=1}^{4} \lambda_{FAi} t} \right\} \quad (1)$$

Now let us derive the formulas for calculating the probability that a false alarm will occur for the corresponding system with the overlap-

Table 1. BIT Diagnosis Parameter Notations and Definitions

NOTATION	TERM	DEFINITION
F_a	Probability of the BIT Fault Detection	The probability that BIT will detect an existing functional failure in the system.
F_t	Probability of the BIT Fault Isolation	The probability that BIT will isolate a failure that has been detected by BIT down to the specified level(usually a single LRU).
λ_{FA}	BIT False Alarm Rate	The rate at which the BIT issues false alarms in a certain time interval for the BIT surviving at the start of the interval.
$F_B=1-R_B(t)$	Probability of the BIT Failure	The probability that BIT will physically fail when there is system functioning.
λ_B	BIT Essential Failure Rate	The rate at which BIT physical failures occur in a certain time interval for the BIT surviving at the start of the interval.
F_a	Probability of the BIT False Alarm	The probability that BIT will indicate a failure when there is no actual system malfunction.

〈Reference to Notation F_a〉

$$F_a = \frac{\Pr(\textit{False Alarm and No System Failure})}{\Pr(\textit{Detect True Failures}) + \Pr(\textit{false Alarm and No System Failure})}$$

ping BIT configuration shown in Figure 1.

Denote the event that BIT i issues a false alarm by i. The complement events are denoted by $\bar{i}$. From Figure 1., We can list the following cases where no false alarms occur :

$$\bar{1}\bar{2}\bar{3}\bar{4},\ \bar{1}\bar{2}\bar{3}4,\ \bar{1}\bar{2}34,1\ \bar{1}2\bar{3}\bar{4},\ \bar{1}2\bar{3}4,$$
$$1\bar{2}\bar{3}\bar{4}\ \text{ and }\ 1\bar{2}34$$

T he no-false-alarm probability $\overline{F_a}$ will be the summation of the probabilities of the above seven cases. We treat events $\bar{i}$ and $\bar{i}$ also as the probability of the events $P(i)$ and $P(\bar{i})$ for short ; then $\overline{F_a}$ can be expressed as

$$\begin{aligned}\overline{F_a}a &= \bar{1}\{\bar{2}\bar{3}\bar{4}+\bar{2}3\bar{4}+2\bar{3}\bar{4}\}+2\bar{3}4\\ &\quad +1\bar{2}\bar{4}\{\bar{3}+3\}\\ &= \bar{1}\{\bar{3}\bar{4}+\bar{3}4+\bar{2}3\bar{4}\}+1\bar{2}\bar{4}\\ &= \bar{1}\{\bar{3}+\bar{2}34\}+1\bar{2}\bar{4}\end{aligned} \qquad (2)$$

Substituting $P(i)=1-e^{-\lambda_{FAi}t}$ and $P(\bar{i})=e^{-\lambda_{FAi}t}$ into (2), after reorganizing, we have

$$\begin{aligned}\overline{F_a} &= e^{-\lambda_{FA1}t}\cdot\{e^{-(\lambda_{FA2}+\lambda_{FA4})t}\cdot(1-e^{-\lambda_{FA3}t})+e^{-\lambda_{FA3}t}\}\\ &\quad +e^{-(\lambda_{FA2}+\lambda_{FA4})t}\cdot(1-e^{-\lambda_{FA1}t})\end{aligned} \qquad (3)$$

The probability that a false alarm will occur in the system with an overlapping BIT will be

$$P_2=\prod_{i=1}^{4} R_i(t)\cdot R_{Bi}(t)\cdot[1-\overline{F_a}] \qquad (4)$$

Therefore, we can formulate the Ratio between the probability that a false alarm will occur without an overlapping BIT ($P_{1)}$ and the probability that a false alarm will occur with an overlapping BIT P_2 which can denoted

by R_{OB}.

$$R_{OB}=\frac{P_2}{P_1}=\frac{[1-\overline{F_a}]}{\left[1-e^{-\sum_{i=1}^{4}\lambda_{FAi}t}\right]} \quad (5)$$

Assuming $\lambda_{FAi}=\lambda_{FA}$, $i=1,2,3,4$, then

$$R_{OB}=\frac{P_2}{P_1}=\frac{1-2e^{-2\lambda_{FA}t}+e^{-4\lambda_{FA}t}}{1-e^{-4\lambda_{FA}t}} \quad (6)$$

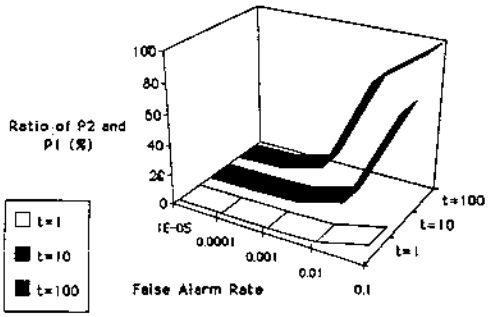

Table 2. Graphic Results of the Numerical Experiment on Overlapping BIT

From Table 2, we see that the false alarm probability of a system with a non-overlapping BIT is greatly reduced by using the overlapping BIT technique.

3.2 Flexible Redundant BITs

The strategy of the Flexible redundant BITs shown in Figure 2. Suppose the subsystem to be tested by a BIT is very important. Very high detection probability and very low false alarm probability are required. Here, three different BITs are used to detect a subsystem fault. BIT-1 is designed for regular purposes; BIT-2 is specially designed for reducing the non-detection probability, while BIT-3 is specially designed for reducing the false alarm probability.

The concept is that BIT-1 has moderate detection and false alarm probabilities, while BIT-2 should have a very high detection probability and BIT-3 should have a very low false alarm probability. BIT-1 tests the subsystem first. If the result is "GO", we may still worry about undetection, so we use BIT-2 to test the system sequentially. If BIT-2 says "GO" too, the system is "OK" ; otherwise, if BIT-2 says "NO GO", BIT-3 tests the subsystem again and the final result will be that of BIT-3. If BIT-1 says "NO GO", we should pay attention to false alarms, so BIT-3 takes its turn to test the subsystem.

If BIT-3 also gets a positive result, the system is down ; otherwise, if BIT-3 gives "GO", BIT-2 will be called to test the subsystem again and BIT-2 has the last word.

〈Case study of the Flexible Redundant BIT technique〉

Let us demonstrate this redundant strategy. The parameters for three BITs are shown in Table 3 :

Table 3. Numerical Example of Parameters for the Flexible Redundant BIT Structure

	F_d	F_a	Content
BIT-1	.980	.10	Moderate BIT
BIT-2	.995	.25	High Detection BIT
BIT-3	.900	.02	Low False Alarm BIT

Calculate the final detection and false alarm

probabilities of the Flexible redundant BIT structure.

〈Case 1〉 Assume that the primary system is at fault

There are three situations in which the Flexible redundant BIT-structure does not detect the fault :

1) BIT-1 and BIT-2 result in "GO" ; then the probability is $P^1_{S1}=.0001$

2) BIT-1 says "GO", BIT-2 gets "NO GO", and BIT-3 gives "GO" ; then the probability is $P^1_{S2}=.00199$

3) BIT-1 gets "NO GO", BIT-3 and BIT-2 both say "GO" ; the probability is $P^1_{S3}=.00049$

Therefore, the final undetection probability is

$$(1-F_d)=\sum_{i=1}^{3}P^1_{Si}=.00258.$$

The detection probability is $F_d=.99742$

〈Case 2〉 Assume that the primary system is fault-free

There are three situations in which the Flexible redundant BIT issues a false alarm :

1) BIT-1 says "NO GO" and BIT-3 says "NO GO" also. The probability is $P^2_{S1}=.002$

2) BIT-1 says "NO GO", BIT-3 says "GO", and BIT-2 says "NO GO". The probability is $P^2_{S2}=.0245$

3) BIT-1 says "GO", BIT-2 says "NO GO", and BIT-3 says "NO GO". The probability is $P^2_{S3}=.0045$

Therefore, the final false alarm probability will be

$$F_a=\sum_{i=1}^{3}P^2_{Si}=.031.$$

It is easy to conclude that the false alarm probability $F_a=.031$ is much lower than for BIT-1, while detection probability $F_d=.99742$ is higher than for any single BIT. Hence, the Flexible redundant BIT improves both false alarm probability and detection probability.

4. Conclusion and Further Topics

The term "Built-in-test" refers to the subsystem whose major purpose is to test the health status of the primary system. It is clear that BIT has played an important role in the process of improving the testability, maintainability and availability of the sophisticated systems. Also, BIT can take part in monitoring and managing various redundant systems such as standby, majority voting and k-out-of-n:G systems, degradable systems and reconfigurable systems. In addition, BIT can also indicate impending failures of the system. Therefore, BIT increases system operational reliability. This paper shows that two proposed Redundancy technique such as Overlapping and Flexible BIT are greatly improve both false alarm and detection probability and various possible suggestions for BIT related technology are

presented. As an advanced testing technique, BIT will become more and more important and useful in the system engineers. In our mid-term report for this research [30], Bayesian processor are presented to compensate BIT diagnostic problems. We need more study on that with redundant BIT techniques such as : (1) Determining the Prior odds effectively and expressing the Likelihood ratios by various ways (2) Expected value of the probability of failure after the number of test (3) The transparent status of the primary system while testing, etc.

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