Preparation of ECR MOCVD $SrTiO_3$ thin films and their application to a Gbit-scale DRAM stacked capacitor structure

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Abstract

It is commonly believed that high permittivity materials will be necessary for future high density Gbit DRAMs. In a first part, we explain the choice of $SrTiO_3$ by ECR MOCVD for Gbit-scale DRAMs. In a second part, after describing the ECR MOCVD system and presenting the requirements $SrTiO_3$ thin films should meet for use in Gbit-scale DRAMs, the physical and electrical properties of $SrTiO_3$ thin film prepared by ECR MOCVD are then studied. A stacked capacitor technology, suitable for use in 1 Gbit DRAM, and comprising high permittivity $SrTiO_3$ thin films prepared by ECR MOCVD at 450 °C on electron beam and RIE patterned RuO_2/TiN storage nodes is finally described.

Introduction: Why $SrTiO_3$ by ECR MOCVD for Gbit DRAMs ?

For future high density Gbit-scale DRAMs, new capacitor dielectrics with a high permittivity will be necessary, in order to reach the required charge storage density of 30 fF/cell. Several materials such as Ta_2O_5 (ε_r = 20-25) and ferroelectric materials (ε_r = 100-1500) have been envisioned to replace Si_3N_4-based capacitor dielectrics (ONO and ON), presently used in 16 Mbit and 64 Mbit DRAMs. Among the great variety of existing ferroelectric materials, paraelectric $SrTiO_3$ and $(Ba,Sr)TiO_3$, with characteristic features such as a high permittivity at high frequency (a few GHz), good chemical and thermal stability and good insulating properties, are often considered the most suitable capacitor dielectrics for the successful fabrication of high density Gbit-scale DRAMs [1-6]. When deposited in thin layers of 500-1000 Å, $SrTiO_3$ and $(Ba,Sr)TiO_3$ exhibit dielectric constants in the 150-500 range [1-10]. The predicted design rule for the storage node of 1 Gbit DRAMs is 0.2 μm or less [5,11]. This means that using a diagonal bit line configuration (DBL) [11], the electrode top surface would be 0.08 μm^2, and that for a storage node height of 0.5 μm, the electrode sidewall surface would be 0.6 μm^2. Therefore, in Gbit DRAMs, these materials are expected to be used in conjunction with a stacked capacitor structure, the sidewall capacitance largely contributing to meet the charge storage requirement of 30 fF/cell [6-7]. Recently, a new RuO_2/TiN multi-layered electrode structure was proposed for use as the storage node of Gbit-scale DRAMs [6]. With a stacked structure and a design rule of 0.2 μm or less for the storage node of Gbit DRAMs, metalorganic chemical vapor deposition (MOCVD) only will allow the preparation of $SrTiO_3$ and $(Ba,Sr)TiO_3$ films with a good step coverage over high aspect ratio features. Moreover, the use of a high density and damage-free low energy plasma, such as an electron cyclotron resonance (ECR) plasma allows low temperature deposition of crystallized films with the suitable leakage and capacitance properties for use in Gbit DRAMs [8]. Low temperature deposition is important to prevent degradation of the lower electrode/barrier layer structure, which can occur at elevated temperatures by diffusion through the barrier layer and/or reaction between the materials constituting the bottom electrode structure. In this paper, after giving some insight on the preparation of $SrTiO_3$ thin films by ECR MOCVD, a new stacked capacitor technology, suitable for use in 1 Gbit DRAM, and comprising low temperature ECR MOCVD $SrTiO_3$ over RIE patterned RuO_2/TiN storage nodes will be presented.

ECR MOCVD of $SrTiO_3$ Thin Films

CVD System

A schematic representation of the ECR MOCVD system is shown in Figure 1. Using this apparatus, $SrTiO_3$ films can either be deposited by thermal CVD or by ECR CVD [5,8,9,12]. In this paper, the discussion will only concern $SrTiO_3$ films prepared by ECR-MOCVD. $SrTiO_3$ films were deposited on 4-inch Si, $Pt/TaO_x/Si$ and $RuO_2/TiN/SiO_2/Si$ substrates using titanium isopropoxide (TIP) $Ti(i\text{-}OC_3H_7)_4$, strontium bis-dipivaloylmethanate $Sr(DPM)_2$ and an O_2 ECR plasma. The TIP bottle was maintained at 35 °C, and the $Sr(DPM)_2$ powder was heated at 210 °C. Argon was used as the carrier gas to transport the metalorganic vapors, and the gas lines between the source bottles and the reaction chamber were maintained at 220 °C in an isothermal tank. TIP and $Sr(DPM)_2$ were mixed just before injection into the reaction chamber, and an oxygen ECR plasma was generated above substrates as shown in Figure 1. The argon flow rates through the TIP and $Sr(DPM)_2$ bottles were 70 sccm and 70-280 sccm, respectively, and the O_2 flow rate was 420 sccm. Sr/Ti composition was adjusted by varying the pressure in the TIP bottle, using a control valve in the gas line just after the TIP bottle. The plasma power was maintained at 580 W throughout deposition. Substrates were placed on a rotating holder and heated by a backside resistance, at temperatures ranging from 450 to 600 °C. Pumping was performed using a series of a turbomolecular pump (TMP), a mechanical booster pump (MBP) and a rotary pump (RP). The operating pressure was 7-9 mTorr.

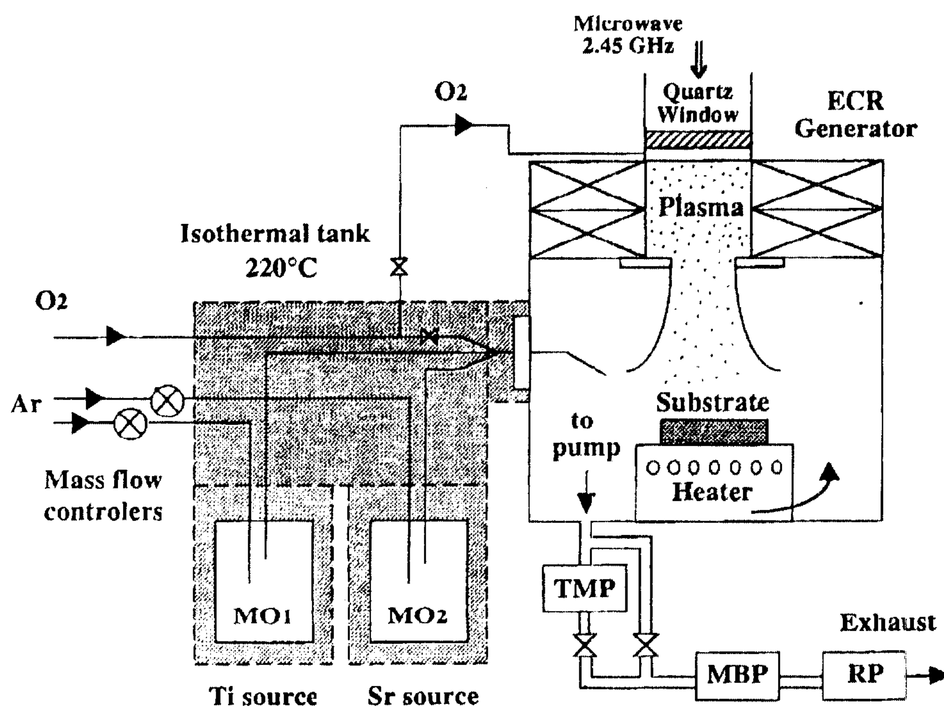

Figure 1 Schematic representation of the ECR MOCVD system.

$SrTiO_3$ deposition

With a permittivity in the 150-500 range when in thin films, $SrTiO_3$ and $(Ba,Sr)TiO_3$ are expected to be used in conjunction with a simple stacked capacitor configuration in Gbit scale

DRAMs [5-6]. The predicted design rule for the storage node is 0.2 μm or less. Therefore, in order to avoid coupling between adjacent nodes, $SrTiO_3$ and $(Ba,Sr)TiO_3$ films should have a lateral thickness of 600 Å or less, over 2:1 to 2.5:1 aspect ratio nodes [5]. The principal requirements these materials have to meet for use in Gbit DRAMs are thus a large permittivity ($\varepsilon_r \geq 150$) and low leakage current density ($J \approx 10^{-8}$ A/cm^2 at 1.0 V) when deposited in thin films, as well as a good step coverage over high aspect ratio features.

After considering the requirements for use in Gbit DRAMs, it is then important to determine and study the important parameters affecting the properties of $SrTiO_3$ and $(Ba,Sr)TiO_3$ thin films. For $SrTiO_3$ thin films prepared by ECR MOCVD, the most influential parameters were found to be the Sr/Ti composition ratio [5,8,9], the film thickness [8], the deposition temperature [8,10], the ECR plasma power [12] and the electrode materials.

The film composition was found to affect important structural and electrical properties, such as the film microstructure, crystallinity, refractive index, dielectric constant and leakage current density [5,9]. Crystallized $SrTiO_3$ films could be prepared at 550 °C by thermal CVD [5] and at a temperature as low as 400 °C by ECR MOCVD [8]. For deposition temperatures above the crystallization temperature, XRD analysis showed that perovskite structure peaks only exist for $SrTiO_3$ films with a composition $0.7 \leq Sr/Ti \leq 1.2$. SEM and TEM observation showed differences in the microstructure with the film composition [5,9]. SEM top views first showed that grains have a round shape for Ti-rich films, a triangular shape for near stoichiometric films and a stretched triangular shape for Sr-rich films. TEM cross-sectional observation then indicated that the microstructure evolves from a granular structure to a columnar structure when composition is changed from Ti-rich to Sr-rich. Titanium rich films are thought to be composed of a mixture of a titanium rich phase and crystalline $SrTiO_3$, and strontium rich films are believed to correspond to a $(SrTiO_3)_m(SrO)_n$ structure [9]. A study of the film refractive index with composition showed that a maximum refractive index of n = 2.4 is obtained for stoichiometric films, and as can be seen in Figure 2, the dielectric constant also is at a maximum $\varepsilon_r = 170$, for Sr/Ti = 1.0. High permittivity is thus clearly associated with good crystalline properties, and composition control will be a key issue in the preparation of $SrTiO_3$ films for Gbit DRAMs.

Though permittivity reaches a maximum for Sr/Ti = 1.0, leakage current density is minimum for titanium rich films, and gradually increases with increasing Sr/Ti ratios over the Sr/Ti = 0.7 to 1.2 composition range [12]. As for step coverage, no significant change was observed in lateral coverage for the same Sr/Ti = 0.7 to 1.2 composition range.

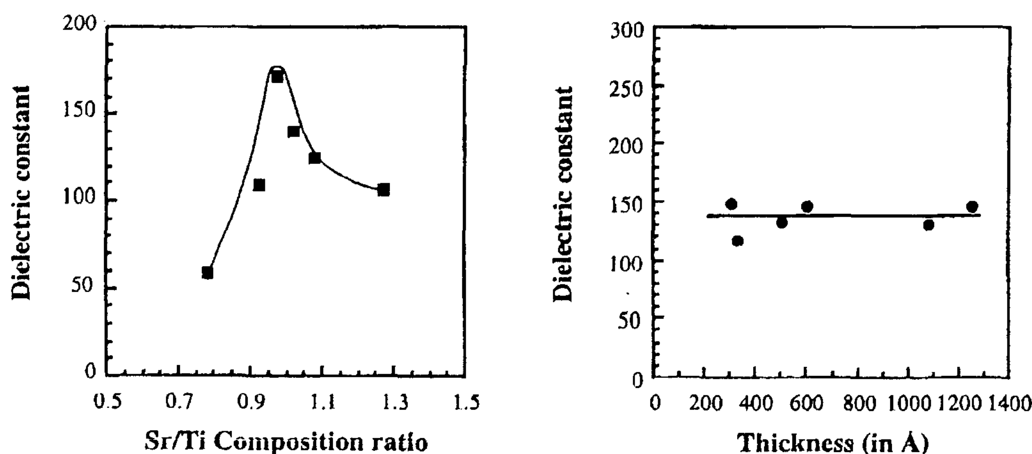

Figure 2 Variation in the dielectric constant with the Sr/Ti ratio (1200 Å $SrTiO_3$ films) and film thickness (Sr/Ti = 1.0), for $SrTiO_3$ thin films prepared by ECR MOCVD at 450 °C on Si substrates with Au top electrodes and Pt bottom electrodes.

Film thickness is another important parameter affecting the properties of $SrTiO_3$ thin films [5]. Variations in the dielectric constant and leakage current density were studied as a function of the film thickness, for stoichiometric $SrTiO_3$ thin films (Sr/Ti = 1.0) prepared by ECR MOCVD at 450 °C. As can be seen in Figure 2, permittivity remains constant near $\varepsilon_r = 150$ for an $SrTiO_3$ film thickness between 300 Å and 1300 Å. However, the leakage current density increases progressively with film thickness, and a sharp increase is observed for films thinner than 300 Å. An $SrTiO_3$ film thickness of 400 Å appears to be the best compromise between high capacitance and low leakage current density, which has a value less than 10^{-6} A/cm^2 at 1.0 V, for 400 Å $SrTiO_3$ films on RuO_2 bottom electrodes.

Reaction mechanisms and step coverage

The influence of the substrate temperature on the deposition rates of Sr and Ti was then studied, in order to determine the dominant reaction mechanisms for SrO and TiO_2 deposition by ECR MOCVD. $SrTiO_3$ films were deposited directly on Si substrates and the temperature was varied between 450 °C and 600 °C. The Sr and Ti deposition rates, extracted from RBS composition measurements of $SrTiO_3$ films are presented in Figure 3, as a function of the substrate temperature. Both rates remain constant with temperature, and Sr and Ti deposition are believed to be transport limited processes over the 450 - 600 °C temperature range. The surface reaction rate is believed to be high, even at a low temperature of 450 °C, thanks to the energy brought to the substrate surface by the ECR O_2 plasma. This could probably explain why Sr and Ti deposition are transport limited processes between 450 and 600 °C.

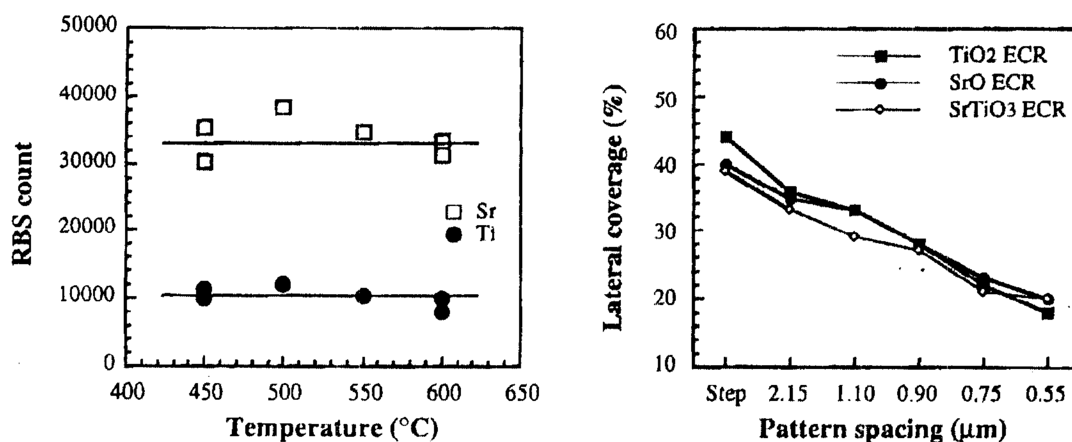

Figure 3 Sr and Ti deposition rates as a function of temperature (left) and variation in the lateral coverage with pattern spacing, for 1000 Å TiO_2, SrO and $SrTiO_3$ films prepared at 450 °C by ECR MOCVD (right).

The step coverage of TiO_2, SrO and $SrTiO_3$ thin films prepared by ECR MOCVD was studied, using 5000 Å high SiO_2 patterns on silicon. Lateral coverage results are presented in Figure 3, for various patterns spacing from an isolated single step to 0.55 µm spaced patterns. Very similar results were obtained for the three materials, possibly because the three deposition processes are all transport controlled processes. The decrease in lateral coverage with decreasing pattern spacing clearly shows that the supply of reactive species to the sidewalls of narrowly spaced patterns is the main step coverage limiting mechanism for ECR MOCVD $SrTiO_3$ films. The step coverage results presented in this study were obtained on SiO_2 test patterns, which differ from the real capacitor structure. Much better coverage was obtained for the real capacitor structure, as will be shown below, with 50 %

coverage over 0.3 μm spaced patterns. Therefore, the quantitative results presented above should be considered carefully, and more attention should be paid to the influence of the deposition regime on step coverage than to the actual step coverage values.

Gbit-scale DRAM Capacitor Technology

A new stacked capacitor technology with high permittivity $SrTiO_3$ films on 1 Gbit compatible RuO_2/TiN storage nodes was developed for Gbit-scale DRAMs [6]. Considering the results of the previous studies, $SrTiO_3$ films were prepared by ECR MOCVD at 450 °C, the composition was Sr/Ti = 1.0, the nominal film thickness was 1000 Å, and the lateral thickness between 400 Å and 500 Å. Though $(Ba,Sr)TiO_3$ films exhibit a larger permittivity than $SrTiO_3$ films, $SrTiO_3$ was selected as the 1 Gbit DRAM capacitor dielectric, because a sufficient storage capacitance can be obtained using $SrTiO_3$ films over 0.5 μm high RuO_2/TiN storage nodes. $SrTiO_3$ presents other advantages, such as a lower dependence of ε_r on the film thickness than $(Ba,Sr)TiO_3$, and it is easier to prepare by CVD.

Capacitor fabrication process

A schematic representation of the capacitor structure is shown in Figure 4. N-type poly-Si plugs were first fabricated in 600 nm thermal SiO_2. A 500 Å TiN barrier and 5000 Å RuO_2 storage electrodes were then deposited by reactive DC sputtering [13]. For RuO_2 sputtering, a Ru metal target was used, the sputtering gas was a mixture of Ar and O_2, and near stoichiometric RuO_2 was obtained for 75 % O_2 in the gas mixture [13]. The typical RuO_2 deposition rate was 7 nm/min.

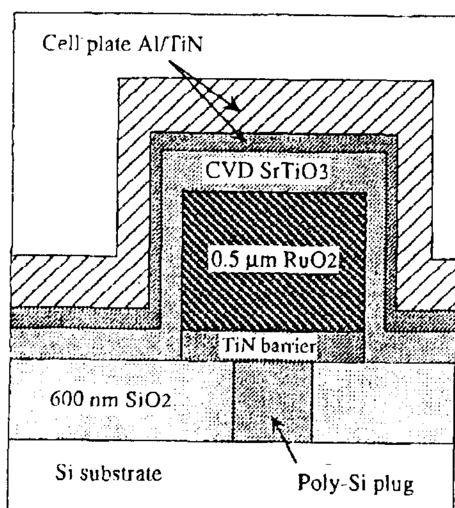

Figure 4 Cross-sectional schematic representation of the 1 Gbit DRAM capacitor structure.

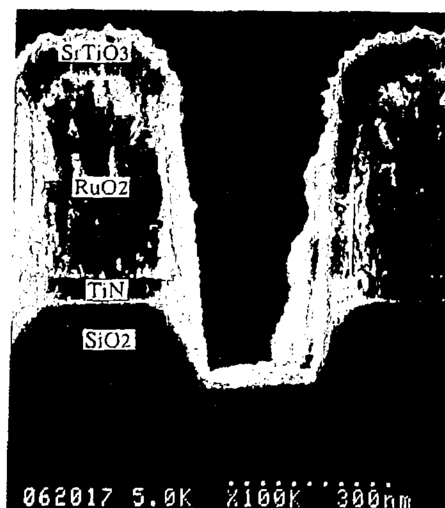

Figure 5 Step coverage of 1000 Å ECR MOCVD $SrTiO_3$ films.

The RuO_2/TiN structure was patterned by photolithography or electron beam lithography followed by reactive ion etching (RIE). Etching of the RuO_2/TiN structure was carried out by ECR plasma, using an O_2-Cl_2 mixture as the etching gas [14]. As most photoresists are etched in an O_2 plasma environment, a 3200 Å SOG hard mask was deposited on top of RuO_2 films. RuO_2/TiN etching was performed according to the following sequence: The SOG hard mask was first etched in

a CHF_3 plasma. Resist was then removed in an O_2 down flow plasma. RuO_2 was etched in an O_2-Cl_2 mixture. SOG was removed in a CHF_3 plasma, and TiN was finally etched using a Cl_2 plasma. The main RuO_2 etching mechanism is as follows : $RuO_2 + O_2 \rightarrow RuO_4 \nearrow$ [14]. By adding 10% Cl_2 to the oxygen plasma, a RuO_2 etching rate more than 250 nm/min and a selectivity of 10:1 between RuO_2 and SOG were obtained. The increase in the etching rate and selectivity are believed to be due to the higher etching efficiency of oxychloride anions such as ClO^-, present in the O_2-Cl_2 plasma, as compared with O^- anion in the O_2 plasma [14]. A damaged layer was observed by SEM at the top and on the sidewalls of RuO_2 patterns, after RuO_2/TiN etching and SOG removal were completed [6]. The damaged layer can be removed by an O_2 ashing treatment performed at 150 °C, after RuO_2/TiN etching is completed, and a clean $SrTiO_3/RuO_2$ interface can be obtained [6].

Following the RuO_2 surface treatment, 1000 Å $SrTiO_3$ films were prepared by ECR MOCVD at 450 °C, with the deposition conditions described above. 7000 Å Al/500 Å TiN plate electrodes were finally deposited by sputtering and patterned by RIE.

The test patterns used to measure the electrical characteristics of the capacitors were fabricated by conventional photolithography. The minimum dimensions were 0.4 μm for the pattern width and the space between adjacent patterns. Electron beam lithography was also used in a series of experiments designed to verify that RuO_2/TiN electrodes can be patterned down to 1 Gbit-scale dimensions, and to measure the step coverage of $SrTiO_3$ thin films on such a high aspect ratio storage node structure. As can be seen in Figure 5, a minimum lateral step coverage of 50 % was obtained for 1000 Å $SrTiO_3$ films deposited on 0.3 μm spaced and 0.5 μm high RuO_2/TiN nodes. A step coverage of 50 % is acceptable, since only the sidewall capacitance will be used in 1 Gbit DRAMs and the lateral thickness is uniform along the RuO_2/TiN storage electrode sidewalls.

Electrical characteristics

Capacitance-frequency and leakage current density characteristics were measured using an array of more than 2000 stacked RuO_2/TiN nodes, identical to the one presented in Figure 4. Electrical contacts for the measurements were made on the wafer backside and the top aluminum layer. The total projected area of the capacitor array on the chip was 0.0081 mm^2. The $SrTiO_3$ film thickness was 1000 Å on the top of patterns and about 400 Å on the pattern sidewalls. Capacitance-frequency measurements showed that capacitance and tanδ are stable over the 100 to 1 MHz frequency range, and ε_r = 150 for 400 Å films [6].

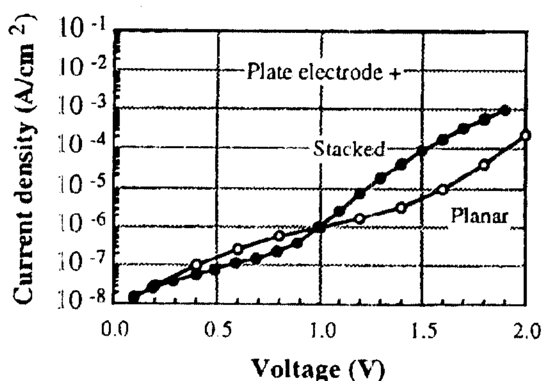

Figure 6 J-V characteristics of 40 nm $SrTiO_3$ (planar) and 100 nm $SrTiO_3$ (40 nm on the sidewalls) stacked over 0.5 μm high RuO_2/TiN nodes.

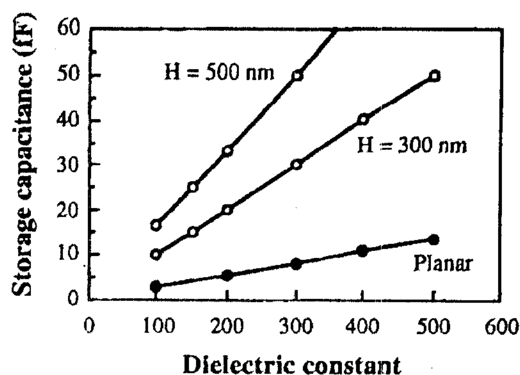

Figure 7 Storage capacitance as a function of ε_r and capacitor type (planar or stacked). H=stack height. Planar, 40 nm $SrTiO_3$ Stacked, top = 80 nm, side = 40 nm.

As shown in Figure 6, a low leakage current density of 8×10^{-7} A/cm^2 is obtained at half Vcc = + 1.0 V, for 1000 Å $SrTiO_3$ films (400 Å on the sidewalls) deposited on the array of stacked RuO_2/TiN nodes. Moreover, the leakage current characteristics are very similar for the 1000 Å $SrTiO_3$ films (400 Å on the sidewalls) deposited on the stacked structure and the 400 Å $SrTiO_3$ films deposited on the planar structure. This last result is very important because it shows that, for the same thickness of 400 Å, top and sidewall $SrTiO_3$ have the same leakage current properties. As shown in Figure 7, using electrode sidewalls only, and with an $SrTiO_3$ lateral film thickness of 400 Å (ε_r = 150), a large capacitance of 25 fF can be achieved for 0.5 µm high RuO_2/TiN electrodes in a 0.125 µm^2 (0.25 µm x 0.50 µm, for a DBL configuration) capacitor area.

Conclusion

Film composition and film thickness were found to be important parameters determining the properties of $SrTiO_3$ thin films prepared by ECR MOCVD. Maximum permittivity and low leakage current density were obtained for stoichiometric composition, Sr/Ti = 1.0. A minimum thickness of 400 Å was found to be necessary to obtain $SrTiO_3$ films with sufficient electrical properties. The substrate temperature did not affect the deposition rate and step coverage, but should be kept low to prevent degradation of the bottom electrode structure. A new stacked capacitor technology was finally described, comprising $SrTiO_3$ films prepared by ECR MOCVD at 450 °C over electron beam and RIE patterned RuO_2/TiN storage nodes. A storage capacitance of 25 fF and a leakage current density of 8×10^{-7} A/cm^2 can be obtained at half V_{CC} = + 1 V, for $SrTiO_3$ films with a sidewall thickness of 400 Å deposited on 0.5 µm stacked RuO_2/TiN storage nodes. This capacitor technology is suitable for use in 1 Gbit DRAMs.

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