SILICON DIOXIDE FILMS FOR INTERMETAL DIELECTRIC APPLICATIONS DEPOSITED BY AN ECR HIGH DENSITY PLASMA SYSTEM

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ABSTRACT

Deposition of thermal quality SiO_2 using a high density plasma ECR CVD process has been demonstrated to give void and seam free gap fill of high aspect ratio metallization structures with a simple oxygen-silane chemistry. This is achieved by continuous sputter etching of the film during the deposition process. A two-step process is utilized to deposit a composite layer for higher manufacturing efficiency. The first step, which has a deposition rate of approximately 0.5 μm/min., is used to provide complete gap fill between the metal lines. The second step, which has a deposition rate of up to 1.5 μm/min., is used to deposit a total thickness of 2.0 μm for the intermetal dielectric film. The topography of this composite film is very compatible with subsequent chemical mechanical polishing (CMP) planarization processing.

INTRODUCTION

For advanced integrated circuit technologies, the requirement of multiple levels of metal interconnections and reduced feature sizes place stringent demands on the intermetal dielectric insulating layers. The dielectric film should demonstrate good gap fill capability for structures with gaps less than 0.3 μm wide and aspect ratios as large as 3 or more. The preferred material should have a low dielectric constant to reduce signal delays resulting from parasitic capacitance. The deposition temperature of the film should be no higher than 400°C to be compatible with aluminum metallization. The film must be stable with an electrical breakdown resistance greater than 7 Mev/cm. To accommodate advanced lithographic techniques, the film must be easily planarized. As such, the films should be compatible with CMP technology. And finally, the film must be deposited at a rate that is compatible with high volume manufacturing technology.

Silicon dioxide, deposited in an ECR reactor from the reaction of silane and oxygen, meets these film requirements.[1,2] In this paper, the requirement for a high throughput deposition process is addressed.

ECR SYSTEM

The reactor used for the deposition of this SiO_2 film utilizes an ECR source chamber for high efficiency of coupling energy into the plasma. A schematic drawing of the reactor is shown in Figure 1. Microwave energy at 2.45 GHz is coupled into the source chamber where an efficient plasma is maintained for the argon and oxygen gases fed into

this chamber. An ion beam of argon and oxygen is extracted from the source chamber and is directed toward the wafer, which is held by a temperature controlled electrostatic chuck (ESC). Silane is fed into the reaction section of the system by a separate manifold. The silane is adsorbed onto the surface of the wafer and reacts with oxygen ions to form the SiO_2 film.[3,4] The ESC is separately powered by a 13.56 MHz RF generator. The microwave power controls the density of the ion beam and the RF power controls the energy of the ions involved in the surface deposition reaction.

The wafer temperature is sensed by a temperature probe and helium gas is introduced behind the wafer to equilibrate the temperature between the wafer and the temperature controlled ESC. With this mechanism, the wafer can easily be maintained at a temperature less than 400°C.

Recent modeling indicates that the deposition process consists of a heterogeneous ion molecule reaction between adsorbed silane and the oxygen ion beam.[5] Simultaneously, sputter etching by the argon ion beam occurs on the surface. This combined process is shown schematically in Figure 2. Due to its physical nature, argon sputter etch is more efficient at a 45° angle. This leads to faceting at the corners of exposed surfaces. This faceting phenomena ensures that the deposited film does not close gaps in the deposition of the film in structures with gaps as small as 0.25 μm. Figure 3 shows the profile of the deposition process utilizing a technique in which the gas ratios of oxygen and silane were modified slightly during the deposition process to provide a thin silicon rich layer. Cross sections of this structure and decoration etching clearly show the anisotropic nature of the gap fill deposition process for the SiO_2 film.

TWO-STEP DEPOSITION PROCESS

To efficiently fill a structure with narrow gaps for a multilevel metallization technology, a two-step deposition process has been developed. In the first step, the deposition process is optimized for efficient gap fill capability. The etch to deposition ratio is optimized to approximately 35%. This leads to a deposition rate in the range of 0.4 to 0.5 μm/min. Figure 4 shows a structure with 0.35 μm spacing which has been filled by such a process.

For multilevel metallization, the thickness of the intermetal dielectric deposited before CMP planarization is often 2.0 μm thick. To efficiently deposit a layer of such thickness, the optimized gap fill deposition process is used for only the first 0.75 μm of the deposition. After approximately 0.75 μm of SiO_2 is deposited, the deposition conditions are changed so that the SiO_2 deposition occurs at a higher rate. By reducing the etch to deposition ratio to approximately 10%, a SiO_2 deposition rate of approximately 1.2 to 1.5 μm can be achieved. Table 1 compares the SiO_2 film characteristics for the two deposition steps. Figure 5 shows the cross section of a metal structure that was filled with such an efficient deposition process. A high quality SiO_2 film is deposited utilizing this two step process. Typical uniformity of this composite film is better than 2.5%, the stress is less than 200 MPa compressive, the dielectric constant is less than 4.1, and the

hydroxyl content of the film is less than 1%. The total deposition time for a 2.0 μm film is typically less than 150 sec.

COMPATIBILITY WITH CMP

The SiO_2 film deposited by the high density ECR plasma is easily planarized by CMP processing.[6] Figure 6 shows a structure with varying metal line widths on which the ECR SiO2 film has been deposited. When this surface is planarized, mesa structures above wide metal lines are quickly polished away, as the total pressure of the polishing process is focused on these structures. The remaining small peaks above the more narrow metal lines are quickly polished away by subsequent polishing. It has been reported that the CMP efficiency of the ECR SiO_2 is 33% higher than for a comparable TEOS based SiO_2 film.[7] Figure 7 shows the cross section of a metallization structure after CMP processing.

CONCLUSION

It has been demonstrated that a high density ECR plasma can be used to deposit a high quality SiO_2 film that is void and seam free in narrow gap structures of advanced metallization technology. An efficient deposition process can be used in which an optimized gap fill deposition is utilized for the first portion of the deposition process. After the gaps between the metal lines have been filled, the deposition conditions can be changed so that a high rate deposition process can be utilized. The composite SiO_2 film has good uniformity, low stress and a low dielectric constant. This film is very compatible with subsequent CMP planarization processing.

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TABLE 1

Parameter	First Layer Properties	Second Layer Properties
Deposition Rate	0.4 to 0.5 μm/min	1.2 to 1.5 μm/min
Uniformity	2.3% (1 σ)	3.0% (1 σ)
Hydroxyl Content	< 1 %	< 1%
Stress	120 MPa	150 MPa
Index of Refraction	1.470 to 1.500	1.475 to 1.480
Dielectric Constant	< 4.1	< 4.1

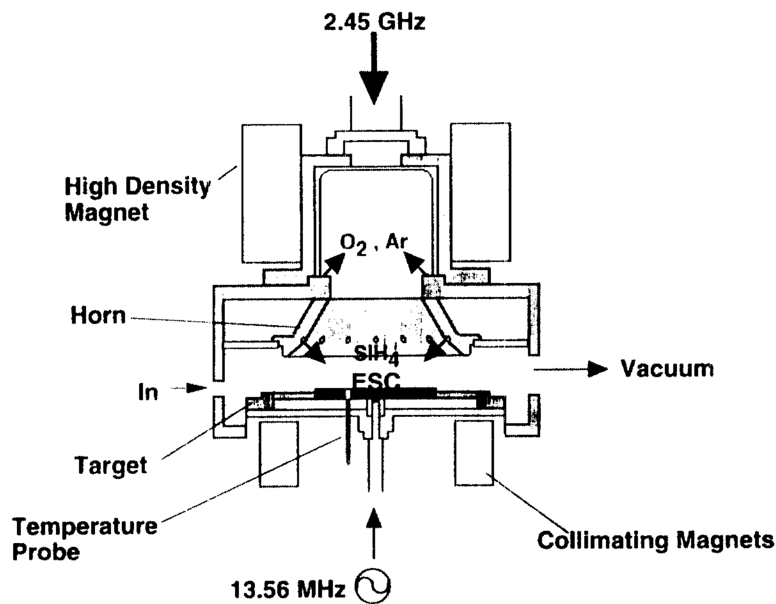

Figure 1. High Density Plasma ECR CVD Chamber

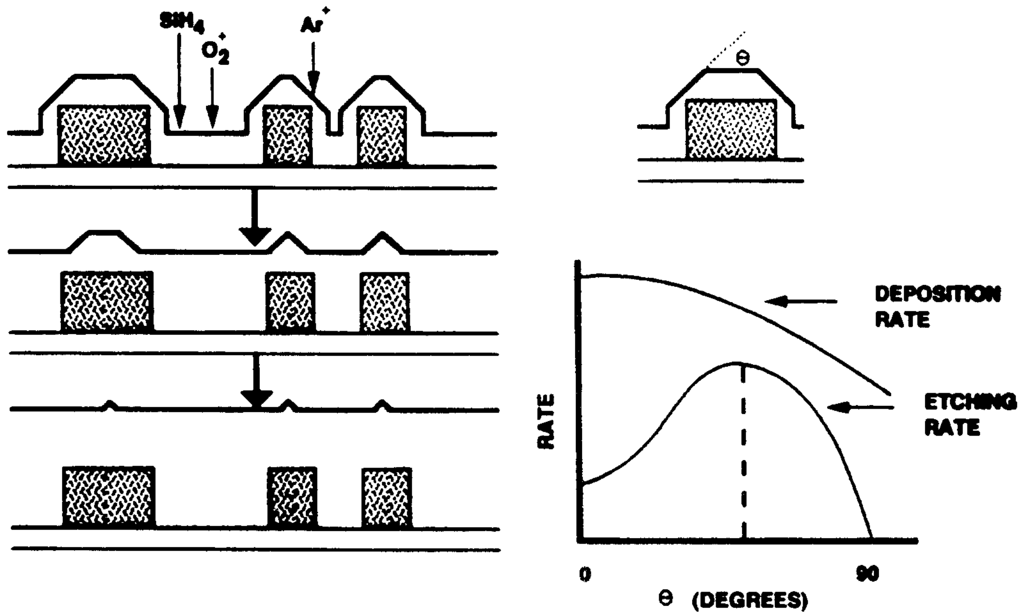

Figure 2. Principle of gap fill and local planarization

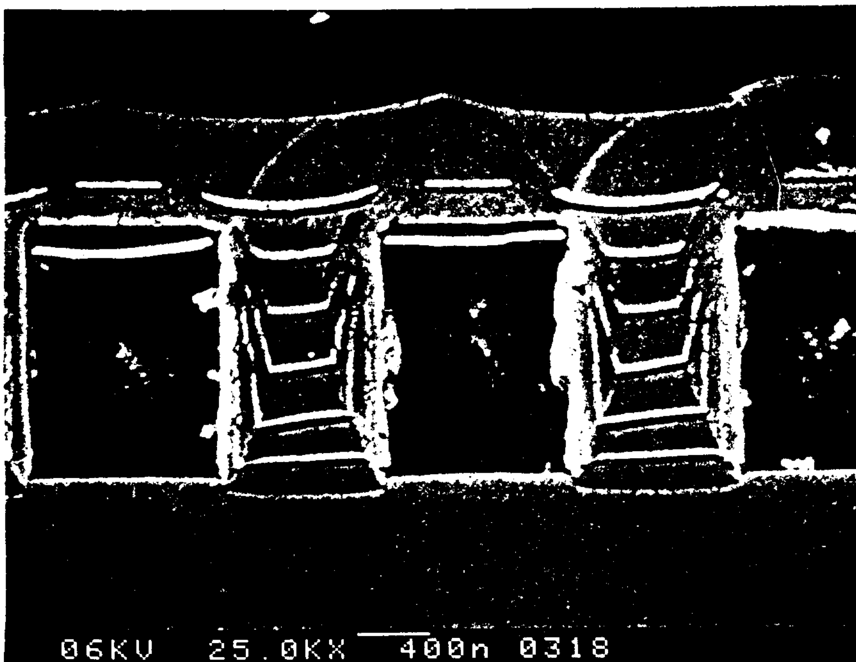

Figure 3. Demonstration of bottom-to-top anisotropic gap fill

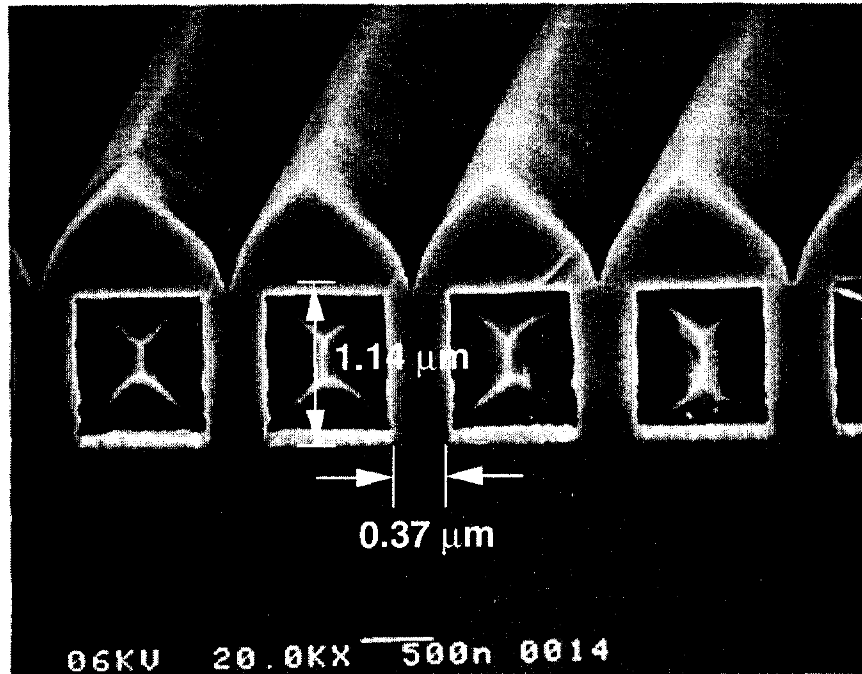

Figure 4. Example of gap fill capability for metal lines with spacing of 0.37μm and an aspect ratio 3:1 filled with a standard 35% etch to deposition ratio

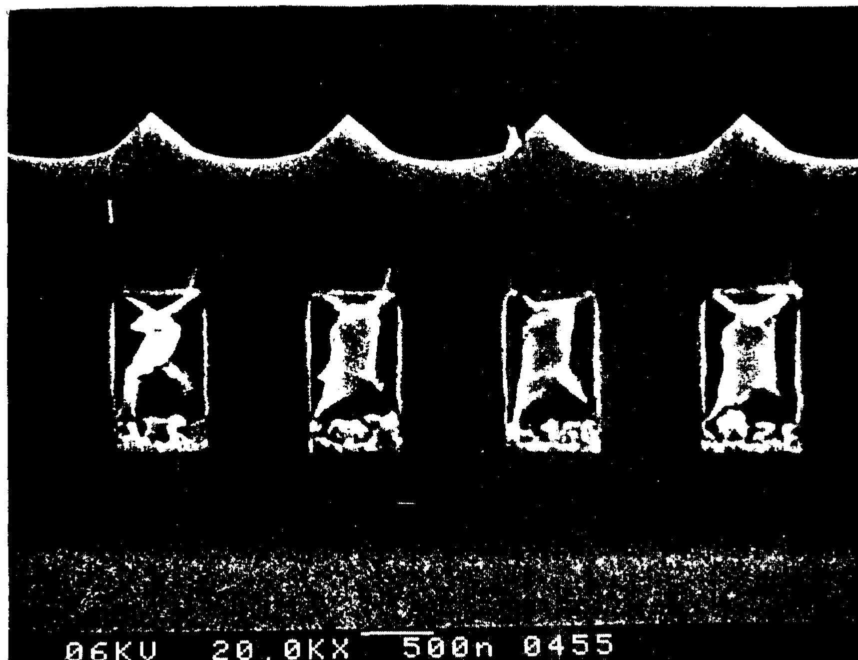

Figure 5. Metal interconnect structure filled with a complete two-step deposition process

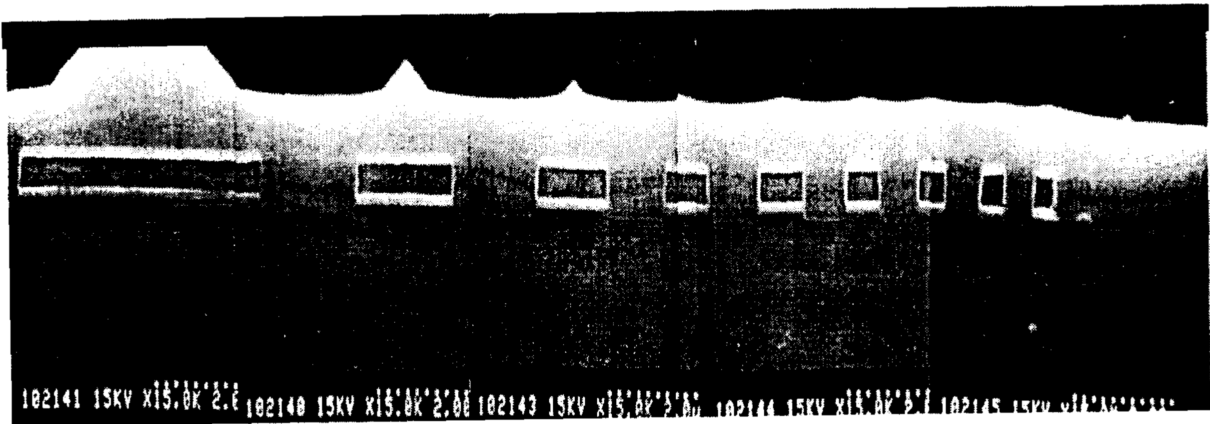

Figure 6. Diminishing peak structures for ECR high density oxide deposited over metal lines with varying line widths

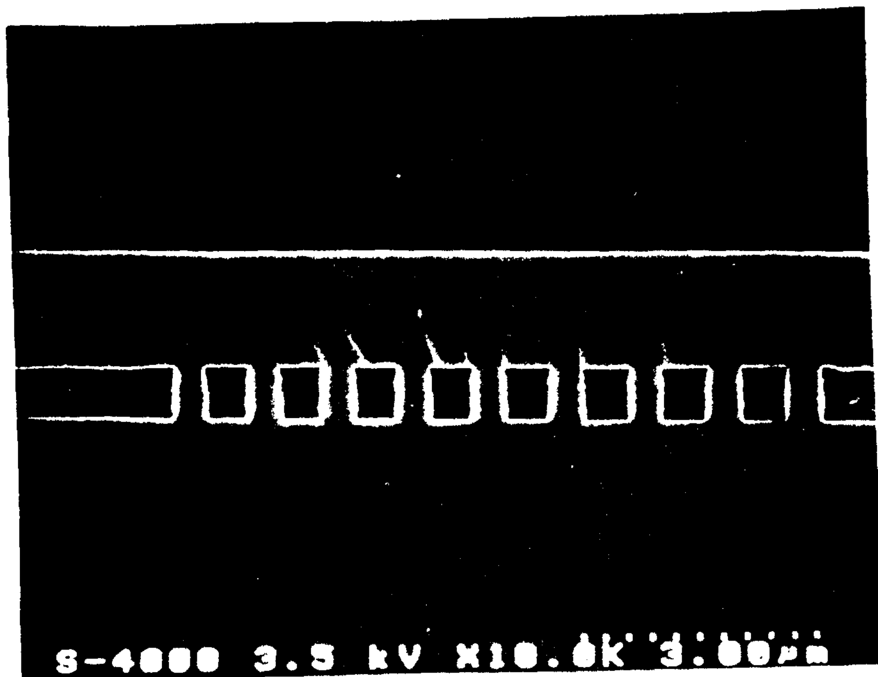

Figure 7. Cross section of a metallization after CMP processing

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