CVD and Sputtering-reflow Copper Metalization Technique with CMP

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Abstract

We review the copper CVD line, via fill properties, and CMP line resistance. With CVD, trenches and vias with high aspect ratio (above 3) can be filled completely. Sputtering-reflow technique, a new method to filling copper into lines, is also reviewed to compare the CVD process.

1. Introduction

Copper interconnects have been received much attention for high reliability and high speed LSI operation, because copper has large electromigration resistance [1, 2] and has low resistivity (1.72 μΩ•cm) Increasing packing density of LSI, the wiring dimension decreases and the current density increases. Large electro- and stress migration resistance are needed. Also wiring delay is becoming larger than delay time in a device. Wiring delay will be reduced by low resistivity copper wiring.

The progress speed of copper wiring technology has been very slow because mainly formation of copper wiring is very difficult. Copper dry etching is difficult because of low vapor pressure Cu halides [2]. High temperature (300°C) is necessary for etching process [2]. Cu corrosion easily occurs by Cu halide compounds diffused from the chamber walls. Chemical mechanical polishing(CMP) has been developed to overcome the difficulty of formation of Cu interconnection [3, 4]. When using CMP process, chemical vapor deposition (CVD) method should be used to embed copper into trenches and vias due to its superior step coverage [4]. Copper CVD has been studied by large number of researchers.

In this paper we review Cu-CVD filling properties of trenches and vias and CMP line formation performances. Recently Cu sputter-reflow method has been succeeded at relatively low temperature (450°C) [5]. We also review sputtering-reflow properties to compare CVD technique.

2. Experimental procedure

We used four-inch wafers. Sputter TiN (50 nm) is formed as glue layers on SiO_2 trench. Trench width and depth are from 0.2 to 16 μm and 0.3 and 0.5 μm. Length was 1,500 mm.

CVD source is hexafluoroacetylacetonate copper(I) trimethylvinylsilyl (Cu(hfa)TMVS [6, 7]). The precursor is vaporized with hydrogen gas. Hydrogen actually serves as both carrier and reductant.

Three sputter chambers were used. One is the conventional. Second chamber has a collimator of one aspect ratio. The other is a long-through sputtering chamber [8]. The background pressure of the conventional sputter chamber is below $3x10^{-7}$ Torr. Others were high vacuum chambers ($3x10^{-9}$ Torr). The distance between target and wafer is 5.5 cm at a conventional one, 7.0 cm at a collimator chamber, 14 cm at a long-through sputtering chamber. Collimator and long-through technique can offer the same good step coverage.

Cu reflow was done with two method. One method is annealing in a vacuum chamber without exposed sputtered Cu film to the air after Cu deposition. The other method was annealing with hydrogen gas. Hydrogen was used as a reductant gas of copper oxide on the sputtered copper films. Reflow time is about 3 min.

Chemical mechanical polish was done with alumina based acid slurry of XGB6861, XJFW7355 (delivered from Rodel). Polishing pad was a stacked type of IC-1000/suba400 (delivered form Rodel-Nitta). Polishing rate was about 2 μm/min.

3. Results and discussion

3.1. CVD

Figure 1 shows the growth rate as a function of the growth temperature and the source (Cu(hfa)TMVS) temperature. When the precursor temperature is high (the precursor supply large), over a wide growth temperature, the deposition rate increases as the growth temperature increases (below 170°C). The region is reaction limited. When the precursor temperature is low (the precursor supply small) the growth rate is almost independent of the growth temperature for the higher growth temperature range.

Figure 2 shows the resistivity as function of the growth temperature along with the growth rate. The resistivity decreases as the growth rate decreases. We grew copper below 175°C to obtain 2.0 μΩ•cm.

Figure 3 shows the surface morphology of copper. Above 170°C (diffusion limited region), the surface is rough (fig. 3a). Below 170°C, the surface become smooth (fig. 3b, kinetic limited region). Figure 4 shows the line and via filling properties. Even the high aspect ratio (about tow) via and trench can be filled with CVD-copper. We filled 2.5 aspect ratio of 0.3 μm diameter via and 3.5 aspect ratio trench of 1.5 μm width. We fortunately can use the kinetic controlled region (below 170°C) to obtain low resistance and good line and via filling properties.

3.2. Sputtering-reflow

First we tried the copper sputter and reflow with high vacuum background chambers ($<3x10^{-9}$ Torr) to prevent copper oxidation. We considered copper oxide to prevent flowing copper into trenches. Also to obtain large step coverage of copper, we set the target at 14 cm apart from the Si wafer (long-through sputtering). Figure 5 shows the cross sectional view of the trench filled with copper. The trench is not filled completely of as deposition without reflow. The bottom coverage is very large due to that the copper target is far from the Si wafer. At 350°C for 3 min copper reflows well to fill trenches (fig. 5b). However the trenches and vias with aspect ratio above about 1.5 were not filled

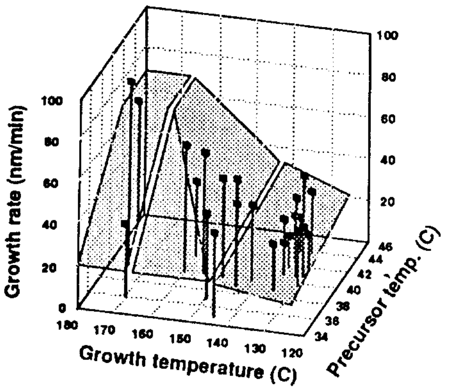

Fig. 1. The growth rate of Cu-CVD as a function of growth temperature and precursor temperature.

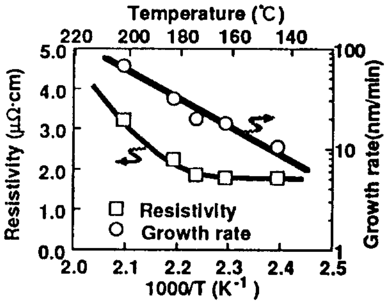

Fig. 2. The growth rate and resistivity of CVD-Cu as a function of growth temperature.

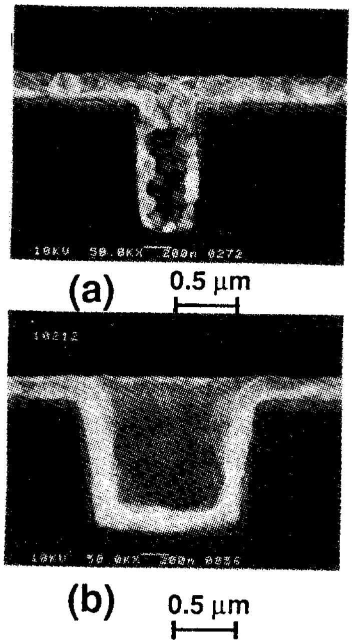

Fig. 3. Surface morphology of Cu grown at (a) diffusion limited region and (b) kinetic limited region.

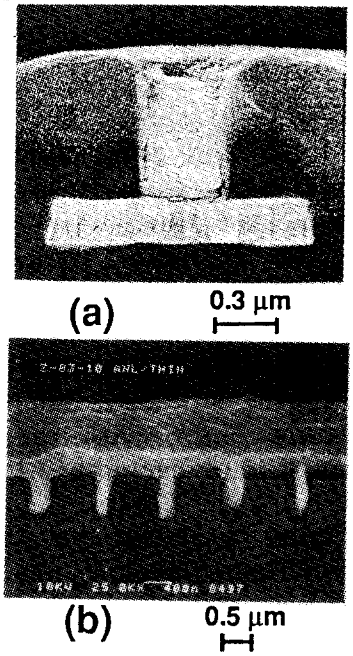

Fig. 4. The via (a) and line (b) fill properties.

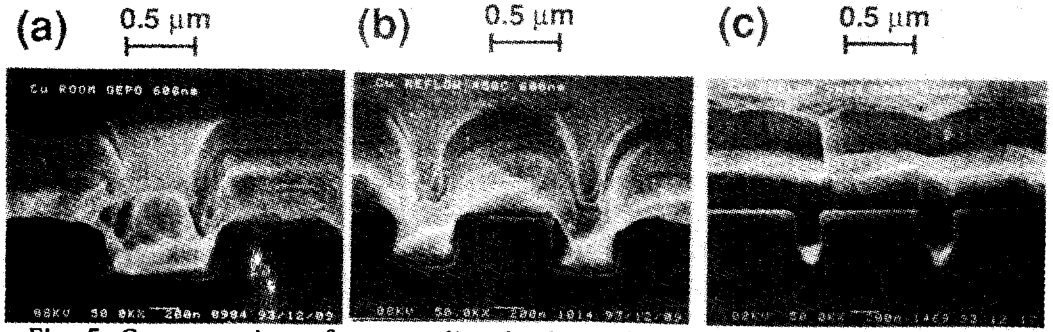

Fig. 5. Cross section of copper line by long thorugh sputtering. (a) As deposition. (b) Reflowed at 350°C for 3 min in vacuum. (c) Reflowed at 450°C for 3 min in vacuum.

(figure 5c). Because this method does not present sufficient step coverage.

Using a conventional collimator trenches with aspect ratio below one can be filled with copper. A conventional collimator method has similar performance with wide gap method for step coverage [8].

We tried sputter and reflow at lower vacuum ($<3\times10^{-7}$ Torr) background to determine the oxidation effect on copper reflow. Copper does not reflow and the shape is exactly same with as deposited copper films. We introduced hydrogen as a reductant of copper oxide and to reflow copper well. Copper well reflowed and the surface of copper film is very flat. Hydrogen is very effective for reflowing copper. However, the step coverage is also important for filling trenches with high aspect ratio. The trenches with aspect ratio of 1.5 were not filled with copper due to insufficient step coverage.

3.3 CMP

The ratio of polishing rate of copper to SiO2 was about 100. The TiN polishing rate is about 75% of copper polishing rate. The surface morphology after CMP is shown in figure 6. Because copper metal is very soft, large number of scratches can be seen. These scratches have no effect on the line resistivity. However these scratch will prevent from removing the contamination on copper. We must decrease these scratches.

3.4. Line resistivity

The copper line resistance is shown in fig. 7 as a function of the line width. Lines filled by CVD have the relatively large standard deviations. Probably it is due to the non-uniformity of copper film thickness. It results non-uniform copper polish. The resistance of long-through sputtering made line have smaller standard deviations than that of CVD line resistances because of uniform copper film thickness. The standard deviation is about 10% of mean value over from 0.3 to 16 µm line width.

The mean value of apparent resistivity (µΩ•cm) is shown in figure 8. The value is calculated from the above line resistivity with the value of fixed line length and cross sectional area. The line width means total line width: copper and TiN. Lines filled by CVD have the relatively small resistivity below 1 µm width. It means that CVD copper was filled well into trenches below 1 µm because of large step coverage. Above o.3 µm, The apparent resistivity becomes large as the line width increases. It is due to the dishing effect of CMP (over polishing at the center of the line). Below 0.3 µm apparent resistivity increase as decreasing line width. Probably it is due to the large resistivity of TiN. Resistivity of TiN is about 100 µΩ•cm and the thickness is 50 nm. It is thick enough compared with copper line width. The apparent resistivity made by long through sputtering method are relatively low over an entire line width from 0.3 to 16 µm line width as well as CVD technique.

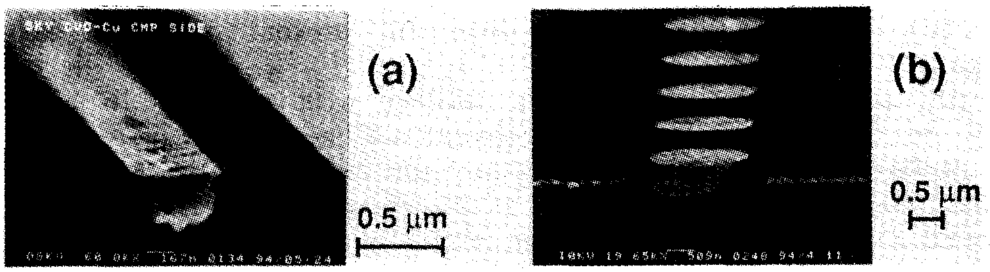

Fig. 6. Cu surfac after CMP. (a) Line and (b) via.

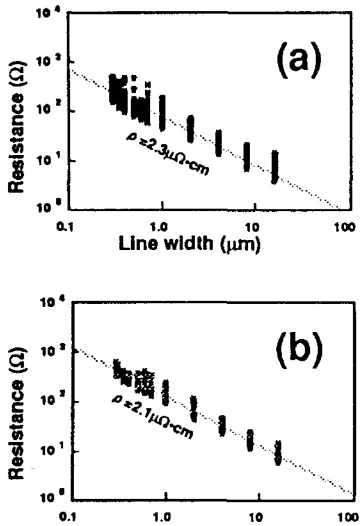

Fig. 7. The resistance of copper lines. (a) CVD. (b) Sputtering-reflow.

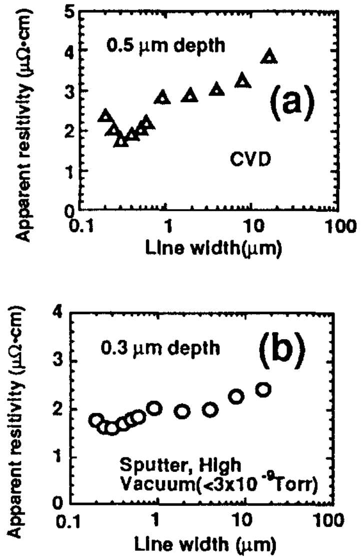

Fig. 8. The apparent resistivity of copper lines. (a) CVD. (b) Sputtering-reflow.

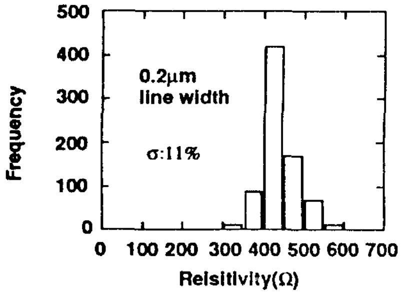

Fig. 9. The histogram of copper line resistance of sputtering-reflow sample.

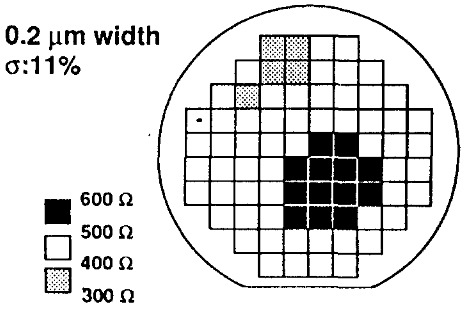

Fig. 10. The map of copper line resistance of sputter-reflow sample.

The histogram of the resistance of lines made by long-through sputtering are shown in figure 9. The uniformity of resistance made by CVD is worse than that by long-through sputtering. We show the results of the long-through sputtering. Above 450 Ω, the over polish is observed. The standard deviation is 11% of the mean value. The large deviation is mainly due to that the CMP polishing rate is not uniform. In figure 10 the map of resistivity shows the line resistivity of wafer center is large. The polishing rate of copper was large at the center, and was about 10% larger than the mean value. The ratio of copper polishing rate to SiO_2 rate was about 100. It is very large for using SiO_2 as a polish stopping layer. However, SiO_2 polishing rate is very large at narrow lines between copper lines(copper line and SiO_2 line is equal in this pattern). Copper polishing uniformity is very important to obtain uniform interconnect resistivity.

4. Conclusion

CVD has the characteristics: Trenches and vias with high aspect ratio (above 3) can be filled completely.

Sputtering-reflow method has the following characteristics: Trenches with aspect ratio below one can be filled completely. However, trenches and vias with high aspect ratio (above 1.5) can not filled completely.

Resistances of lines by sputter-reflow and CVD do not have much differences. Taking account of the difference in the manufacturing superiority, sputter is suitable for line formation of low aspect ratio (below one). CVD is suitable for via and high aspect ratio line and dual Damascene process (trenches and vias are filled at one time).

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