# Selective Deposition of *in-situ* doped Polysilicon using RTP-CVD for Shallow Junction Formation

H. G. Chun*, T. Y. Hsieh**, and D. L. Kwong**

*Department of Materials Science and Engineering, University of Ulsan, 680-749, Korea
**Microelectronics Research Center, University of Texas at Austin, TX 78712, USA

(Received Jan. 10, 1995)

# 얇은 접합형성을 위하여 *in-situ* 도핑된 폴리실리콘 박막의 RTP-CVD 선택적 증착에 관한 연구

천희곤*, T. Y. Hsieh**, D. L. Kwong**

*울산대학교 공과대학 재료공학과
**Microelectronics Research Center, University of Texas at Austin

(1995년 1월 10일 접수)

**Abstract** – Selective polysilicon was successfully deposited and *in-situ* doped with arsenic by rapid thermal processing chemical vapor deposition (RTP-CVD). Excellent selectivity was achieved with proper deposition conditions. The growth rate decreased as doping levels increased, and drastically decreased when the arsine mole fraction was higher than 5ppm. The growth rate was linearly proportional to the $SiH_2Cl_2$ flow rate for a fixed arsine flow rate. The dopant concentration was higher at the polysilicon/silicon interface and at the surface, and the dopant concentrations were higher when the deposition temperature was lower. The dopant transition width was about 40nm to 50nm. Extremely shallow $n^+$-p junctions were achieved and laterally uniform delineated junctions were also observed using RTP-CVD.

**요 약** - As으로 *in-situ* 도핑된 폴리실리콘 막을 원하는 부위에만 선택적으로 증착시킬 수 있는 RTP-CVD 증착기술이 성공적으로 수행되었다. 막의 증착속도는 도핑량이 증가함에 따라 점차 감소하였으나 As의 양이 5ppm보다 커지자 급격히 감소하였다. 또한 증착속도는 As의 유량이 일정할 때, $SiH_2Cl_2$ 유량에 따라 직선적으로 변화하였다. As 도펀트의 농도는 막 내부에 비해 폴리실리콘/실리콘기판의 계면과 표면에서 상대적으로 높게 나타났으며, 특히 증착온도가 낮을 때 As 도펀트의 농도는 더 높아짐을 알 수 있었다. 실리콘 표면에서 약 40-50nm 위치에서 도펀트의 농도천이가 급격히 일어났으며, 그 결과 RTP-CVD 공정을 이용할 때 극히 얇고 일정한 깊이분포를 갖는 $n^+$-p 접합을 형성시킬 수 있음을 알 수 있었다.

## 1. Introduction

The use of deped polysilicon films as diffusion sources for shallow junction formation has been demonstrated in several applications. In advanced bipolar technology, heavily doped polysilicon is used as an emitter contact and as a diffusion source for shallow emitter diffusions. In addition, it has potential applications in elevated source/drain MOSFET structures for the next generation ULSI technology. Recently, great interest has been generated in the selective deposition of polysilicon in seed windows of an oxide and/or nitride mask for CMOS, bipolar, and BiCMOS application. In order to ensure performance and reliability of ICs, the disparity between the mask layout dimensions and the final device geometry caused by the transfer of patterns should be minimized. In addition, a planar surface topology is highly desirable for fine-line lithography and the number of technological steps should be reduced.

Consequently, methods for self-aligned deposition or growth of materials in selected areas on thin film structures defined by lithography techniques have become increasingly attractive in the fabrication of ultra-small devices. A good example can be found in back-end processing, where the heavily doped polysilicon is used for shallow junction formation as well as for self-aligned contact refill and planarization for interconnect. The approach is simple, gives excellent contact yields with low contact resistance, and is not troubled by problems generally seen with selective tungsten deposition such as worm hole tunneling defects.

The *in-situ* doping of polysilicon has become increasingly important in the fabrication of VLSI devices and has many practical advantages compared with conventional methods of diffusion and ion implantation such as the elimination of the complexity of post-deposition doping processes. The important requirements of *in-situ* doping are the precision and uniformity of dopant profiles and the flexibility of dopant types and concentrations. Rapid thermal processing chemical vapor deposition (RTPCVD) is capable of meeting these requirements[1].

RTP is a widely used process in the fabrication of semiconductor devices (e.q., dopant activation and annealing after ion implantation, thermal oxidation and nitridation, silicide and salicide formation)[2]. RTPCVD is the combination of RTP with concept of CVD. It provides very short process times at high temperatures with the significant capability of rapidly changing the chemical gas environment, allowing *in-situ* multiple processings in a single chamber. Due to the precise control of the RTPCVD process, deposition of ultra-thin, heavily doped layers can be achieved. RTPCVD also permits the dopant concentration to be easily altered to cover a wide range by adjusting the process parameters. In our work, we report the selective deposition of *in-situ* doped polysilicon on silicon as a diffusion source using RTPCVD, and have studied the dopant diffusion and junction formation.

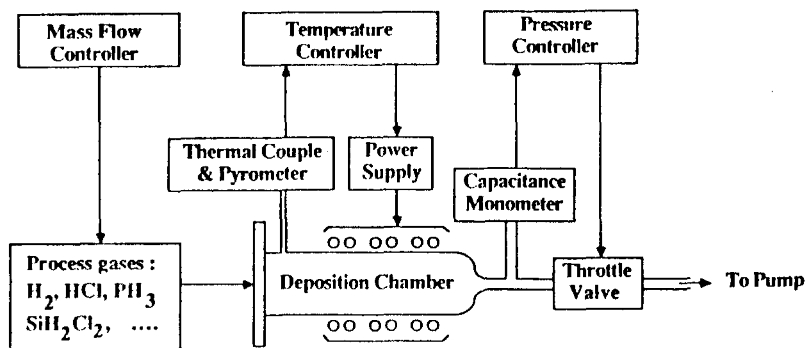


Fig. 1. Schematic diagram of the RTP-CVD system.

## 2. Experiment

The experiments were performed in a low pressure CVD quartz reactor and the substrate was heated from top and bottom by two banks of six nitrogen cooled tungsten halogen lamps as shown in Fig. 1. The cool wall system can prevent heavy deposition on the reactor wall and greatly minimize chamber memory effects due to previous processing. The substrate temperature during the reaction was monitored by an optical pyrometer and controlled by a microprocessor temperature control system, which periodically regulates the lamp power by comparing the signal from the optical pyrometer and the programmed temperature. In the RTPCVD process, the gas flows are set and stablized while the wafer is cool. Deposition is initiated by pulsing the lamps and bringing the wafer rapidly to deposition temperatures. At the end of each cycle, the lamps are shut off and the gas flows are stopped, and the reaction stops as the wafer rapidly cools down to room temperature. The deposition temperature can be reached in less than 3 seconds. The gas flow rates in the reaction chamber were controlled by mass flow controllers. The silicon source gas used in our system was dichlorosilane ($SiH_2Cl_2$). Arsenic was chosen to from shallow $n^+$-p junctions in our experiment due to the high solid solubility and low diffusion coefficient of arsenic. Arsenic doping was obtained by adding dilute arsine (100 ppm $AsH_3$ in $H_2$) to the gas flow during deposition. Hydrogen was used as the carrier gas. The advantage of the $SiH_2CL_2/H_2$ gas system is that the incorporation of Cl from $SiH_2Cl_2$ enhances selective growth under proper growth conditions.

The starting materials for selective polysilicon growth were p-type (100) Si wafers covered with a 700nm reactive ion etched (RIE) patterned oxide with the oxide sidewalls aligned in the [110] direction. They were chemically cleaned, etched in dilute hydrofluoric acid, and rinsed in deionized water just prior to the silicon deposition. To achieve a clean interface, an *in-situ* hydrogen pre-bake process was performed prior to deposition. No patterned p-type (100) Si wafer were used to investigate the dopant distribution profile.

## 3. Result and Discussion

The effect of temperature on the film quality and growth rate of the $SiH_2Cl_2/AsH_3/H_2$ system was first investigated. The deposition temperature varied between 775℃ and 1050℃ and the partial pressure ratio of dichlorosilane to hydrogen was fixed at 1:49. The arsine concentration was 2ppm. The Arrhenius plot of the growth rate of the Si layer is shown in Fig. 2. The growth rate increases linearly with temperature until 950℃ and the activation energy calculated from the slope in Fig.2 is about 52Kcal/mol. The growth rate of the Si epitaxial layer increases slowly when the temperature is higher than 950℃ and the activation energy in this regime is about 7 Kcal/mol. The apparent variation of the activation energy is due to different growth mechanisms. At high temperatures, the growth rate is a weak function of temperature and the reaction is mass transport limited. At low temperatures, the growth rate decreases exponentially with decreasing deposition temperature and reaction is surface reaction limited. The transition between the regimes occurs between 900℃-950℃. The quality of the deposited film is strongly dependent on temperature. The film quality is monocrystalline when the temperature is higher than 950℃. It becomes polycrystalline when the temperature is lower than 850℃.

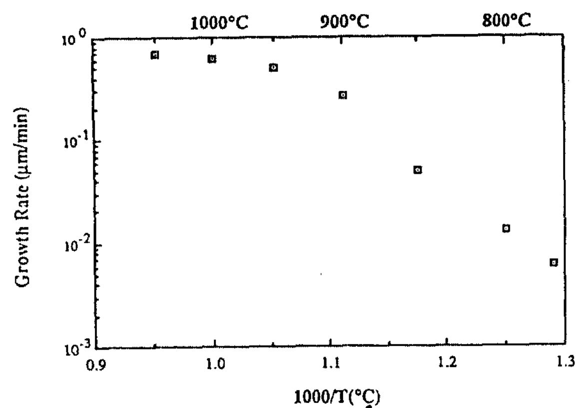


Fig. 2. Arrhenius growth rate relation for $SiH_2Cl_2$ / $AsH_3$ /$H_2$ system.

Excellent selectivity was achieved for polysilicon films deposition from 2% vol $SiH_2Cl_2$ in hydrogen at 6 torr and a total flow of 1000sccm. The SEM micrographs of samples processed at 775℃ and 850℃ are shown in Figs. 3. No deposition and local nucleation were observed on the $SiO_2$ surfaces even without the addition of HCl, due to the fact that the chlorine from $SiH_2Cl_2$ tends to etch away silicon atoms loosely adsorbed on the oxid surface. The average polysilicon grain size is 0.03μm at 775℃ and increases to 0.2μm at 850℃, indicating a significant increase in grain size at higher temperatures. Due to the precise control of temperature, time, and gas composition, the thickness of deposited polysilicon film can be controlled very accurately with excellent selectivity.

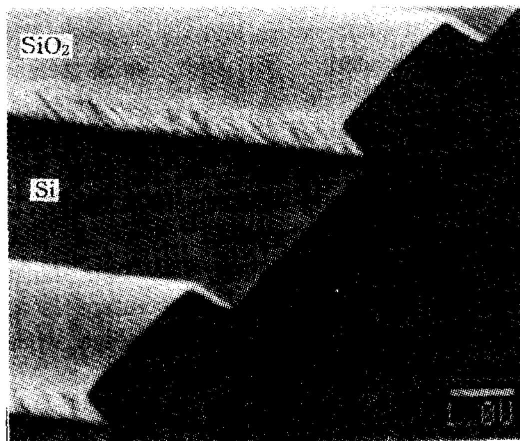


Fig. 3(a). SEM micrograph of oxide line pattern before polysilicon deposition.

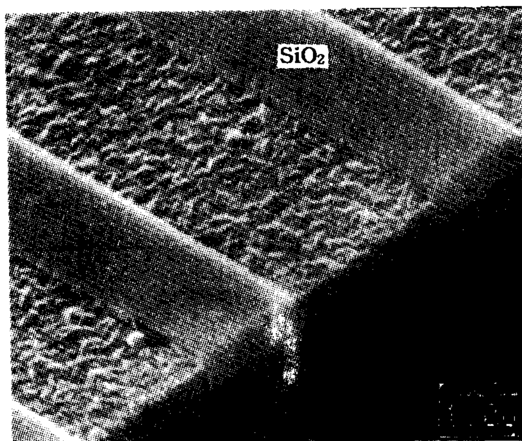


Fig. 3(b). SEM micrograph of polysilicon interconnect lines after 775℃ deposition.

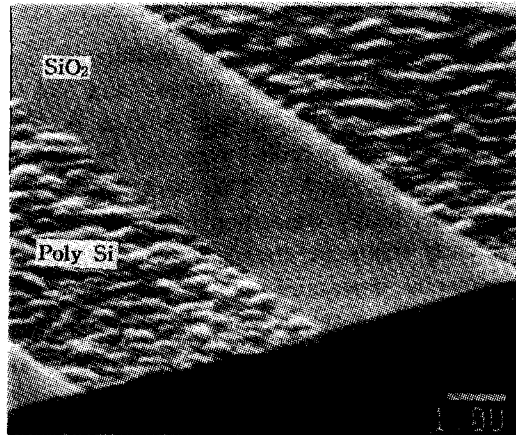


Fig. 3(c). SEM micrograph of polysilicon interconnect lines after 850℃ deposition.

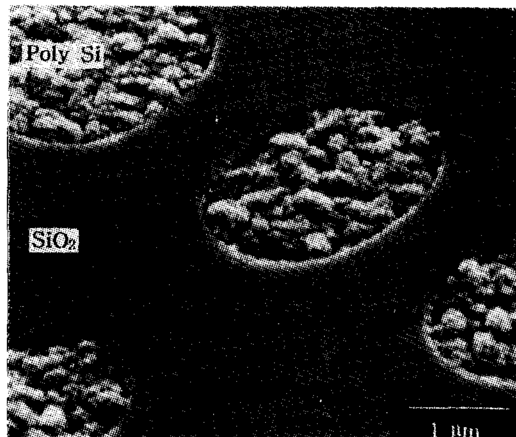


Fig. 3(d). SEM micrograph of polysilicon contact fills after 850℃ deposition.

The polysilicon deposition rate as a function of arsine mole fraction is shown in Fig. 4. The growth conditions were 5% vol $SiH_2Cl_2$ in hydrogen at 6 torr for 1min at 800℃ and for 1 min at 900℃. The film thickness decreases as doping level increases. When the arsine mole fraction is higher than 5ppm, the growth rate decreases rapidly. Our result show that the decrease of growth rate appears most dramatically at high doping levels, which is in

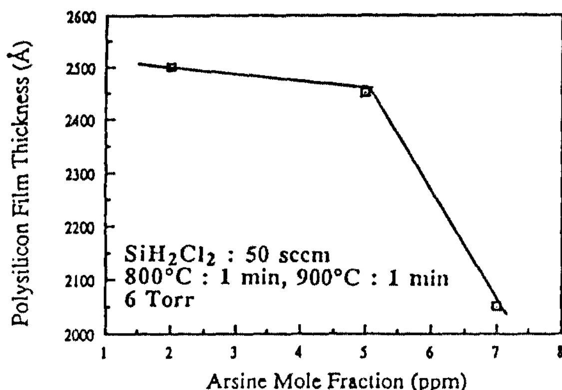


Fig. 4. Dependence of doped polysilicon film thickness on arsenic mole fraction.

good agreement with previously reported data for conventional thermal CVD[3]. The decrease in growth rate indicates the inhibiting of polysilicon growth by the incorporation of arsine. The inhibited growth has been attributed to preferential adsorption of the arsenic species on the silicon and subsequent decomposition of dichlorosilane.

The polysilicon decomposition rate as a function of $SiH_2Cl_2$ flow rate is shown in Fig. 5. The film thickness increases linearly with $SiH_2Cl_2$ flow rate. This trend is similar to that obtained under standard LPCVD conditions at low flow rates, because more of the surface is being covered by $SiH_2Cl_2$. However, the growth rate did not reach the saturation point even when the $SiH_2Cl_2$ flow rate was 150sccm (15% vol). A possible reason for the lack of growth rate saturation is the preferential adsorption of arsine on the silicon surface, which inhibits polysilicon growth. Therefore, a higher $SiH_2Cl_2$ flow rate is required to reach the growth rate saturation point.

The main issues in these applications which involve a doped layer of polysilicon directly on Si and a drive-in process are the dopant redistribution in the single crystal silicon and polysilicon layers[4] and the morphology of the interfacial layer between the polysilicon layer and silicon substrate after the high temperature anneal[5].

Dopant redistribution is a complicated process in polysilicon on silicon structures. The polysilicon grain boundaries provide fast diffusion paths for redistribution[6], and the interfacial layer can influence the dopant segregation and transport across the interface[7]. The dopant-induced enhancement of solid-phase epitaxy and the grain growth due to silicon self-diffusion across grain boundaries make the diffusion process even more complicated. It has been shown that in the early stages of the anneal, the grain boundary movement is the major mechanism by which dopants transfer from the grains tothe grain boundaries[8].

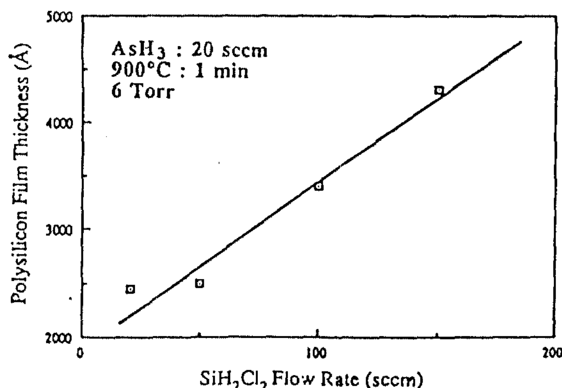


Fig. 5. Dependence of doped polysilicon film thickness on $SiH_2Cl_2$ flow rate.

The interface between polysilicon and silicon acts as a high diffusivity grain boundary. The dopants can rapidly redistribute along the boundaries before diffusing into the silicon substrate. Hoyt et al. [9] found that the lateral distribution of diffusion front is very uniform, even though the anneal caused nonuniform breakup of the interface and partial alignment of the polysilicon.

The arsenic profiles of as-deposited samples measured by SIMS using 10KeV $Cs^+$ ions at several growth temperatures are shown in Fig. 6. The samples underwent the same processing conditions except for the difference in the deposition temperature and time, resulting in different polysilicon film thickness.

The main features of the dopant profiles show the arsenic distributions exhibited pile-up phenomena with the peak position at the polysilicon/silicon interface as well as at the surface. The As interface peak shows broadening due to the roughness of the polysilicon surface and the depth resolution of SIMS. The interface position was also identified by XTEM and the result were consistent with the SIMS results. The arsenic concentration was not uniform within the polysilicon layer. The arsenic concentration was much higher at the polysilicon/silicon interfase and at the surface. The dopant redistribution mechanism can be explained in terms of grain growth and grain boundary diffusion. The pile-up of As at the interface may be interpreted as an indication of grain boundary segregation or as trapping of As within the interfacial region caused by oxygen and other impurities present at the interface.

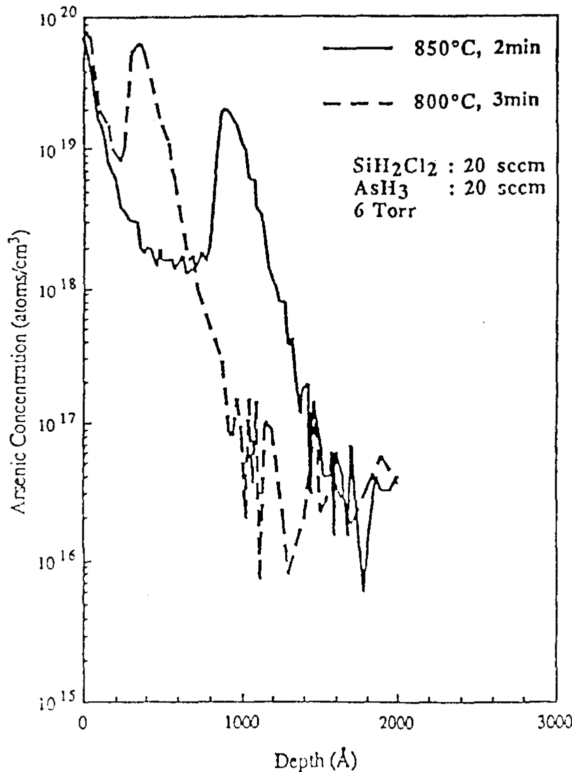


Fig. 6. The arsenic concentration profiles of as-deposited samples from 2% vol $SiH_2Cl_2$ and 2ppm $AsH_3$

The oxygen profiles of as-deposited samples measured by SIMS show small peaks at the polysilicon/silicon interface. We suspect that they are unremoved oxides after HF dip and hydrogen pre-bake step and reoxidation of the silicon surface between the hydrogen pre-bake step and polysilicon deposition. To verify this some samples with the same preparation procedures was deposited at temperatures higher than 950℃. But compared with the SIMS data of epitaxial growth single crystal silicon in Fig. 7, the arsenic profiles do not show any peak at the interface. So the pile-up phenomenon is mainly due to the As segregation at the interface. The arsenic concentration of the polysilicon layer is higher at lower temperatures, which is in good agreement with previously reported data[10]. The temperature dependence of the As segregation at the interface is shown in Fig. 8. The As concentrations decrease with temperature increase. From the figure, we can see a transition around 900℃ and it indicated different segregation mechanism at different temperature region.

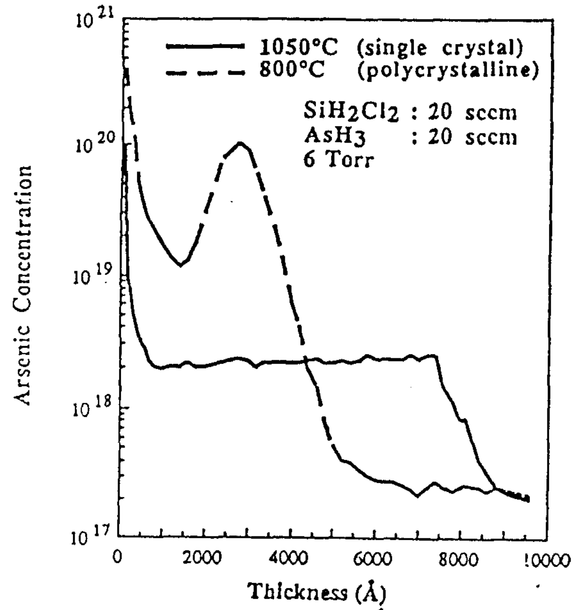


Fig. 7. The arsenic concentration profiles of as-deposited samples from 5% vol $SiH_2Cl_2$ and 5ppm $AsH_3$.

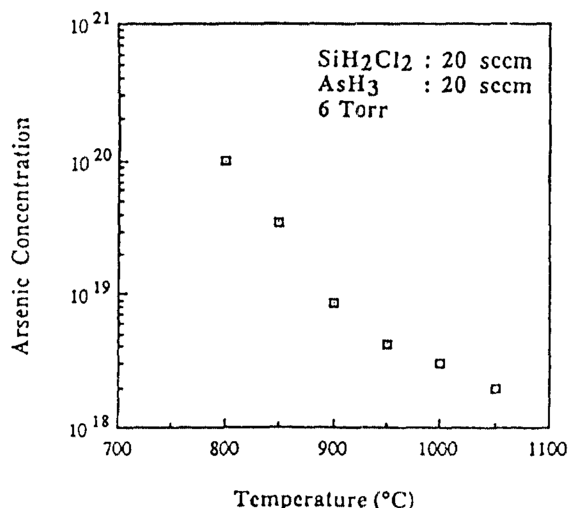


Fig. 8. Dependence of arsenic concentration at polysilicon/silicon interface on deposition temperature.

We attributed the phenomena to the different crystallinity due to different deposition temperature. The arsenic segregates at the silicon surface due to the lower surface energy. The segregation effect is also supported by the calculation using the Ising-like model[11]. The dopant profiles show the arsenic concentration drops from $10^{19}cm^{-3}$ to $10^{17}cm^{-3}$ within 35nm in Si. Extremely shallow $n^+$-p junctions were obtained using RTPCVD. The arsenic already diffused into the silicon substrate for the as-deposited sample due to the high temperature deposition process. The dopant redistribution is complicated because deposition and diffusion occur at the same time. The elevated temperature process also causes grain growth and enhanced grain boundary diffusion.

The as-deposited samples were subjected to rapid thermal annealing(RTA) in the temperature range of 1000℃ - 1100℃ for times of 15 - 60 seconds to drive in dopants. The XTEM samples were prepared by $Ar^+$ ion milling to electron transparency and examined in a JEOL 200CX microscope at an accelerating voltage of 200KeV. The arsenic diffusion front was delineated by chemical etch in a solution consisting of 0.3% HF in $HNO_3$. The etching solution etches faster in the heavily arsenic-doped substrate than the lightly doped silicon substrate.

The XTEM image contrast will change due to dopant concentration, sample thickness, concentration of etching solution, and etching time. As a result, the lateral uniformity of the diffusion front can be examined. Fig. 9 is a XTEM micrograph after junction delineation. A partial realignment was observed in the top polysilicon layer with twinning and hairpin dislocations. The nonuniform breakup of the polysilicon/silicon interface can also be seen. Two bright delineated regions on both sides of the polysilicon/silicon interface can be seen running parallel to the interface as shown in Fig. 10. The delineated region at the silicon substrate shows the diffusion front. The diffusion front corresponds to an arsenic concentration of 5 × $10^{18}$ $cm^{-3}$. The diffusion front is very uniform regardless of the nonuniformities of the top polysilicon layer. This indicates that the arsenic rapidly and uniformly redistributes along the interface before diffusing into the silicon substrate. The delineated region at the polysilicon layer shows the arsenic concentration region at the polysilicon layer, and the results are in good agreement with SIMS result.

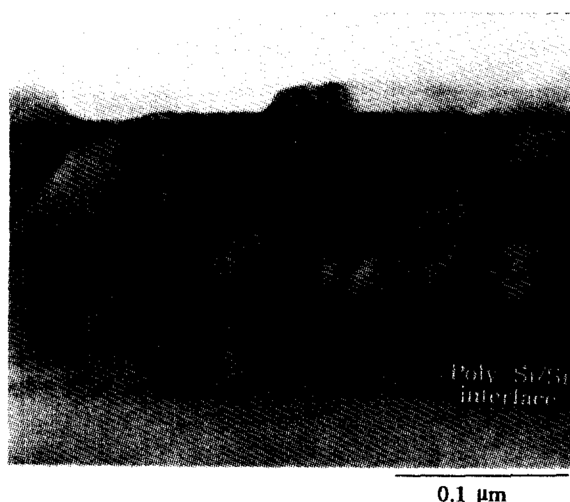


Fig. 9. XTEM micrograph shows the partial realignment of polysilicon layer and the breakup of the polysilicon/silicon interface after 1100℃, 15s anneal.

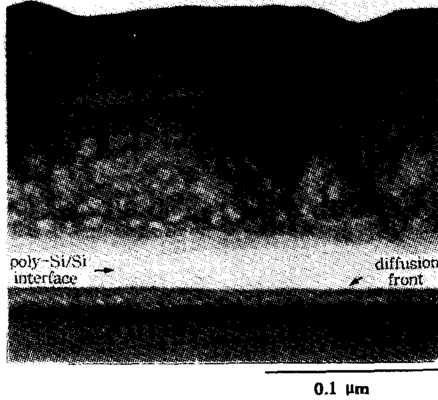


Fig. 10. XTEM micrograph shows the diffusion front after 1000℃, 20s anneal.

## 4. Conclusions

We have demonstrated the capability of RTPCVD to grow *in-situ* heavily doped polysilicon for shallow junction formation. The growth kinetics of the $SiH_2Cl_2/AsH_3/H_2$ system has been studied and results show that the inclusion of arsine can inhibit the growth rate. The deposited film quality is polycrystalline when the deposition temperature is lower than 850℃. Excellent selectivity was achieved by proper conditions. The growth rate decreased as doping levels increased, and drastically decreased when the arsine mole fraction was higher than 4ppm. The growth rate was linearly proportional to the $SiH_2Cl_2$ flow rate for fixed arsine flow rate. The dopant concentration was higher when the deposition temperature was lower. The dopant transition width was about 40nm to 50nm. Extremely shallow $n^+$-p junctions were achieved using RTPCVD and laterally uniform delineated juntions were also observed.

## References


1. J. F. Gibbons, C. M. Gronet, and K. E. Williams, Appl. Phys. Lett., **47**, 721 (1985)
2. R. Singh, J. Appl. phys., **63**, R59 (1988)
3. J. H. Comfort and R. Reif, Proceedings of the Tenth International Conference on Chemical Vapor Deposition, **PV 87-8** (1987)
4. M. Arienzo, Y. Komen, and A. E. Michel, Appl. Phys., **55**, 365 (1984)
5. C. Y. Wong, A. E. Michel, R. D. Isaac, R. H. Kastl, and S. R. Mader. J. Appl. Phys., **55**, 1131 (1984)
6. B. Swaminathan, K. C. Saraswat, R. W. Dutton, and T. I. Kamins, Appl. Phys. Lett., **40**, 795 (1982)
7. B. Swaminathan, E. Demoulin, T. W. Sigmon, R. W. Dutton, and R. Reif, J. Electrochem. Soc., **127**, 2227 (1980)
8. A. G. O'Neill, C. Hill, J. King, and C. Please, Appl. Phys., **64**, 167 (1988).
9. J. L. Hoyt, E. F. Crabbe, R. F. W. Pease, J. F. Gibbons, and A. F. Marshall, J. Electrochem. Soc., **135**, 1773 (1988).
10. J. Borland, T. Thompson, V. Tagle, and W. Benzing, Proceedings of the Tenth International Conference on Chemical Vapor Deposition, **PV 87-8** (1987)
11. Mohammad M. Mandurah, Krishna C. Saraswat, and C. Robert Helms, J. Appl. Phys., **51**, 5755 (1980).