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〈연구논문〉

Subthreshold Characteristics of Poly-Si Thin-Film Transistors Fabricated by Using High-Temperature Process

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고온공정으로 제작된 다결정실리콘 박막 트랜지스터의 서브트레시홀드 특성

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Abstract – The subthreshold characteristics of polycrystalline silicon (poly-Si) thin-film transistors (TFTs) fabricated by using high-temperature process, including solid phase crystallization of amorphous Si and thermal oxidation of poly-Si, have been studied. The devices show high performances with a field effect mobility higher than 60 $cm^2/V \cdot s$ and a subthreshold swing lower than 0.65 V/decade. However, the threshold voltages of the devices are strongly shifted toward the negative gate voltage and there are prominent differences in the subthreshold characteristics of the n-channel and p-channel poly-Si TFTs. The subthreshold characteristics of the poly-Si TFTs with thermally grown gate oxide was modeled by traps in the bandgap of poly-Si active layer and fixed charge density at the interface between gate oxide and poly-Si. Simulation showed that the proposed trap model of poly-Si could explain the experimental results very well.

요 약 – 비정질실리콘의 고상결정화 및 다결정실리콘의 열산화를 포함한 고온공정으로 제작한 다결정실리콘 박막 트랜지스터의 서브트레시홀드 특성을 연구하였다. 제작된 소자의 전계효과이동도는 60 $cm^2/V \cdot s$ 이상, 서브트레시홀드 스윙은 0.65 V/decade 이하로 전기적 특성이 매우 우수하다. 그러나, 소자의 문턱전압이 음게이트전압으로 크게 치우쳐 있으며 n-채널과 p-채널 소자간의 서브트레시홀드 특성이 크게 다르다. 열성장된 게이트 산화막을 가진 다결정실리콘 박막 트랜지스터의 서브트레시홀드 특성을 다결정실리콘 활성층내의 트랩과, 게이트산화막과 다결정실리콘 사이의 계면 고정전하를 이용하여 모델링하였다. 시뮬레이션을 통하여 제안된 다결정실리콘의 트랩모델이 실험결과를 잘 설명할 수 있음을 확인하였다.

1. Introduction

Polycrystalline silicon (poly-Si) thin-film transistors (TFTs) have attracted much attention for high-resolution active matrix liquid crystal display (AMLCD) [1]. The peripheral circuits of AMLCD can be integrated with poly-Si TFT because it has much higher field effect mobility than amorphous silicon (a-Si) TFT. A p-channel poly-Si TFT has also been used instead of poly-Si resistor in order to obtain a high charging current and a low leakage current in 4 Mbit or higher density static random access memory (SRAM) [2].

The performance of poly-Si TFTs is strongly in-

fluenced by grain boundaries and intragranular traps of the poly-Si active layer. Hydrogen passivation of grain boundaries [3] and solid phase crystallization (SPC) of a-Si [4] have been used to improve the performance of poly-Si TFTs. Recently, it was reported that the characteristics of poly-Si TFTs were greatly changed by oxygen-treatments, such as O_2 annealing (thermal oxidation) of SPC-poly-Si [5] or oxygen-plasma exposure of devices [6]. It is believed that oxygen atoms themselves, like hydrogen atoms, passivate the grain boundary traps of poly-Si. Also, the oxygen-plasma exposure was used to lower the crystallization thermal budget before a-Si crystallization [7]. The oxygen-treatments during or after the fabrication of poly-Si TFTs resulted in the predominant increase of field effect mobility.

In this paper, the effects of thermal oxidation of the poly-Si active layer on the performances of n-channel and p-channel TFTs have been studied. It was found that the devices exhibited an anomalous shift of threshold voltage toward the negative gate voltage and predominantly different subthreshold characteristics between n-channel and p-channel while the field effect mobilities of both devices are high. The subthreshold characteristics, including the threshold voltage, of the devices was modeled by the deep traps in the bandgap of the poly-Si active layer and the fixed charge density at the interface between gate oxide and poly-Si.

2. Experiments and Results

The structure of the poly-Si TFTs used in the experiments is coplanar. The fabrication sequence is as follows. Amorphous Si films of 800 Å thickness were deposited on 5-inch quartz wafers by low-pressure chemical vapor deposition (LPCVD) using Si_2H_6 at 470 ℃. These films were annealed at 590 ℃ for 20 h for crystallization, resulting in poly-Si with grain sizes of 2 ~ 4 μm in diameter. After the poly-Si active layer was patterned, a gate

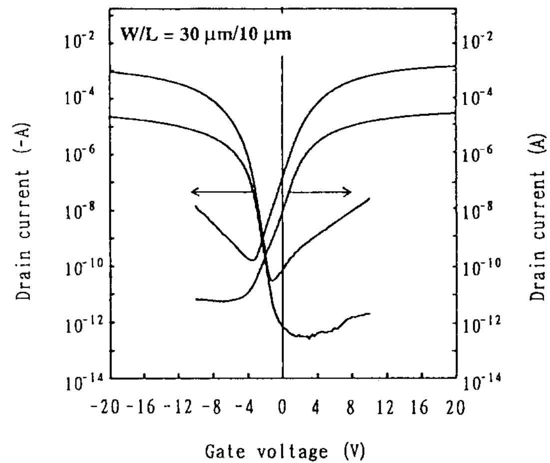

Fig. 1. Drain current versus gate voltage characteristics at different drain voltages (V_d) for n-channel and p-channel poly-Si TFTs. The upper (lower) curve of each channel is at a drain voltage, $|V_d|$=5.0 V (0.1 V).

oxide of 430 Å was grown by dry thermal oxidation at 900 ℃. The thickness of the active layer was decreased to be of 600 Å after thermal oxidation. A 3000-Å-thick poly-Si gate was deposited by LPCVD, and then the gate was patterned. In order to form the source, drain and gate regions, arsenic ions with an energy of 110 keV for n-channel and BF_2 with an energy of 70 keV for p-channel were implanted at a dose of $5 \times 10^{15}/cm^2$ each. Passivation oxide layer of 7000 Å thickness was deposited by LPCVD at 420 ℃ and then the implanted ions were activated by thermal annealing at 920 ℃ for 30 min. After metallization, the samples were alloyed at 420 ℃ for 30 min in forming gas of N_2 and H_2. The maximum temperature in the fabrication process is 920 ℃ for dopant activation of the implanted ions.

Fig. 1 shows the drain current versus gate voltage (I_d-V_g) characteristics at different drain voltages (V_d) for the n-channel and p-channel poly-Si TFTs. The channel width and length, drawn on the photomask, of the measured devices are 30 μm and 10 μm, respectively. These values are 5 to 10 times larger than the grain size of the poly-Si. Both n-channel and p-channel poly-Si TFTs ex-

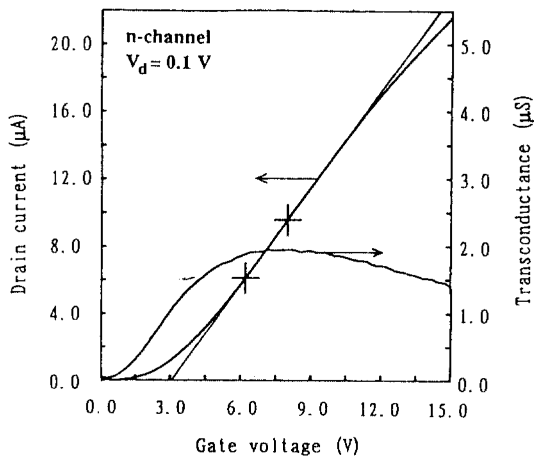

Fig. 2. Transconductance and drain current versus gate voltage in linear plot for n-channel TFT.

hibit excellent subthreshold characteristics while the I_d-V_g curves shift toward the negative gate voltage from zero value.

Fig. 2 shows the linear plots of the transconductance ($=\Delta I_d/\Delta V_g$) and the drain current versus gate voltage at a drain voltage of 0.1 V for the n-channel device. The behavior of the transconductance is similar to that of the single-crystalline Si (c-Si) metal-oxide-semiconductor field effect transistor (MOSFET). The linearity of the drain current is well satisfied while the threshold voltage is somewhat large. These results indicate that the local effects of poly-Si grain boundaries were low and the device parameters could be extracted by the similar way in c-Si MOSFET. The estimated trap density at grain boundaries from the Levinson's method [8] is below $1\times10^{12}/cm^2$.

The characteristic parameters of the n-channel and p-channel poly-Si TFTs without post-hydrogenation are summarized in Table 1. The field effect mobility is calculated from the transconductance in the linear region. The threshold voltage is defined as a gate voltage at which the drain current slope intersects the gate voltage axis at $|V_d|=0.1$ V. Both devices have high performances with a field effect mobility above 60

Table 1. Characteristic parameters of n-channel and p-channel poly-Si TFTs

Parameter	N-channel	P-channel
Field effect mobility ($cm^2/V\cdot s$)	85	62
Subthreshold swing (V/decade)	0.61	0.46
Threshold voltage (V)	2.4	−5.7
Leakage current (pA)	13.0	−5.2
ON/OFF ratio	10^7	10^7

$cm^2/V\cdot s$, a subthreshold swing below 0.65 V/decade, and an ON/OFF ratio above 10^7. However, there appear some differences in the threshold voltage and the subthreshold swing of the n-channel and p-channel devices. The subthreshold slope of the p-channel poly-Si TFT was steeper than that of the n-channel device. The threshold voltages of both devices were anomalously shifted toward the negative gate voltage. Also, as shown in Fig. 1, the separation of the I_d-V_g curves with V_d in the subthreshold region was observed for only n-channel device, which was caused by the threshold voltage reduction with V_d. These asymmetrical characteristics between n-channel and p-channel devices make it difficult to use the poly-Si TFTs including the thermal oxidation process for complementary metal-oxide-semiconductor (CMOS) circuit applications in which the threshold voltages of both n-channel and p-channel TFTs must be adjusted simultaneously. It requires an additional process to control the threshold voltage, such as ion implantation into the device channel. We should note that the asymmetrical behaviors in the subthreshold characteristics of n-channel and p-channel poly-Si TFTs are not observed for the devices without thermal oxidation process [9].

Our experimental results agree partially with those of Chern [6] and Yin [7]. The former used a thermal oxidation process for the gate insulator formation and the oxygen-plasma exposure for the passivation of grain boundary traps. The latter applied the oxygen-plasma exposure for lowering thermal budget of a-Si crystallization. The ne-

gative threshold voltage shift could be observed in their data, even though for only n-channel device.

3. Modeling and Simulation

Threshold voltage, V_{TH} of poly-Si TFT consists of the ideally defined threshold voltage, V_{THO} and the nonideality-related flat band voltage, V_{FB} [10].

$$V_{TH} = V_{THO} + V_{FB} \tag{1}$$

Also, the nonideality-related flat band voltage could be written as the following equation.

$$V_{FB} = \Phi_{MS} - Q_F/C_{OX} - Q_{IT}/C_{OX} - Q_T/C_{Si} \tag{2}$$

where Φ_{MS} is the workfunction difference between gate electrode and active layer, Q_F is the fixed charge density in gate oxide, Q_{IT} is the interface trap charge density, C_{OX} is the gate oxide capacitance per area, Q_T is the trap density near the midgap of poly-Si active layer, and C_{Si} is the equivalent capacitance of trap density in poly-Si. In Eq. (2), the mobile charge effect is neglected due to the chlorine neutralization by introducing TCA (TriChloroethAne: $C_2H_3Cl_3$) during the growth of the oxide layer.

In this experiment, the threshold voltage shift, ΔV_{TH} defined as the difference of the absolute threshold voltage between n-channel and p-channel devices is very large, nearly larger than 3.0 V. Considering Eq. (2), ΔV_{TH} is mainly caused by Q_F and Q_T if the interface trap density is uniform in the bandgap of poly-Si. The workfunction difference in Eq. (2) does not contribute to the threshold voltage shift because the gate poly-Si has the same doping type as the channel majority carrier. If the fixed charge density which can not be exactly estimated for poly-Si TFTs is assumed to be of about $(1\sim5)\times10^{11}/cm^2$, ΔV_{TH} lies in 0.4 to 2.0 V. This value is much smaller than the experimental one. Furthermore, the fixed charge density can not cause the difference in the subthreshold swings of n-channel and p-channel poly-Si

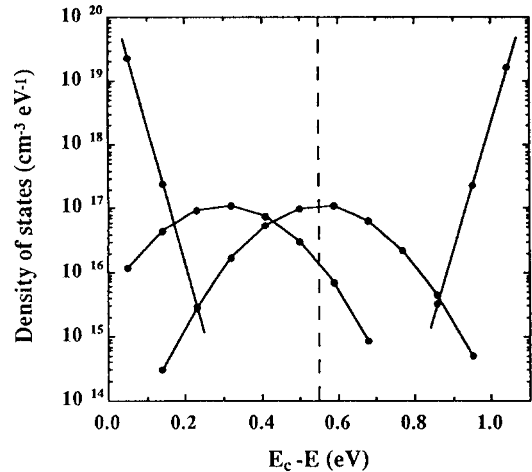

Fig. 3. Density of states (DOS) model of the poly-Si active layer. The dotted line indicates the midgap of poly-Si. The peaks of acceptor-like and donor-like deep states lie at 0.30 eV and 0.55 eV below the conduction band edge, respectively.

TFTs. Therefore, in order to explain the experimental data we must consider the effect of the traps in the poly-Si active layer and/or the interface traps on the subthreshold characteristics of the devices. We focused on the traps in the poly-Si active layer rather than the interface traps because oxygen atoms strongly affected the electronic properties of poly-Si film [5-7]. It is well known that the deep traps in the bandgap of poly-Si greatly influence the subthreshold characteristics of the devices [11]. We assume that the deep traps of poly-Si have an asymmetric distribution relative to the midgap with thermal oxidation process.

Fig. 3 shows the proposed density of states (DOS) model of the poly-Si active layer for case of the TFTs with thermally grown gate oxide. The band tail states have exponential distributions with a characteristic slope of about 20 meV. The deep traps near the midgap of poly-Si are composed of acceptor-like and donor-like states with gaussian distributions. We mainly changed the deep trap energy level to fit both n-channel and p-channel subthreshold characteristics. Simulation was per-

formed by using a 2-dimensional device simulator with effective medium approach, whereby the traps and grain boundaries are treated as a spatially uniform density of localized states in the bandgap. While this effective medium approach may not be suitable for the detailed analysis of the local field dependent characteristics such as leakage currents in poly-Si TFTs, it does enable us to model realistically the subthreshold characteristics of the devices [12]. Shockley-Read-Hall kinetics accounts for the carrier capture and emission processes.

Fig. 4 shows the simulated subthreshold characteristics with the experimental data for both n-channel and p-channel TFTs. We assume the fixed charge density to be $5\times10^{11}/cm^2$. The solid line was obtained with the poly-Si DOS shown in Fig. 3. The gaussian peaks of acceptor-like and donor-like states with a characteristic decay energy of 0.17 eV lie at 0.30 eV and 0.55 eV below the conduction band edge, respectively. The dotted line was the simulated results with the symmetric trap distribution relative to the midgap of poly-Si. The acceptor-like and donor-like deep states was located at 0.125 eV above and below the midgap of poly-Si, respectively. The simulated results with the asymmetric trap distribution are in good agreement with the experimental data while the drain currents at larger gate voltages are slightly different from the experimental values due to the lack of vertical electric field degradation of field effect mobility in the simulation. It is specifically noted that we can not achieve the proper fittings to experiments with the only fixed charge density. This result indicates that the different subthreshold characteristics between n-channel and p-channel poly-Si TFTs arise from the asymmetric distribution of the deep traps in the poly-Si active layer.

The proposed DOS of poly-Si may also explain the threshold voltage shift with V_d in the subthreshold region for the n-channel TFT. This phenomenon was hardly observed for the p-channel device. It was demonstrated by Hack and Lewis [13] that grain boundaries and traps in the poly-Si active layer significantly enhance the kink effect in poly-Si TFTs and reduce the threshold voltage with drain voltage. Although both n-channel and p-channel TFTs have same poly-Si active layer, the traps themselves and their distribution in the bandgap of poly-Si can give rise to the difference in the kink effect and the threshold voltage dependence on drain voltage.

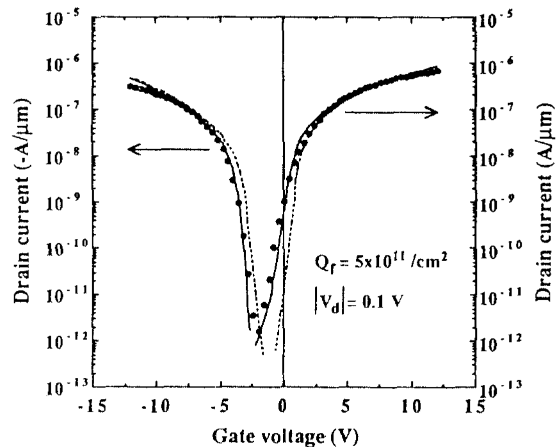

Fig. 4. Comparison of simulated subthreshold characteristics with experimental data (●) for n-channel and p-channel poly-Si TFTs. The solid line represents the simulated results with the DOS shown in Fig. 3. The dotted line is the simulation results using the symmetric distribution of the deep traps relative to the midgap of poly-Si.

The traps in the poly-Si bandgap mainly consist of the bandtail states originated from the distorted atomic bonds in grains and on their boundaries, and the deep states originated from the broken bonds, named dangling bonds, located at the grain boundaries. The thermal oxidation process for the gate dielectric formation reduces the inter- and intra-grain traps in poly-Si, so that the total trap density prominently decreases and the device with this process has high performances. However, our model reveals that the thermal oxidation reduces the traps more at the low energy level than the high level relative to the midgap, resulting in the

asymmetric distribution of the deep traps in poly-Si and the different subthreshold characteristics between n-channel and p-channel TFTs. The physical origin of the passivation of poly-Si traps by thermal oxidation is rather sophisticated. In general, thermal annealing, diffusion of oxygen into poly-Si, and interface formation effects are involved in thermal oxidation process. They all affect the trap distributions in the bandgap of poly-Si after the thermal oxidation. The detailed mechanism needs further studies.

4. Conclusion

We have presented a DOS model to explain the subthreshold characteristics of the poly-Si TFTs having thermally grown gate oxide. The proposed model could explain the experimental data for both n-channel and p-channel devices. The different subthreshold characteristics between n-channel and p-channel TFTs and the shift of threshold voltage toward the negative gate voltage are caused by the asymmetric distribution of the deep traps in the poly-Si active layer with the fixed charge density in the gate oxide. We suggest that the deep trap passivation in poly-Si by thermal oxidation is more favorable at the low energy level than at the high level relative to the midgap, resulting in the asymmetric trap distribution in the bandgap of poly-Si.

References

1. S. Morozumi, K. Oguchi, T. Misawa, R. Araki, and H. Ohshima, *SID International Digest of Technical Papers* (Society for Information Display, Philadelphia, 1983), p. 316.
2. T. Yoshida, M. Kinugawa, S. Kanbayashi, S. Onga, M. Ishihara and Y. Mikata, *Technical Digest of IEDM* (IEEE, Washington DC, 1991), p. 23.
3. I.-W. Wu, A. G. Lewis, T.-Y. Huang and A. Chiang, IEEE Electron Device Lett. **EDL-10**, 123 (1989).
4. R. B. Iverson and R. Reif, J. Appl. Phys. **62**, 1675 (1987).
5. Y. Fukushima, T. Ueda and H. Komiya, *Extended Abstracts of the 1993 International Conference on Solid State Devices and Materials* (The Japan Society of Applied Physics, Makuhari, 1993), p. 993.
6. H. N. Chern, C. L. Lee and T. F. Lei, IEEE Electron Device Lett. **EDL-14**, 115 (1993).
7. A. Yin and S. J. Fonash, *Technical Digest of IEDM* (IEEE, Washington DC, 1993), p. 397.
8. J. Levinson, F. R. Shepherd, P. J. Scanlon, W. D. Westwood, G. Este and M. Rider, J. Appl. Phys. **53**, 1193 (1982).
9. Y.-H. Song, B.-G. Yu and K.-S. Nam, Korean Appl. Phys. **7**, 318 (1994).
10. R. F. Pierret, *Field Effect Devices (2nd edition) in Modular Series on Solid State Devices*, edited by G. W. Neudeck and R. F. Pierret (Addision-Wesley Publishing Company, USA, 1990), Chap. 4.
11. I.-W. Wu, T.-Y. Huang, W. B. Jackson, A. G. Lewis and A. Chiang, IEEE Electron Device Lett. **EDL-12**, 181 (1991).
12. M. Hack, A. G. Lewis and I.-W. Wu, IEEE Trans. Electron Dev. **ED-40**, 890 (1993).
13. M. Hack and A. G. Lewis, IEEE Electron Device Lett. **EDL-12**, 203 (1991).