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MULTI-CHANNEL REMOTE SENSING CCD CONTROLLER DESIGN WITH MULTIPLEXING CONCEPT

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ABSTRACT

We present a design study for a remote sensing camera system which can be operated in multi-channel mode simultaneously with several bandpass filters. The camera control electronics is based on the multiplexed driving concept, which can provide a variety of flexibility for system control parameters and its individual optimisation. The design can also be applied to any system with linear sensors or frame sensors according to its functional requirements. The system design parameters have been examined, including modification of driving waveforms for different types of sensors, waveforms for low-noise readout circuit in analog chain, and synchronisation with other signal processing.

1. INTRODUCTION

In recent remote sensing camera systems, CCDs are widely employed to obtain images in visible and near-infrared spectral bands. Microprocessors are often very useful to provide necessary waveforms and other relevant signals to control CCDs. However when a large number of CCDs are involved in the system design, it is not always simple to control all the CCDs together efficiently either in hardware or in software development. With recent technology development, the controller for multiple CCDs can be implemented directly by the digital logic design with a CAD system. The control of multiple CCDs is not a new approach in astronomical purposes particularly for a larger sensing area (Leach and Denune 1994, Reiss 1994, Han *et al.* 1994). In some cases of remote sensing camera system, multiple CCDs are used to collect image data with several spectral bands simultaneously.

The whole remote sensing camera system consists of several subsystems such as optics, sensors and focal plane, bus interface, mass storage, data transmission system, *etc.* In this

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paper, we mainly focus our discussion on the CCD camera controller design and other related electronics. One of the main functions of the CCD controller is to supply appropriate digital waveforms for several CCDs efficiently. The principal idea to produce multiple waveforms for each CCD is to multiplex the digital waveforms in interleaving manner so that they can be distributed to associated CCDs. Then the digital waveforms are converted to analog forms which are directly connected to the CCDs in analog circuitry. The multiplexing concept can be implemented by a software programming or by hardware design directly, according to the design efficiency and functional requirements. Both approaches have been examined here, and its design concept is suggested for a multi-channel remote sensing application.

2. DESIGN CONSIDERATIONS

Considering its operational environment, the design of the CCD camera controller for remote sensing applications requires particular attention compared to any other applications such as astronomical purposes. Once the system launched and operated in the orbit, it is impossible to replace any components when problems occur in the system. This suggests that the whole system design should be examined thoroughly by functional tests before practical operation, which are often made with the engineering model. Thus the control of the whole system also has to be made in a manner of software downloading than any hardware modulation. Some important factors are discussed as follows that have to be considered in the designing stage of remote sensing camera system.

- Controllability to support multiple CCDs : this is an important factor in the system design for multi-channel application in several spectral bands. Basically each CCD requires its own waveforms and control signals independently. However this requirement possibly needs several duplicated circuitries depending upon the number of CCDs to be employed. Parallel driving of entire CCDs lacks the control flexibility and has the possibility of cross-talk between the devices. Therefore a different approach has to be explored to cope with multiple CCDs efficiently. Multiplexed driving of several CCDs compared to the parallel control, is the key feature in this work.

- Compactness : satellite camera system has an inevitable restriction of its mass and volume in design. The circuit of the controller has to be small enough to fit in the predetermined area and the number of components should be minimised by careful designing. The surface mount devices would be desirable to achieve such system requirements, though not all the electronic components are available.

- Flexibility : the waveforms of a CCD require individual tuning for its best performance even in the case of the same type of devices, particularly for scientific applications. Thus the design should allow flexible drive waveforms according to its functional requirements for each CCDs. This implies the waveforms of any CCD have to be configured independently with the other devices. This requirement can be satisfied by the software-defined waveforms in a form of bit pattern, thus any digital pulse can be defined easily from software. With this technique, it is possible to supply various waveforms and bias signals for multiple CCDs including even different format with mixed devices. It also allows the optimisation of a CCD independently in the focal plane so that all devices can demonstrate its best performances. Apart from the control flexibility of a system, design flexibility can also be secured by employing a CAD system in developing stage because the whole controller design can be easily upgraded by software.

- Operating condition : The existing flight hardware requires strict qualification against the severe operating environment of the controller. Mechanical shocks during the launch and separation from the rocket have to be considered in design (Arian Space 1992). Thermal variation in a satellite should not give any effect during operation of the controller in the orbit, although normally it is designed to maintain within a certain range of temperature. Also there are many kinds of high energy particles in space environment which could give unavoidable damage to the electronic components. Vacuum condition is another factor of concern that could result in 'out gassing' of gaseous materials from the components. This can be critical to the other part of a system, particularly to the optical components of the CCD camera. Considering all of these circumstances, the electronic components have to be carefully selected among space proven specifications.

- Low noise performance : It is generally known that analog signals from the CCDs are very susceptible in noise. Correlated Double Sampling (CDS) techniques have been developed to improve system performance, particularly for astronomical purposes (Leach and Beale 1990). It has been widely used in slow scan operation with relatively longer pixel readout time, however some difficulties are expected for remote sensing applications due to its processing timing constraint. Including this, the system should be designed to allow individual optimisation of each device to achieve its lowest noise performance.

3. MULTIPLEXING FOR REMOTE SENSING APPLICATION

In dealing with simultaneous multiple operation, the most important work in the design would be the waveform arrangement for the devices. Such driving pulses cannot be efficiently provided by parallel driving because this lacks the flexibility and is difficult to support multiple CCDs. Cross talk between the devices is another potential problem when multiband signals are required with several devices *synchronously*, at the cost of compactness and simplicity. Meanwhile separate driving for multiple devices is unacceptable due to intricacy within the limited space of the circuitry in a satellite, particularly when a larger number of CCDs are involved. But in this case, control flexibility is fully guaranteed for all the devices.

Taking advantages of those two approaches, a new technique has been explored. The concept of multiple driving for astronomical mosaic CCDs (Han 1993) can be directly applied to remote sensing applications. Basically, driving concept of multiple CCDs is the same, except processing timing of the image data. The waveforms can be defined in a form of digital bit pattern from the software. This applies not only to a single CCD but to also waveforms for several CCDs that can be specified by the software, then interleaved together to build multiplexed waveforms for several CCDs. Whenever any event is defined for a clocking phase of any CCD, it carries its own CCD address information. One clocking phase requires one digital bit for any number of CCDs but it is discriminated by its own addresses. In this case, the length of the digital bit practically presents one pixel readout time. More details for multiple CCD control have been described by Leach and Denune (1994) and Han *et al.* (1994).

Scanning of the multiplexed waveforms provides necessary digital waveforms for each multiband sensors. The multiplexed waveforms have to be decoded according to the address information to identify the corresponding sensor so that the clocking signals of any phase can be distributed to any specific CCD. Thus such process can be referred as demultiplexing. The timing arrangements for this concept are shown schematically in Figure 1. Particular consideration has to be paid to timing overhead in implementation of this concept for remote sensing application. Practically this is the main difference with the instruments for other application. All multiplexed outputs must be processed and digitised before arriving of the multiplexed signal packet of the next pixel at output port. The difficulty of the timing restriction comes from the sampling and hold speed in CDS (Correlated Double Sampling) of the readout circuit.

Considering such timing restriction, the feasibility of the multiplexing concept have to be examined for other signals, apart from the timing waveforms. The address signals require several bits to be multiplexed, depending on the number of devices. Four digital bits would be enough to decode 16 devices, and it can be applied to practical remote

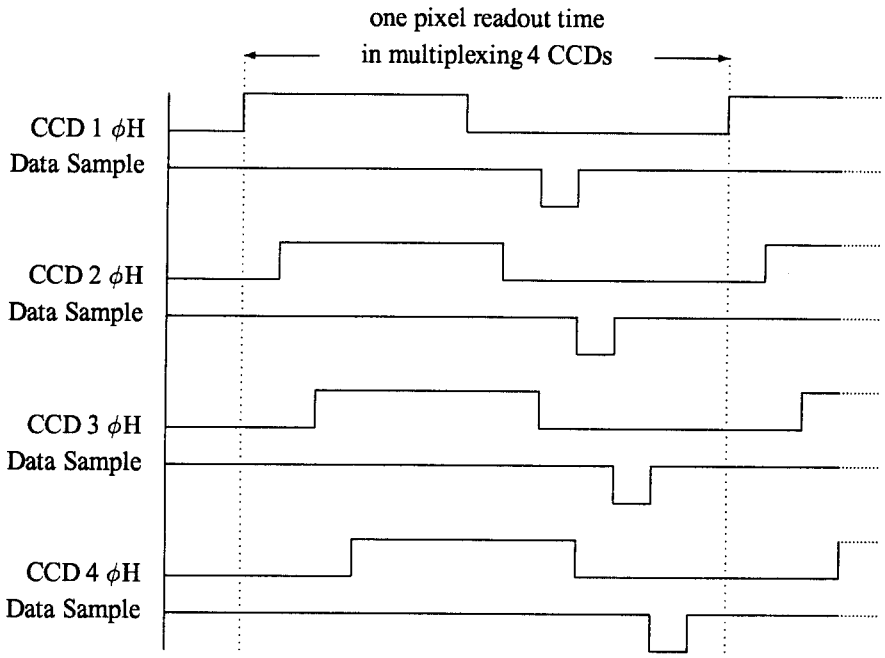

Figure 1. The schematic timing arrangements for the multiplexing concept when virtual phase linear CCDs are employed.

sensing application. These signals are indicators to select proper devices, in digital form. No timing overhead problem arises, however interleaving them in a multiplexed manner determines proper sequence of multiple operation. The trigger signal of ADC (Analog to Digital Convertor) is another critical parameter. Although the signal itself is free from timing overhead due to its digital nature, the conversion time of a ADC has to be carefully considered in design. The experiences of earlier researchers (Leach and Beale 1990, Han 1993) suggest that precise timing arrangement is a key factor in data collection for multiple operation.

The signal chain of CDS timing is one of the primary concerns to multiplex the image signal from the devices. This technique has been developed mainly for long exposure frames in astronomical applications to reduce the system noise. Figure 2 shows typical timing arrangements of CDS. In practice, the processing speed restriction originates from

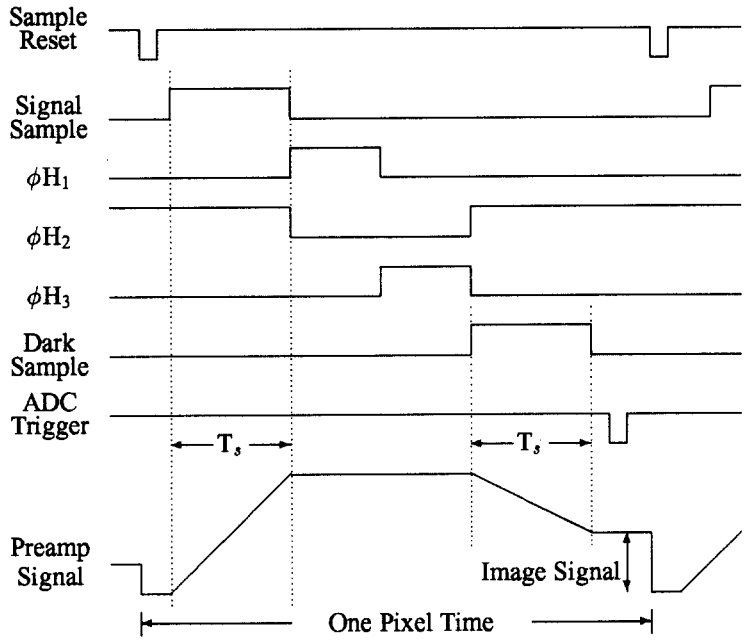

Figure 2. The Timing arrangement for Correlated Double Sampling.

the unavoidable integrator in the sample and holder. More than ten mega pixels per second fast readout circuit will be necessary for future higher resolution and wider width imaging systems (Yoo 1994). Currently one mega pixels per second is commercially available (Datel 1994). The electronics subsystem, including various types of amplifiers, switches and other components in the signal processing chain should not influence system noise and linearity performance. In the case of French remote sensing satellite SPOT, each four output ports within a single channel use separate sample and hold circuits to overcome this processing timing restriction. Having more outputs in a single channel CCD array can be helpful to multiplex image signals. Some manufacturer like EEV support such architecture within a single device in their new series of large linear array (EEV 1992).

4. TWO DESIGN APPROACHES WITH PLD

The system hardware of a CCD camera controller can be implemented with various design approaches. Particularly, a microprocessor provides extensive capability to deal with

many digital video signals efficiently. Recent developments using a DSP (Digital Signal Processor) for the mosaic CCD system design by Leach and Denune (1994), and Reiss (1994) are excellent examples for astronomical use. Another system design approach has also been investigated actively by employing PLDs (Programmable Logic Devices) with an electronic CAD system (Han *et al.* 1994). It preserves most advantages of microprocessor design and offers further flexibility with compactness and predictable timing delays in designing procedure. In Principle, most of the controller digital logic can be integrated into a single PLD chip with some external memory devices. Details of the property with this design approach has been presented elsewhere (Han 1994). Therefore the discussions are focused on the practical implementation of the PLD for remote sensing applications, in other terms, fast signal processing scheme with several multi-channel CCDs.

Currently several CAD software packages are commercially available with PLD logic design facility. The FLEX8000 family PLDs developed recently by Altera Corporation (1994) can integrate more than 20 thousands logic gates into a single device with very high processing speed. Applying this to the controller logic design, high speed digital waveforms can be generated for multiple CCDs. The design concept is basically the same with the recent work demonstrated by Han *et al.* (1994), but the clocking rate has to be increased further for remote sensing applications. In this design, the PLD controller produces external memory address information to define the status of the waveforms (including other relevant signals) at any given moment. The information in memory device contains detailed sequence of instructions during a pixel readout time, downloaded from the software before readout operation. Thus, cycling around the memory device directly generates digital waveforms and relevant signals for multiple CCDs in a multiplexed form. These will be decoded for each CCD just before analog conversion. This can be referred as memory addresser design. The block diagram of the sequencer design is shown in Figure 3, which is the most important logic block in the PLD design.

The control flexibility is secured with this design approach because the operations of the controller is defined by the software during the readout process. Users can send any operational sequences from the ground. The design allows to control many CCDs easily by the multiplexing technique with software. If a large number of CCDs are involved, a difficulty is expected to present the multiplexed waveforms in a form of digital bit pattern (hereafter bitmap) by software. The problem can be arranged by the subroutine that could define waveforms with all related signals in a GUI (Graphic User Interface) format. Such effort is already being made by Kim (1995). This allows to interleave many individual waveforms conveniently for each CCD into a single multiplexed one. External system control and interfacing signals can also be arranged with the same manner. The speed performance in this design is determined by the length of the bitmap for one pixel readout

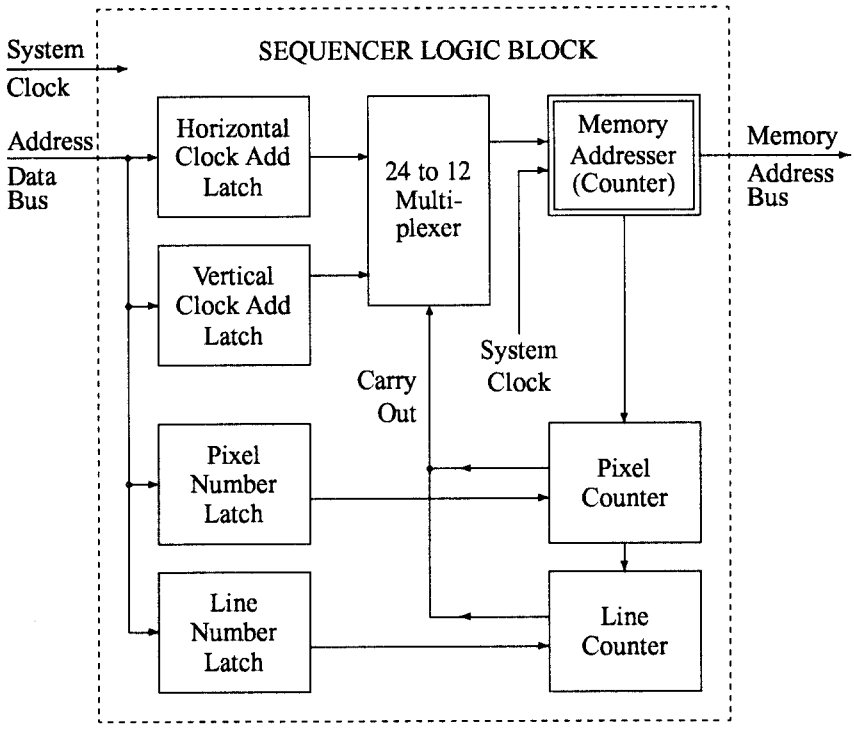

Figure 3. The block diagram of the sequencer logic design.

time, based on the resolutions of a given system clocking rate. Therefore the access time of the external memory device is a critical specification and should be fast enough to deal with many events in one pixel readout time. For example, a 10ns memory device can define 100 events within one micro second as one pixel readout time for multiple CCDs. In this case, power consumption and heat dissipation for the high speed memory chip could be a potential problem.

An alternative design approach has been explored with the PLD technique to improve difficulty of timing arrangements in memory addresser design. The concept is direct logic implementation into a PLD *without* external memory devices to generate waveforms for multiple CCDs. This approach can be termed the PLD waveform sequencer design. The system clocking rate into the PLD can be reflected to the digital drive waveforms by the

logic circuit, and no software defined bitmap is necessary. The controller can be designed to generate all waveforms and control signals directly based on the system clock, which enables to provide very fast processing timing in practice. The simplicity of hardware structure is another benefit with this design. However it is easily expected that the control flexibility may not be fully guaranteed for multiple CCDs and various type of sensors. Precise synchronising in timing arrangements for waveforms and related control signals could results in the complexity of PLD design itself, since no external instructions are involved.

Considering remote sensing application with the waveform sequencer design, the controller flexibility may not be the first priority in system requirements. This is because the number and type of sensors are pre-determined normally before system design in such applications. With a given type of sensor and number, the system design can be much simpler to fulfil the requirements. Further, once the camera system is in the orbit, the sensors cannot be replaced, though a new upgraded devices are available. In terms of control flexibility, this is the fundamental difference with other applications, such as astronomical purposes. The design complexity can also be reduced significantly by employing virtual phase linear CCDs, which require only a single phase clocking in readout (Texas Instruments 1990).

Using the same type of sensors also contributes to the design simplicity, which is the case of this application practically. With these reasons, it is worthwhile to consider PLD waveform sequencer design approach particularly when relatively a small number of CCDs are involved, for example, less than ten. The multiplexing concept can be implemented in the form of hardware logic design in this case with high speed signal processing. Experiments are being made with this approach by Yoo (1995).

5. PROTOTYPE SYSTEM CONFIGURATION

Based upon the design concept discussed above, the multiple CCD camera controller using the PLD, as a single chip controller has been investigated. The heart of the whole system is the controller, however, the other parts play important roles which have to be considered together in design. In practice, optimisation of each parts in the whole system could be as important as the controller itself in operation. All relevant signals from the PLD should be exactly synchronised with the timing requirement of other units. The performance of the whole system would be reflected by the functional specification of each units. The system configuration is suggested here briefly on the basis of the single chip controller, however these should be optimised further according to the specific purpose of the instrument. Figure 4 is the schematic block diagram of the whole controller design.

- **CCD Sensors** : Currently a number of CCDs are produced by many manufacturers. For low altitude (less than 1000 Km) remote sensing application, orbital scanning mode

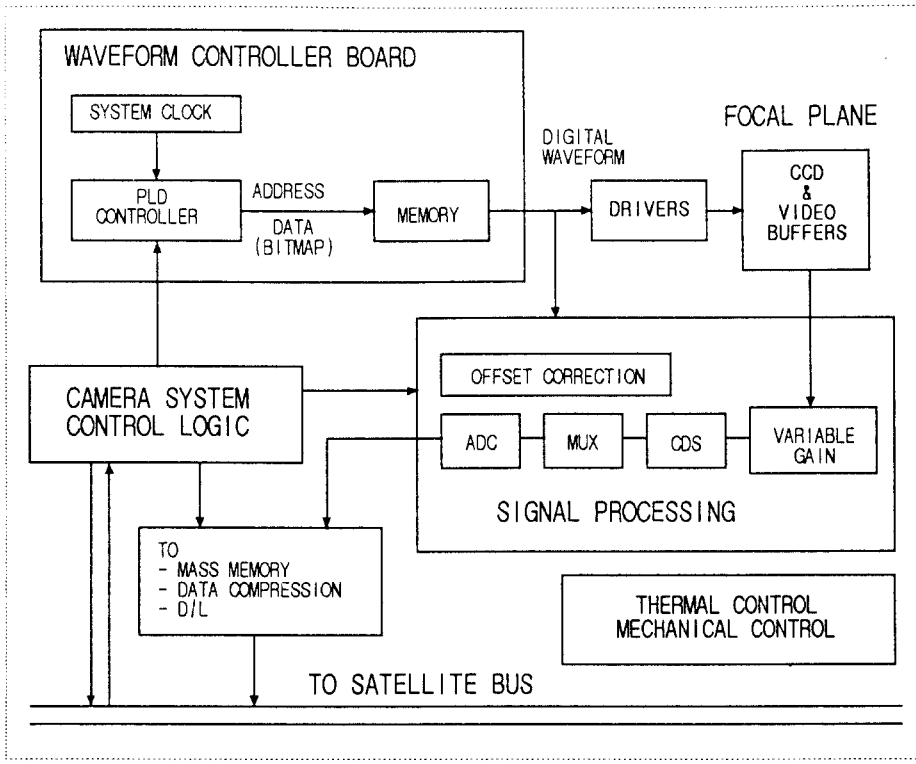

Figure 4. The schematic of system configuration for multiple CCD controller.

with linear sensors can be used. For example, in the focal plane of the SPOT satellite it has three optically butted CCDs. Each array has four Thomson TH7781 linear CCDs, with 1728 pixels per sensor, uses only 1500 pixels from each sensor to make 6000 pixels (Fratter *et al.* 1991). The incident light coming into each butted array is splitted by semi reflectant coating. In the case of using frame sensors, the controller can be easily configured with simple software effort.

- **Controller** : The controller design have been discussed above that can be integrated practically into a single PLD chip. External memory devices will be employed with the memory addresser design as described so far, while direct waveform sequencer logic can be implemented without memory for fast signal processing. The major factor in determining them will be the number of CCDs to be controlled and the type of sensors, considering its application.

- **Analog Driver** : This circuit is triggered by digital waveforms from the PLD controller to provide analog waveforms to each sensors. Recently available octal DACs are particularly useful to produce many voltage sources through software control and to minimise its space. Demultiplexing logic have to be designed to distribute the waveforms for individual sensors, which also can be integrated into a single PLD. The surface mount devices should be utilised for amplifiers and buffering circuit to reduce its space.

- **Video Processor** : This is the most susceptible part in terms of system noise performance, because the video signals from the sensors are amplified here. The CDS circuit is implemented to lowering the system noise and its precise timing control from the PLD, is the key feature. It would be desirable to use separate CDS circuitries for each sensors rather than multiplexing the analog image signals from the CCDs, which is the case of SPOT. This approach could overcome the processing speed constraint in fast readout mode.

- **Digitiser** : The signal conversion time is another factor to limit the signal processing timing when high resolution image data is required, such as in astronomy. For remote sensing application, it would be acceptable to have 12 bit resolution or less. Higher resolution requires longer conversion time, thus it becomes difficult to comply with its timing restriction. Some high speed digitisers for such purposes are available.

- **Digital data processing and Image storage buffer** : Due to its high speed signal processing, it would be desirable that data acquisition can be made in multiplexed manner from each channel. The digital multiplexing with some memory devices can avoid any significant timing problem. The image data have to be stored in a massive memory buffer so that it can be released by request from the ground station.

Apart from these, many other system components have to be supplemented as a complete remote sensing CCD camera system. The camera system control command logic block includes amplifier offset correction, integration and gain control, thermal and mechanics control etc. The bus interfacing is also an important part to interface the control signals and image data between camera controller and satellite system. Data transmission method have to be referred in controller design to match its system requirements. The attitude control and pointing accuracy are also critical factors in image data stability. The discussions in this paper rather focused on the camera controller design itself, without including above system parameters which will be discussed elsewhere separately. The design concept in this paper can be directly applied to the multiple CCD controller design with extensive experiments.

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