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On Designing Domino CMOS Circuits for High Testability

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高 Testability를 위한 Domino CMOS회로의 설계

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Abstract

In this paper, a new testable design technique for domino CMOS circuits is proposed to detect stuck-at(s-at), stuck-open(s-op) and stuck-on(s-on) faults in the circuits by observing logic test responses. The proposed technique adds one pMOS transistor per domino CMOS gate for s-op and s-on faults testing of nMOS transistors and one nMOS transistor per domino gate or multilevel circuit to detect s-on faults in pMOS transistors of inverters in the circuit. The extra transistors enable the proposed testable circuit to operate like a pseudo static nMOS circuit while testing nMOS transistors in domino CMOS circuits. Therefore, the two-phase operation of a precharge phase and a evaluation phase is not needed to keep the domino CMOS circuit from malfunctioning due to circuit delays in the test mode, which reduces the testing time and the complexity of test generation. Most faults of the transistors in the proposed testable domino CMOS circuit can be detected by single test patterns. The use of single test patterns makes the testing of the proposed testable domino CMOS circuit free from path delays, timing skews, chage sharing and glitches. In the proposed design, the testing of the faults which require test sequences also becomes free from test invalidation. The conventional automatic test pattern generators(ATPG) can be used for generating test patterns to detect faults in the circuits.

要 約

본 논문에서는 논리 모니터링 방식에 의해 stuck-at(s-at)고장, stuck-open(s-op)고장 및 stuck-on(s-on) 고장을 검출하기 위한 Domino CMOS회로의 테스트용이화 설계기법을 제안한다. Domino CMOS 게이트내 nMOS트랜지스터들의 s-op고장과 s-on고장을 검출하기 위하여 한개의 pMOS 트랜지스터를 부가하고 단일 게이트 및 다단 Domino CMOS회로내 인버어터의 pMOS트랜지스터 s-on고장을 검출하기 위해서 한개의 nMOS 트랜지스터를 부가한다. 부가된 트랜지스터는 Domino CMOS를 테스트 모드에서 pseudo nMOS회로로 동작하도록 만든다. 따라서 일반 domino CMOS회로의 테스트 시 회로지연에 의한 오동작을 방지하는 선충전(precharge phase)과 논리결정(evaluation phase)의 이상(two-phase) 동작을 필요로 하지 않아 테스트 시간과 테스트 생성의 복잡도를 줄일 수 있게 된다. 제안된 회로에서는 대부분의

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고장들이 단일 테스트 패턴에 의해 검출되는데 이에따라 경로지연이나 타임스큐, 전하재분배 및 글리치 등에 의해 테스트가 무효화되는 것을 피할 수 있으며 테스트 패턴 생성을 위하여 기존의 자동 테스트패턴 생성기(ATPG)를 이용할 수 있는 장점을 갖는다.

I. Introduction

Domino CMOS circuits have received much attention by researchers and engineers in industry due to their advantages over fully CMOS(FCMOS) circuits. In a domino CMOS gate, a single clocked pMOS transistor is used for pull up function which reduces the chip area and the parasitic capacitance, and thereby improves the switching speed of the gate[1,2].

However, the testing of domino CMOS circuits remains to be problematic. It has been known that the classical s at fault model is not adequate for CMOS circuits because it does not guarantee high fault coverage[3]. FCMOS and domino CMOS circuits have peculiar failure modes which are modeled as transistor s-op and s-on faults [3-8]. Many researchers have attempted to solve the problem of detecting s-op and s on faults in FCMOS and domino CMOS circuits[9-24]. It has been pointed out that to detect the s-op fault, two test patterns are required and to detect s-on faults, the current monitoring method and some special hardware are required together with two-pattern tests or three-pattern tests for logic monitoring. Even with these multi-pattern tests, some s-op faults in CMOS circuits may be missed in the presence of unequal path delays, timing skews and charge sharing among internal nodes [11,17]. To overcome this problem, robust tests have been introduced[11-14]. A robust test sequence is composed of two test patterns with unit Hamming distance to prevent the occurrence of intermediate patterns which may change the gate output value set by the initialization pattern. Recently, it has been reported that even the robust two-pattern tests can be invalidated in the presence of glitches[15,18]. The generation of robust test sequences is complex and time consuming. For certain faults in CMOS combinational circuits, robust two-pattern tests may not even exist.

More recently, several researchers have proposed testable CMOS design schemes which are capable of detecting s-op and s-on faults by logic test patterns[12,14,15,18,22]. In Liu and McCluskey's design[12], two extra transistors are used per gate for testability, each of them is connected between V_{dd} and pMOS block or V_{SS} and nMOS block. In multi-level circuits, one inverter is inserted after each gate and two-pattern tests are required to detect the s-op and s-on faults. In Gupta et al's design[14], two extra transistors are used and a two-pattern test is required to detect a s-op fault and a three-pattern test to detect a s-on fault. These two design schemes require two or three test patterns, which are not efficient due to highly complex test generation and also relatively long test length. Furthermore, because of multiple test patterns, test invalidation problems bue to glitches can not be overcome in these methods.

In Malaya al's design[18], one extra transistor and two control lines are used at the output node of a gate for testability as shown in Figure 1. In this scheme one pMOS transistor or nMOS transistor is connected to the gate output. By the control inputs(sc, st) together with test inputs for a pMOS or nMOS block, the gate is transformed to a pseudo pMOS or nMOS gate during the test mode. That is if sc = 1 and st = 0 together with the test patterns for a pMOS block, the circuit is transformed to a pseudo pMOS circuit. If sc = 1 and st = 1 together with test patterns for a nMOS block, the circuit is transformed to a pseudo nMOS circuit. This scheme does not invoke a high impedance state in the test mode and is free from the test invalidation. Unfortunately, this

design scheme is aimed for only s-op fault detection in FCMOS circuits. In Lee and Kang's method[22], a robust testable CMOS design is proposed to detect all s-op and s-on faults by single-pattern tests for the logic circuit and two-pattern sequences for the circuit added for testability. The proposed technique adds one transistor per gate for s-op fault testing and two transistors per gate or multi-level circuit for s-on faults.

In domino CMOS circuits, s-op faults may not be detectable due to test invalidation caused by charge sharing. This problem can be overcome by designing domino CMOS circuits with some extra hardwares. Some methods to detect single faults in domino CMOS circuits were presented[20,24] and a method for multiple fault detection in domino CMOS circuits was shown in [23]. In these methods, a properly ordered test set, derived for the gate-level models of domino CMOS circuits, can detect s-at, s-op and s-on faults in domino CMOS circuits by logic monitoring together with current monitiring. A testable design method for domino CMOS PLAs was given in [21]. However, no testable design technique for general domino CMOS circuits has been reported yet.

In this paper, a testable design technique of domino CMOS circuits to detect s-op and s-on faults by logic monitoring is proposed. The proposed design uses extra transistors to convert testable domino CMOS circuits to pseudo nMOS circuits during the test mode for nMOS transistors. Thus, the two-phase operations are not required during the test mode for nMOS transistors and the circuit can be tested by single-pattern tests. Therefore, the testability of domino CMOS circuits is improved drastically due to reduced testing time and test-pattern generation complexity. Under our design technique, the s-on faults in all the transistors can be detected by logic monitoring. In section II, we discuss fault behaviors in domino CMOS circuits and methods to ehnance the testability of domino CMOS circuits, which are the core of our approach. In seetion III, we present a new testable domino CMOS design technique and describe the detection of single and multipie faults in testable domino CMOS circuits. In section IV, we describe the testing of extra circuitry added for testability. In section V, we present simulation and layout results for benchmark 8-to-1 multiplexer circuit designed by the proposed technique. Finally, concluding remarks are given in seetion VI.

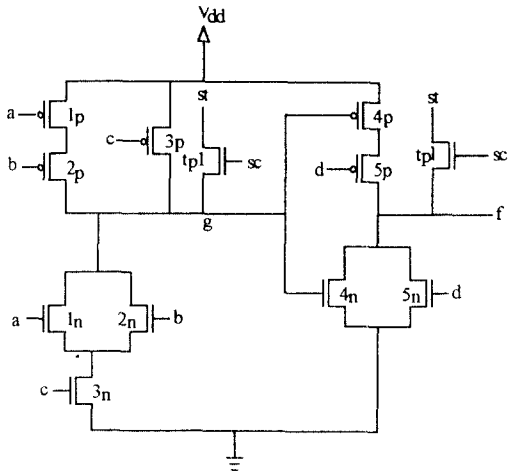

Fig 1. A testable CMOS circuit designed by conventional method[18].

Ⅱ. Faults and Their Testability in Domino CMOS Circuits

Domino CMOS circuits have some advantages over FCMOS circuits. Especially, the testability of domino CMOS circuits is known to be better. A domino CMOS circuit consists of clocking transistors, a nMOS functional block and an inverter as shown in Figure 2. The single precharging pMOS transistor is used to replace the pMOS block, thereby reducing the chip area. The domino CMOS circuits have inherently high testability. This is due to the fact that the domino CMOS circuit operates under a system clock composed of the precharge phase and the evaluation phase. After input signals get settled down during the precharge phase, the logic evaluation is performed. In the precharge phase, even when an intermediate pattern due to circuit delays occurs, the output value of the circuit can not be changed since the grounding nMOS transistor is turned off by $c_S = 0$. Therefore, the operation of domino CMOS circuits can be free from path delays and timing skews. However, the test may be still invalidated due to charge sharing[25]. The charge sharing problem in domino CMOS circuit has been overcome by adding a transistor in parallel with precharging pMOS transistor with its gate input fed by the output of the inverter. In the previous section, it was pointed out that all s-at, s-op and s-on faults in domino CMOS circuits can be detected by properly ordered single tests derived for all single s-at faults by using the conventional ATPG for gate-level models. These test patterns are applied to primary inputs during the precharge phase. After all of the test inputs are settled down, the system clock c_S is changed to logic 1 to evaluate the output value. In the conventional methods, testing operations are carried out by the precharge phase and the evaluation phase as normal circuit operations. The current monitoring method has been used to detect s-on faults in domino CMOS circuits. However, current monitoring requires additional hardware. Furthermore, the extraction of information from current measurement can be difficult.

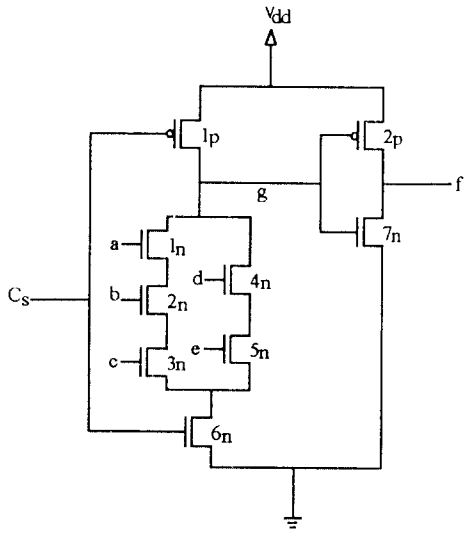

Fig 2. Basic domino CMOS circuit.

To overcome the overhead of current monitoring and two-phase test operations, a new approach based on our earlier method for a testable CMOS design[22] is proposed. In the previous work on a testable CMOS circuit design, to detect all s-op faults in the CMOS gate by single-pattern tests, each CMOS gate was designed to have no high impedance state. To detect the faults by single-pattern tests, the output node of gate is connected to V_{dd} through a load device during the test mode as in the testing operation of the nMOS circuit. Extra transistors were introduced to make the circuit operate like a pseudo nMOS circuit in the test mode for nMOS transistors. This design scheme allows no high impedance state during the testing of all the faults in nMOS transistors. The similar idea[15,18] was presented to detect the s-op faults in FCMOS circuits. The concept on the idea is applicable to domino CMOS circuits to detect the s-op and s-on faults by logic monitoring. We will next discuss some problems of the conventional techniques used for a CMOS test-

able design[18].

For clarity, we define the followings.

Definition 1 : The part containing the nMOS functional block and nMOS grounding transistor is called a ***nMOS-region.***

Definition 2 : $1_{ts}(x1, x2,...,xn)(0_{ts}(x1, x2,...,xn)$ is the set of test input values by which the nMOS functional block is turned on(off), where x1, x2,...,and xn are input variables of the nMOS functional block and these can be omitted for simplicity.

Definition 3 : 1^*_{ts} is the set of test input values by which only the path including faulty transistors in a nMOS functional block is turned on.

Let us assume that the transistor 3_p in Figure 1 is s-op. To detect this fault, the test pattern T(a, b,c,d,sc,st) = (1,1,0,0,1,0) can be used. Under the test pattern, the faulty circuit has logic value 0 at node g, whereas the fault-free circuit should have the different logic value at node g. Thus, the fault can be detected. Under the test patterns, the extra transistor t_{pl} works as a pull-down transistor ; if a s-op fault exists in the pMOS block, the output value is pulled down to logic 0 through t_{pl}. If the extra transistor t_{pl} is a pMOS transistor, the output value is pulled down at best to the absolute value of the threshold voltage. This voltage may be considered as logic 0, but not enough to turn on completely the pMOS transistor 4_p in the next gate. Therefore, the test may fail to detect this fault. This drawback can be overcome by using an extra nMOS transistor which is connected in parallel with the nMOS-region[15]. However, this design scheme is not practical because of its high hardware overhead. On the other hand, in detecting s-op faults of pMOS transistors in a domino CMOS circuit, even if there exists a high impedance state during the test mode, the circuit is free from test invalidation due to path delays, timing skews, charge sharing and glitches at input nodes. For the test to be invalidated, the output of a faulty gate should be changed during test opeartions. Since there exists only the s-op transistor between V_{dd} and the output node of the faulty gate, the output value of the faulty gate can never be changed. Therefore, this test can not be invalidated.

Next, let us consider the s-on fault detection in a domino CMOS circuit. First, we pay attention to the clocking transistors and the inverter. Assume that the transistor 6_n is s-on faulty in Figure 2. To detect this fault, 0 should be applied to c_S which is the input of transistor 6_n, and 1_{ts} is required to make a path from the gate output g to the ground. The output f of the fault-free circuit is set to 0. However, due to a conduction path formed between V_{dd} and V_{SS}, the voltage of output f is determined by the relative resistances of the pMOS transistor and the nMOS-region. Therefore, if the dominant relation between the pMOS transistor and the nMOS-region is not assumed, the output of a faulty gate can not be obtained deterministically by this test pattern. One method to solve this problem is to make the circuit n-dominant or p-dominant by using extra transistors in testing mode. This technique will be described in detail in the next section.

In the conventional method[23], it is described that s-at, s-op and s-on faults in transistors except the nMOS transistor in the inverter of a domino CMOS circuit can be detected by signle-pattern tests. But strictly speaking, the single-pattern tests described in [23] may be considered to be two-pattern tests ; the precharge phase of the system clock acts as an initialization pattern. It should be noted that the system clock input is used to control the two phases during normal operation. However, if we detect the faults in the domino CMOS circuits by single-pattern tests without the precharge phase, the testability of the domino CMOS circuits can be enhanced. Our approach is based on this concept. We will describe a new testable domino CMOS circuit in the next section.

Ⅲ. A New Testable Design of Domino CMOS Circuits

In the previous section, it was pointed out that the use of two-phase test operations makes domino CMOS circuits robust-testable against circuit delays and timing skews. The testing speed of a domino CMOS circuit by single-pattern tests, under two clock phases, is comparable with that of a FCMOS circuit by two-pattern tests. In the conventional testing methods for domino CMOS circuits, it has been inevitable to order the test patterns and/or to insert special initialization patterns in the test set, and the testing of s-on faults by logic monitoring has not been possible [20,23]. To overcome these problems, we introduce a new testable domino CMOS circuit with some extra transistors. One pMOS transistor is added to every gate output and one nMOS transistor is added to the last stage of the circuit as shown in Figure 3. Thus, for multi-level circuits consisting of N gates, only N+1 extra transistors are used for testability. The extra transistors are controlled by two control inputs ct_1 and ct_2. Although a similar technique for the CMOS testable design has been presented[18], it is not free from testing problems as described in section II. In the testable domino CMOS circuit proposed here, during normal operation, $ct_1=1$ and $ct_2=0$ are needed to ensure that extra transistors do not affect normal operations. Every output of gates is controlled by the two inputs ct_1 and ct_2. We consider the system clock input c_S as one of primary inputs during the test mode. The extra transistors t_{p1} and t_{p2} act like load transistors of nMOS circuits during $ct_1=0$ and $ct_2=1$, which make the circuit under test operate as a pseudo nMOS circuit. Because the testable circuit acts like a pseudo nMOS circuit in the test mode for nMOS transistors, most of the faults can be detected by single-pattern tests without test invalidation due to circuit delays, timing skews, charge sharing

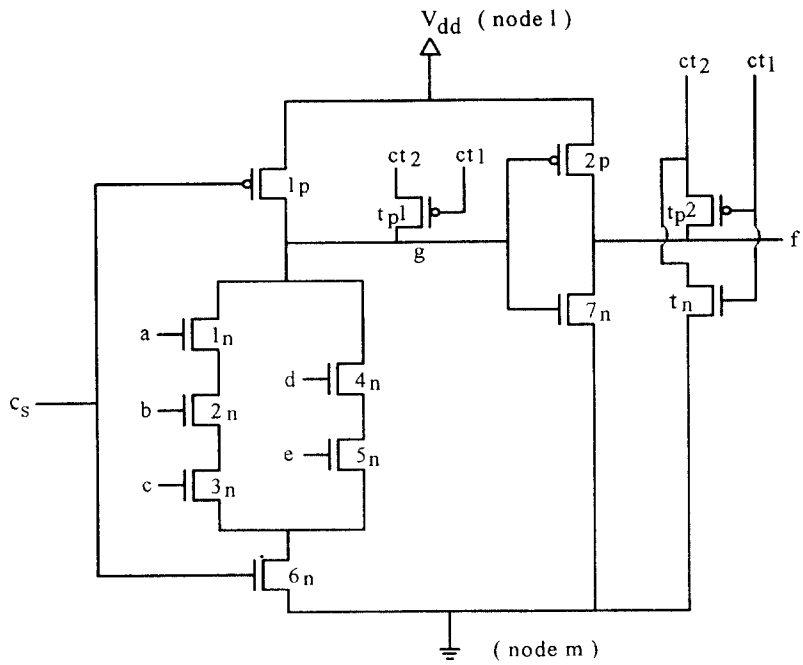

Fig 3. Proposed basic testable domino CMOS circuit.

and glitches. The testing time for the circuit which operates as a pseudo nMOS circuit is almost same as that of a general nMOS circuit. In the next two subsections 3.1 and 3.2, we describe the test operation in detail.

3.1 S-op faults detection.

3.1.1 Detection of s-op faults in nMOS transistors.

For s-op testing, $ct_1=0$ and $ct_2=1$ together with 1_{ts} or 0_{ts} are required. It should be noted that the on-resistances of the extra transistors t_{p1} and t_{p2} are considerably higher than those of nMOS transistors in the circuit. By the control inputs, the circuit acts like a pseudo nMOS circuit. Figure 4 represents the circuit schematic during the s-op test mode for the nMOS-region. During the testing of s-op faults in the nMOS-region, $c_S=1$ is needed. This keeps the precharging pMOS transistor turned off and the faults can be detected by signle-pattern tests.

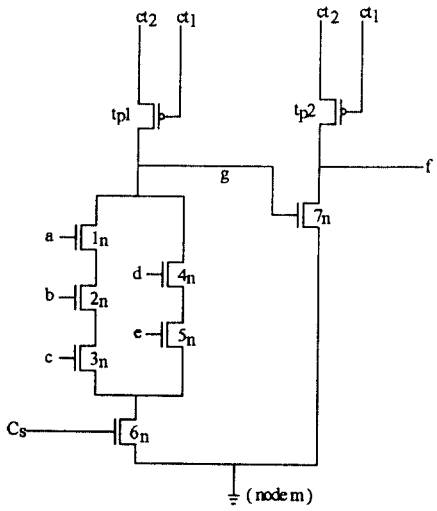

Fig 4. Circuit schematic in the test mode for nMOS transistors.

Definition 4 : When 0_{ts}, 1_{ts} and 1^*_{ts} are used for a part of the test pattern, they are denoted as $\langle 0_{ts}\rangle$, $\langle 1_{ts}\rangle$ and $\langle 1^*_{ts}\rangle$ respectively in the test pattern.

Assume that the transistor 2_n is s-op. We can detect the fault by the test pattern $T(a,b,c,d,e,C_s,ct_1,ct_2,1,m)=(\langle 1^*_{ts}\rangle 1,0,1,1,0)$. In this test pattern, 1 and m represent the V_{dd} and V_{SS} nodes of the circuit. The output f of the faulty circuit is 0 for the test pattern, whereas the output of the fault-free circuit is 1. Therefore, the fault can be detected. In case of the s-op fault of the transistor 6_n, we can detect this fault by the test pattern $(\langle 1_{ts}\rangle 1,0,1,1,0)$.

The test pattern for the s-op fault of the transistor 6_n is same as that of nMOS transistors in the functional block. That is, the s-op fault in the grounding nMOS transistor can be tested by the test pattern for s-op faults in the nMOS functional block.

Next we consider the s-op fault of the transistor 7_n which is the nMOS transistor of the inverter. This fault can be detected by the test pattern $(\langle 0_{ts}\rangle,1,0,1,1,0)$. To make the circuit act like a pseudo nMOS circuit, $ct_1=0$ and $ct_2=1$ are required. By this pattern, the output of the faulty circuit is set to 1, whereas the output of the fault-free circuit is set to 0. Therefore, the fault can be detected.

3.1.2 Detection of s-op faults in pMOS transistors

First, let us assume that the transistor 1_p is s-op. When 1_p is s-op, no conduction path exists between V_{dd} and the node g, and hence the node g can not be charged to logic 1. During the testing of pMOS transistors in a domino CMOS circuit, $ct_1=1$ and $ct_2=0$ are required. This fault can be detected by the test sequence $\{T_1(a,b,c,d,e,c_S,ct_1,ct_2,1,m),\ T_2(a,b,c,d,e,c_S,ct_1,ct_2,1,m)\}=\{(\langle 1_{ts}\rangle,1,1,0,1,0),\ (\langle 1_{ts}\rangle 0,1,0,1,0)\}$. By the first test pattern, the circuit output f is initialized to logic 1. Under the second test pattern, the output f of the faulty circuit is set to 1, whereas the fault-free circuit output f is set to 0. Thus the fault is detected. Next, we consider when the transistor 2_p is s-op. Under this fault, the output f can never be charged to logic 1, since no path exists between V_{dd} and the output node f. This

fault can be detected by the test sequence {(⟨1_{ts}⟩,0,1,0,1,0), (⟨1_{ts}⟩,1,1,0,1,0)}. By the first test pattern, the output node f is initialized to logic 0. By the second test pattern, the faulty output is set to 0, whereas the fault-free output f is set to 1. Therefore, the fault can be detected.

Theorem 1 : The s-op faults in the proposed testable domino CMOS circuits can be detected without test invalidation by path delays, timing skews, charge sharing and glitches.

Proof : During the testing of s-op faults in the nMOS transistors in the proposed testable domino CMOS circuit, $ct_1=0$ and $ct_2=1$ are applied, by which the circuit acts like a nMOS circuit. To detect the s-op fault in the nMOS region, 1_{ts} should be applied to primary inputs. Under this test pattern, the faulty output of the circuit attains the V_{dd} level through t_{pl}, whereas if the circuit is fault-free, there exist a conduction path from V_{dd} to V_{SS} through t_{pl} and some paths in the nMOS region. Because the on-resistance of the extra transistor t_{pl} is designed to be considerably higher than that of the nMOS-region, the output of the fault-free circuit is set to 0. Therefore, the fault is detected. The s-op fault in a nMOS transistor of the inverter can be detected simply. To detect this s-op fault, the test pattern (⟨0_{ts}⟩,1,0,1,1,0) can be used. Under this test pattern, the circuit operates like a pseudo nMOS circuit and no high impedance state occurs. By the test pattern, the faulty output of the circuit shows the logic value 1, whereas the fault-free output represents the logic value 0. Thus, the fault can be detected. Durign testing pMOS transistors, even if a high impedance state exists, test invalidation due to the delays, timing skews and glitches does not occur. To invalidate the initialization value at the output of the clocking gate, any path without the faulty transistor is needed, by which the initialization logic value at the output node of the clocking gate can be changed. However, there does not exist any conduction path connected in parallel with the pMOS transistor under test. Therefore, the faults can be detected without test invalidation. Because the node g and f have logic value 0 in high impedance during s-op fault testing, charge sharing problem does not occur. Q.E.D.

3.2 S-on fault detection.

3.2.1 Detection of s-on faults in the nMOS-region.

Let us suppose that the transistor 2_n in the nMOS-region is s-on. By the test inputs $ct_1=0$ and $ct_2=1$, the circuit is converted to a pseudo nMOS circuit. The fault free output f of the domino CMOS circuit is set to 0. For this fault to be detected, the faulty output should be 1. However, by the test patterns, the precharging pMOS transistor is kept turned on during the test operation. Therefore, the net on-resistance of the pMOS block is reduced, which invalidates the function of t_{pl}. This problem can be avoided by disconnecting the V_{dd} node from the power supply during s-on fault testing. One may suspect that if the V_{dd} node is disconnected from the power supply, the circuit may not work during test operation. In our design technique, when the V_{dd} node of every gate is disconnected from the power supply, the power required for testing operations is supplied through the extra transistors which are connected to the output of each domino gate. This fault can be detected by the test pattern(1,0,1,0,0,1,0, 1,NC,0). In the test pattern, NC represents that the V_{dd} node of the circuit is disconnected from the power supply. By this test pattern, the output g of the faulty circuit is set to 0, whereas the output g of the fault free circuit is set to 1. Thus, the fault is detected.

Next, consider the s-on fault of the transistor 6_n, the grounding nMOS transistor. This fault can be detected by the test pattern(⟨1_{ts}⟩0,0,1,NC, 0). The faulty output f of the circuit for this test pattern is 1, but the fault-free output f is 0. Therefore, the fault is detected.

Lastly, let us consider the s-on fault of the nMOS transistor 7_n in the inverter. We can detect this s-on fault by the test pattern (⟨1_{ts}⟩, 1,0,1,NC,0). Under this test pattern, the output f of the faulty circuit is 0, because the on-resist-

ance of t_{p2} is considerably higher than that of the transistor 7_n. When the circuit is fault-free, there is no conduction path from V_{dd} to V_{SS} and the output f of the fault-free circuit is 1. Thus, the fault is detected.

3.2.2 Detection of s-on faults in pMOS transistors of domino CMOS circuits.

Let us consider s-on faults in the precharging pMOS transistor and the inverter in a domino gate. To ensure that the s-on fault can be detected by logic monitoring, the circuit should be p-channel dominant during the test mode, which is made possible by inserting an additional high-resistance transistor serially with the nMOS transistor in the inverter. In our design scheme, the resistance of the nMOS block can be increased by using the transistor t_n. First, we consider the transistor 1_p s-on fault. We can detect this fault by the test sequence {(⟨1_{ts}⟩,1,1,0,1,0), (⟨0_{ts}⟩,1,1,0,1,0)}. By the test sequence, the fault-free output f is set to 1, whereas the faulty output f becomes 0. Therefore, the fault can be detected. Now we consider the test invalidation problem in the s-on testing of transistor 1_p. In detecting the transistor 1_p s-on fault, we do not use any extra transistor for testability. There exists a high impedance state during the testing and two test patterns are required to detect this fault. As described earlier, if there exists a high impedance state at the output node during the test, test invalidation may occur. For the test to be invalidated, the node g should be at 1 in the fault-free circuit, which is possible only when a negative glitch occurs at the system clock input c_S. If the test invalidation is only due to the glitches caused by the delays in the prior logic, the transistor 1_p s-on testing is free from such test invalidation.

Next, let us consider the transistor 2_p s-on fault. Figure 5 represents the circuit schematic in the s-on fault test mode for the pMOS transistor in the inverter. To detect this fault, the node g shoud be set to 1 and $c_S = 0$ is needed. This test input value sets the output f to logic 0 in the fault-free circuit. However, when this test input value is applied to the faulty circuit, a conduction path is formed from V_{dd} to V_{SS} in the inverter. Therefore, the faulty output value cannot be obtained deterministically, and the fault may not be detected This problem can be overcome by using an extra transistor t_n. The on-resistance of the transistor t_n is made higher than that of the pMOS transistor 2_p. This fault can be detected by the test pattern (⟨0_{ts}⟩,0,1,0,1,NC). By this test pattern, the fault-free output is set to 0, whereas the faulty output is set to 1. Therefore, the fault can be detected.

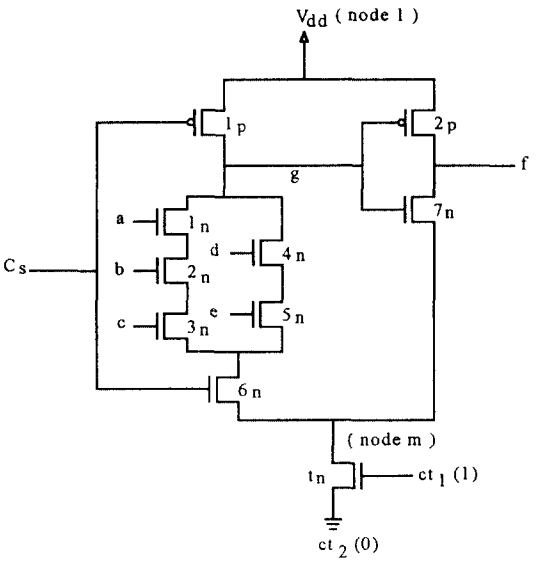

Fig 5. Circuit schematic in the s-on fault test mode for the pMOS transistor in the inverter.

Theorem 2: The s-on faults in the proposed testable domino CMOS circuit can be detected by logic monitoring without test invalidation due to path delays, timing skews, charge sharing and glitches.

Proof: Because during the s-on fault testing of the precharging pMOS transistor in the testable donino CMOS circuit, the gate output is in a high

impedance state and two test patterns are required However, no paths are connected in parallel with the path containing the faulty transistor and this two-pattern test is free from the test invalidation due to path delays, timing skews and glitches. Because the output of the faulty gate in a high impedance state is kept to logic 0, the testing operation is also free from the charge sharing problem. When detecting other s on faults except the precharging pMOS transistor in the circuit, no high impedance state occurs. Therefore, the fault can be detected without test invalidation. Q.E.D

3.3 Design of testable multi-level domino CMOS circuits.

Definition 5 : A general domino CMOS circuit which consists of more than two basic domino CMOS circuits is called a ***multi-level domino CMOS circuit.***

Our design technique can be easily expanded to multi level domino CMOS circutis. We next consider the realization of robust testable multi level domino CMOS circuits. As shown in Figure 6, one pMOS transistor is connected to every domino gate output and one nMOS transistor is connected to V_{ss} for detection of the s on fault in the pMOS transistor of the inverter in the last stage of the multi level circuit. The total number of extra transistors added for testability in the proposed testable N gate multi level domino CMOS circuit is N+1. Assume that the pMOS transistor *n is s op, we can detect this fault by the test sequence (T_1(a,

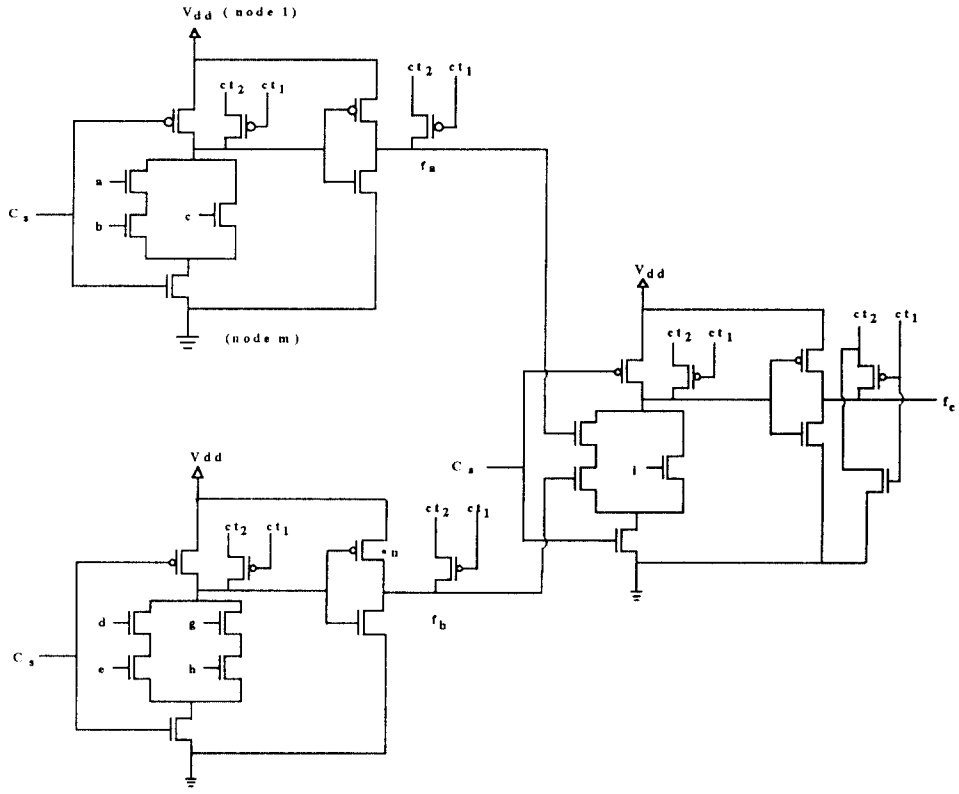

Fig 6. A testable multi level domino CMOS circuit.

b,c,d,e,g,h,i,C_s,ct_1,ct_2,1,m), T_2(a,b,c,d,e,g,h,i,C_s, ct_1,ct_2,1,m) ={(〈$1_{ts(a,b,c)}$〉,〈$1_{ts(d,e,g,h)}$〉,0,0,1,0,1,0), (〈$1_{ts(a,b,c)}$〉,〈$1_{ts(d,e,g,h)}$〉,0,1,1,0,1,0)}. By this test sequence, the fault-free logic value of output f_c is 1, whereas the faulty output value is set to 0. Therefore, the fault can be detected. Next, suppose that s-on fault occurred in transistor *n. This fault can be detected by the test sequence {(〈$1_{ts(a,b,c)}$〉,〈$0_{ts(d,e,g,h)}$〉,0,0,1,0,1,NC), {(〈$1_{ts(a,b,c)}$〉, 〈$0_{ts(d,e,g,h)}$〉,0,1,1,0,1,NC)}. By this test sequence, the fault-free output f_c is set to 0, whereas the faulty output f_c is set to 1. Therefore, the fault can be detected.

3.4 Multiple fault detection in domino CMOS circuits

In this section, we show the operation of domino CMOS circuits under multiple faults composed of s-op and s-on faults along with methods to detect these multiple faults. It is known that the multiple fault test set(MFTS) derived for multiple s-at faults in the gate-level model of a domino CMOS circuit can also detect multiple faults composed of s-at, s-op and s-on faults in the nMOS functional block[23]. In [23], it is also pointed out that multiple faults in the functional block of a domino CMOS circuit can not change the fault effect caused by any faults in clocking transistors and the inverter. Therefore, we only have to consider multiple faults in the clocking transistors and the inverter. It is known that multiple faults consisting of s-at and s-op faults in a domino CMOS circuit can be detected by logic monitoring with the test patterns derived from the gate-level model. Therefore, it is obvious that any multiple fault consisting of s-at and s-op faults in the proposed testable domino CMOS circuit can be detected by the test patterns derived from the gate-level model. In contrast, a careful attention is needed for testing of multiple faults with s-on faults in clocking transistors and the inverter. Generally s-on fault testing by logic monitoring is difficult. Especially, in case of multiple s-on faults, it may be more complex. However, this problem can be easily solved in our design scheme. Let us consider 4 cases of multiple faults in the circuit of Figure 3, each of them contains the s-on faults in four transistors(1_p, 2_p, 6_n, 7_n).

〈Case 1〉: Suppose a multiple fault containing the transistor 2_p s-on fault this s-on fault is equivalent to the s-a-1 fault on the output line f in the test mode, because even if there exists other faults in the clocking transistors and the inverter, the output value of the faulty circuit can not be changed in the test mode. Therefore, any multiple fault composed of the 2_p s-on fault and any other faults in 1_p, 6_n and 7_n can be detected by the test pattern for the 2_p s-on fault.

〈Case 2〉: Suppose a multiple fault containing the transistor 7_n s-on fault. To detect this fault, the test pattern (〈1_{ts}〉,1,0,1,NC,0) is required. The circuit is transformed to a pseudo nMOS circuit by this test pattern. Therefore, the output of circuit under test is 0 in spite of any other faults in clocking transistors and the inverter. That is, the fault is equivalent to the s-a-0 fault on the output line f.

〈Case 3〉: Suppose a multiple fault containing the transistor 6_n s-on fault. During the test mode for this s-on fault, the circuit is transformed to a pseudo nMOS circuit. By the test pattern for the s-on fault in the transistor 6_n, a conduction path is activated from the node g to V_{SS} resulting in the logic 0 at g. This implies that the 6_n s-on fault is equivalent to s-a-0 on the line g and to s-a-1 on the line f during the test mode. This s-at logic value can not be changed by any other faults except the s-on fault in 7_n. The multiple faults containing the s-on fault in 7_n can be detected by the test pattern(〈1_{ts}〉,1,0,1,NC,0) as described in Case 2.

〈Case 4〉: Suppose a multiple fault containing the transistor 1_p s-on fault. During the test mode, the 1_p s-on fault is equivalent to the s-a-1 fault at the node g and the s-a-0 fault at the node f if the transistor 7_n is not s-op faulty. During testing operations, any other fault except the s-op fault of the transistor 7_n in the circuit can not change

the faulty value at the output node f. The multiple faults containing the transistor 7_n s-op fault can be detected by the test pattern for the transistor 7_n s-op fault. From the above discussion, it can be pointed out that any multiple fault containing the s-on faults of the clocking transistor and the inverter can be detected in proposed design scheme.

Theorem 3 : Any multiple fault consisting of s-at, s-op and s-on faults in domino CMOS circuits can be detected by MFTS for the gate-level models of domino CMOS circuits without test invalidation due to circuit delays, timing skews, charge sharing and glitches.

Proof : In the testable domino CMOS circuit designed by the proposed technique, because any multiple fault can be mapped to any multiple fault in the gate-level models for domino CMOS circuits, it can be detected by the MFTS for the models. When detecting the s-op faults in the precharging pMOS transistor and the pMOS transistor of the inverter, even if a high impedance state is created at the gate output, test invalidation due to circuit delays, timing skews, charge sharing and glitches does not occur. This is due to the fact that the faulty output value can be changed by no means, if only the glitches caused by circuit delays in the prior logic are considered. During the testing of other faults except these faults, the testable domino CMOS circuit acts like a nMOS circuit and/or no high impedance state is caused by any test patterns. Therefore, the test can not be invalidated by the circuit deays, timing skews, charge sharing and glitches. Q.E.D

Ⅳ. Testing the Circuitry Added for Testability

Before testing the original circuit, the additional circuit for testability should be tested to guarantee the test results for the original circuit. In our technique, two test patterns are used to detect the s-op and s-on faults in additional transistors. For the test to be invalidated, the output of the gate under test should be in a high impedance state during test application. While detecting the faults in extra transistors by two test patterns, test invalidation can occur if the output value by the first pattern is changed to its complementary logic value. This can be possible when at least one path from V_{dd} or V_{SS} to the primary output exists even without any faulty transistor. In our design scheme, since no circuit is connected in parallel with the extra transistors under testing, test invalidation cannot occur. The possible faults are s-op, s-on faults in transistors and s-a-0/1 fault on transistor leads. The s-a-0/1 faults on control line ct_1 are equivalent to s-op and s-on fault of transistor t_n. Therefore, the faults which need to be considered are s-op, s-on faults in transistor t_n, t_{p1} and t_{p2}, and s-a-0/1 faults on control line ct_2. First, let us consider the testing of transistor t_n. Suppose that the transistor t_n is s-op. Table 1 shows the test sequences for the s-op and s-on faults in transistor t_n. (T_1, T_2) is for s-op fault and (T_3, T_4) is for s-on faults. By the test pattern T_1, the output f is initialized to logic 1 and by test pattern T_2 the fault-free output is 0, whereas the faulty output is 1. Therefore, the fault can be detected. By the test pattern T_3, the output f is initialized to logic 1 and by the test pattern T_4, the output of fault free circuit retains the previous logic value 1. However, the output of faulty circuit should be 0, and thus the s-on fault can be detected.

Table 1. Test sequence for the s-op and s-on faults in extra transistor t_n.

	a	b	c	d	e	c_S	ct_1	ct_2	l	m
T_1	1	1	1	0	0	1	1	0	1	0
T_2	0	0	0	0	0	0	1	0	0	NC
T_3	1	1	1	0	0	1	1	0	1	0
T_4	0	0	0	0	0	0	0	0	1	NC

Next, we consider the s-a-0/1 faults on the control line ct_2. We can detect this fault by test sequence in Table 2. In Table 2, X represents 'don't care' input and M represents that the corresponding nodes are used for monitoring the gate output

singals. The s-a-0 fault on the control line ct_2 can be detected by test sequence (T_1, T_2) and the s-a-1 fault on the control line ct_2 can be detected by sequence (T_3, T_4). By the test pattern T_1, the control node ct_2 is initialized to logic 1 and under test pattern T_2, ct_2 shows the faulty logic value 0, whereas ct_2 should represent fault-free logic value 1. Therefore, the fault can be detected.

Table 2. Test sequence for s-op and s-on faults on control line ct_2.

	a	b	c	d	e	c_S	ct_1	ct_2	1	m
T_1	X	X	X	X	X	X	1	1	1	0
T_2	X	X	X	X	X	X	1	M	1	0
T_3	X	X	X	X	X	X	1	0	1	0
T_4	X	X	X	X	X	X	1	M	1	0

Let us consider s-op and s-on faults in the extra transistor t_{p1}. This fault can be detected by the test sequence in Table 3.(T_1, T_2) is for s-op fault and (T_3, T_4) is for s-on fault. By the test pattern T_1, the output f is initialized to 1. By the test pattern T_2. the faulty output shows logic 1, whereas the fault-free output represents logic 0. Therefore, the fault can be detected. By the test pattern T_3, the output f is initialized to logic value 1. By the test pattern T_4, the faulty output shows logic 0, whereas the fault-free output represents logic 0. Therefore, the fault can be detected.

Table 3. Test sequence for s-op and s-on faulits in extra transistor t_{p1}.

	a	b	c	d	e	c_S	ct_1	ct_2	1	m
T_1	1	1	1	0	0	1	1	0	1	0
T_2	0	0	0	0	0	1	0	1	1	0
T_3	1	1	1	0	0	1	1	1	1	0
T_4	0	0	0	0	0	1	1	1	1	0

Lastly, we consider s-op and s-on faults in the extra transistor t_{p2}. We can detect these faults by the test sequence in Table 4. (T_1, T_2) is for s-op fault and (T_3, T_4) is for s-on fault. By the test pattern T_1, the output f is initialized to 0. By the test pattern T_2, the faulty output shows logic 0, whereas the fault-free output should represent logic 1. Therefroe, the fault can be detected. By the test pattern T_3, the output f is initialized to logic 0. By the test pattern T_4, the faulty output shows logic 1, whereas the fault-free output represents logic 0. Therefore, the fault can be detected.

Table 4. Test sequence for s-op and s-on faults in extra transistor t_{p2}.

a	b	c	d	e	c_S	c_1	c_2	1	m	
T_1	0	0	0	0	0	1	0	1	1	0
T_2	0	0	0	0	0	1	0	1	1	NC
T_3	0	0	0	0	0	1	0	1	1	0
T_4	0	0	0	0	0	1	1	1	1	NC

V. Experimental Results for 8-to-1 Multiplexer

The testable domino CMOS circuit designed by using the proposed technique was tested for quantitative analysis of overheads in test operation, area and delay overheads. A 8-to-1 multiplexer is used as a benchmark circuit. Layouts in both standard cell and gate array structures were created with the MAGIC design tool. Scalable CMOS technology with two layers of metal was used. Figure 7 shows the two standard cells with the extra transistors added for testability. The timing analyzer CRYSTAL was used to determine the delay for the two designs. Figure 8 shows the equivalent design using a gate array structure. Table 5 shows the data on the four testable multiplexers. The data shows that the delay overhead is small for the standard cell design methodology. But, the testable standard cell designs have relatively large area overhead compared with that of the gate array design. This is due to the fact that original standard cells were very compact. As a result, the additional transistors required in

testable design causes a significant increase in the cell area. The total area overhead percentage including the routing may be overestimated due to the fact that the number of additional signals needed, namely ct_1 and ct_2, is relatively large compared to the number of original signals. In large circuits, this ratio between the original circuit area and the additional area for extra transistors should decrease and, as a result, the additional area needed to route the two signals should be relatively small. For the gate array design, no area overhead exists in the design of cells. This is primarily due to the fact that in the gate array structure wherein the transistor utilization is less than 100 percent, the additional transistors needed is already available in the layout. Thus, the only overhead in area is due to the routing of the two additional signals. However, the overhead in de lay is rather large for gate arrays, compared to the standard cell design, due to the regular structure of the gate array. The effect of added capacitance from the additional pMOS transistor is larger than those in the testable standard cell design and hence the delay overhead in gate array design becomes larger than that of the standard cell design.

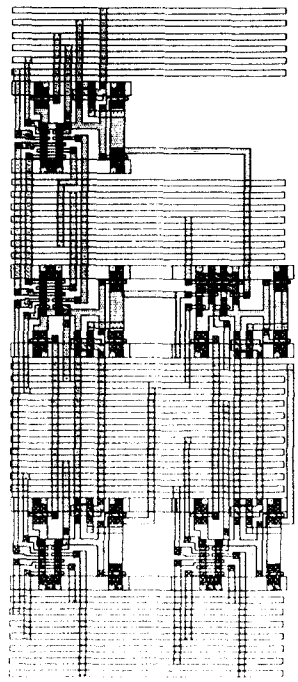

Fig 7. Standard cell layout for the testable domino CMOS 8-to-1 multiplexer designed by the pro posed technique.

Table 5. Area and delay overheads of testable 8-to-1 multiplexer designed by the proposed technique.

	Cell 1 Area [μm^2]	Cell 2 Area [μm^2]	Total Cell Area [μm^2]	Total Area Including Routing [μm^2]	Delay [ns]
Standard cell(S.C)	60 x 70	60 x 73	60 x 353	397 x 176	16.4
Testable S.C	60 x 75	60 x 79	60 x 379	437 x 181	16.84
S.C Overhead	7.14%	8.22%	7.37%	13.2%	2.68%
Gate Array (G.A)	116 x 108	116 x 81	116 x 513	370 x 309	29.17
Testable G.A	116 x 108	116 x 81	116 x 513	370 x 309	32.62
G.A Overhead	0.0%	0.0%	0.0%	2.16%	11.82%

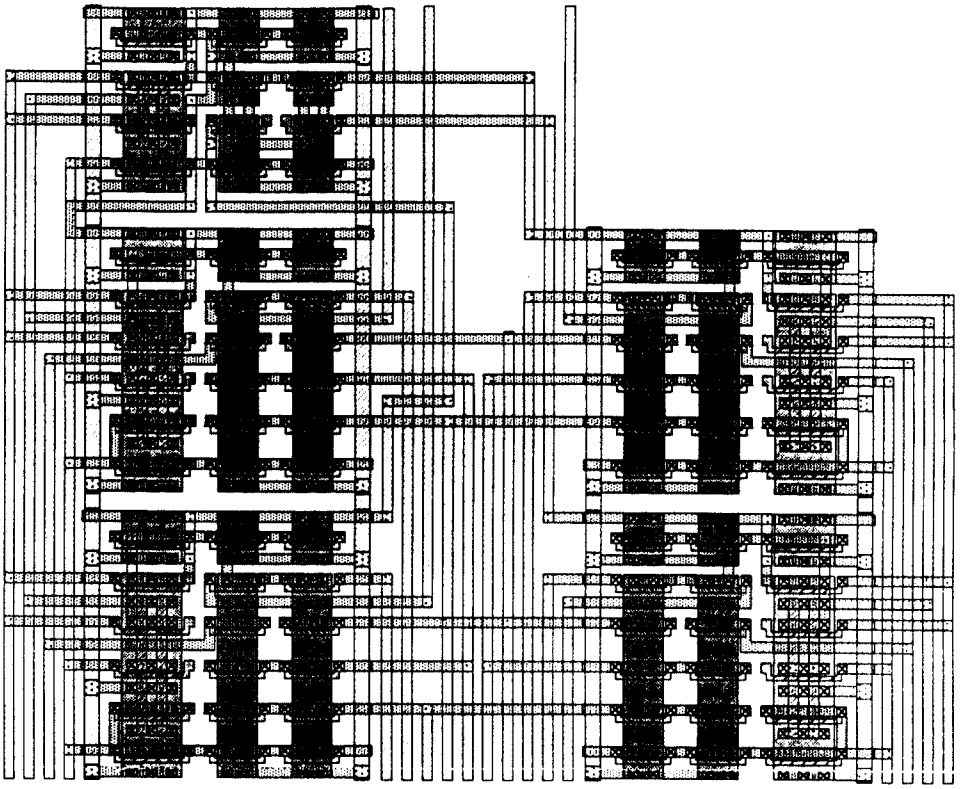

Fig 8. Gate array layout for the testable domino CMOS 8-to 1 multiplexer designed by the proposed technique.

Ⅵ. Concluding Remarks

A new testable design for domino CMOS circuit for high testability is proposed. By using small extra hardware, a domino CMOS circuit is designed so that all single and multiple s-at, s-op and s on faults can be detected by logic monitoring with high speed. Most of the transistors in the proposed testable domino CMOS circuit can be detected by single test patterns. Single pattern test makes the circuit testing insensitive to path delays, timing skews, charge sharing and glitches. Because the proposed testable scheme does not have precharge phases during testing operations, the testing speed is improved to that of nMOS circuits. The conventional ATPG for gate-level models is also applicable to generate the test set for the circuit designed by proposed technique. The proposed technique can be easily extended to multi-level circuits to obtain high testability. Unlike the discussion in [15,18], the extra transistors added for testability can be tested by two test sequences. Test invalidation problems due to the high impedance state do not occur in our design scheme. In FCMOS and dynamic CMOS circuits, some faults may cause electrical parameters change gradually and degrade the circuit performance. Analog testing is useful to detect this kind of failures[16]. In our design scheme, the extra transistors for testability can be used for monitoring the internal gate outputs in the circuits for analog testing. In multi-level circuits, the monitoring function of every gate would usually need many independent control lines to avoid signal

conflicts, but this drawback can be overcome by scan-path design. The extra transistors for s-op faults, when they are used in sequential circuit design with scan path technique, enable the monitoring of the gate output signals, which enhances the observability of the circuit.

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