고속 스윗칭을 위한 새로운 GTO 구동기법

論文
43~2~8

A New GTO Driving Technique for Faster Switching

金 永 錫*·徐 範 錫**·李 宅 基**·玄 東 石***
(Young-Seok Kim · Beom-Seok Seo · Taeck-Kie Lee . Dong-Seok Hyun)

Abstract—This paper presents the design of a new turn-off gate drive circuit for GTO which can accomplish faster turn-off switching. The major disadvantage of the conventional turn-off gate drive technique is that it has a difficulty in realizing high negative di_{GQ}/dt because of V_{RGM}(maximum reverse gate voltage) and stray inductances of turn-off gate drive circuit[1~2]. The new trun-off gate drive technique can overcome this problem by adding another turn-off gate drive circuit to the conventional turn-off gate drive circuit. Simulation and experimental results of the new turn-off gate drive circuit in conjunction with chopper circuit verify a faster turn-off switching performance.

Key Words : Turn-off Gate Drive Circuit(턴-오프 게이트 구동 회로), Storage time(축적 시간), Fall time(하강 시간), Tail current(후미 전류), Added turn-off gate drive circuit(첨가된 턴-오프 게이트 구동 회로)

1. Introduction

Recent developments in high-power semiconductor switching devices have yielded new and efficient controllable switches like the gate turn-off (GTO) thyristor. GTO's are able to handle higher surge currents than power transistors and have the advantage of gate turn-off capability, eliminating the need for commutator circuitry used silicon controlled rectifiers(SCRs). However, the efficiency and reliability of the GTO as a power switch is strongly influenced by its gate drive circuit. The effect of various gate drive circuit parameters on the GTO performance has been studied, and various types of drive circuit have been developed[3~6].

The main purpose of GTO turn-off driving is to turn off GTO safely with a shorter turn-off time and no increase of P_{off}(turn-off power dissipation). But it is difficult to satisfy both of these requirements because they are trade-off relationship. This paper presents a new topology of the turn-off gate drive circuit that can shorten the turn-off time with a little increase of P_{off} and be free from restriction of V_{RGM} and stray inductances of the turn-off gate drive circuit.

2. The Conventional Turn-off Gate Drive Technique

A GTO is turned off by applying a large nega-

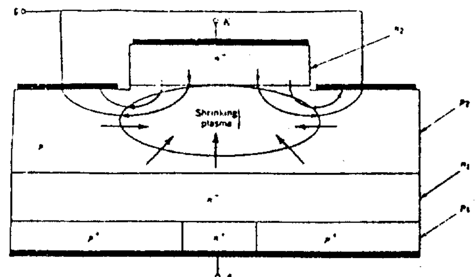


Fig. 1 Negative gate current squeezing the excess carriers stored in the P_2 and N_2 layers[1]

*正 會 員 : 漢陽大 大學院 電氣工學科 碩士課程
**正 會 員 : 漢陽大 大學院 電氣工學科 博士課程
***正 會 員 : 漢陽大 工大 電氣工學科 敎授·工博
接受日字 : 1993年 8月 10日
1次修正 : 1993年 11月 11日

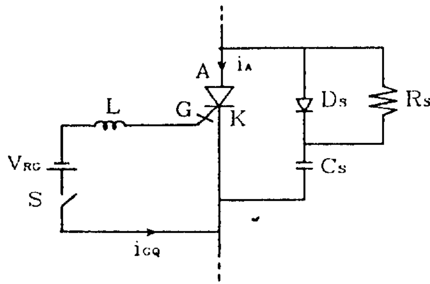


Fig. 2 Conventional turn-off gate dirve circuit

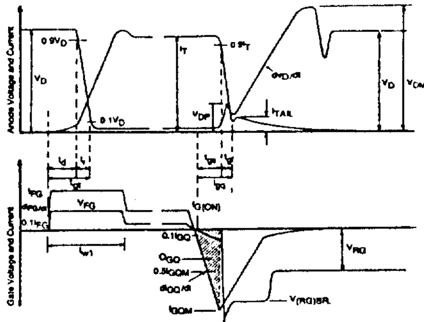


Fig. 3 General switching waveforms for GTO[2]

tive gate current for a short time on the order of 1/5 to 1/3 of the anode current being turned off.

Fig. 1 shows that the growing negative gate current is removing carriers stored in the P_2 and N_2 layers at the periphery of cathode islands. The conventional turn-off gate drive circuit of Fig. 2 supplies the negative gate current by turning on S. Fig. 3 shows general switching waveforms for GTO with snubber circuit. The negative di_{GQ}/dt, determined by V_{RG}/L, must be large in order to have a short t_{gs}(storage time) and a short t_{gf} (anode current fall time).

However, if negative di_{GQ}/dt is too large, anode tail current would be increased because many excess carriers remain in the N_1 and P_2 layers after regaining of voltage blocking capability of GTO. Hence, we must make negative di_{GQ}/dt as large as possible without a lot of increase of P_{off}. To make large negative di_{GQ}/dt within specific range, we should have a large V_{RG} and a small turn-off inductance L. But V_{RG} has limitation such as it should not be larger than the gate-cathode junction breakdown voltage. And for large GTOs the stray inductances(L_s) of the turn-off gate drive circuit may be large. We must pay attention to the layout and components of drive circuit to recuce the stray inductances. Therefore it isn't easy to make appropriately large negative di_{GQ}/dt at our request.

3. The New Turn-off Gate Drive Technique

3.1 The New Turn-off Gate Drive Topology

Fig. 4 show the new turn-off gate drive circuit. It is composed of the conventional turn-off circuit and the added turn-off circuit.

When we start GTO turn-off transient by turning on S_1, S_2 simultaneously, i_{GQ1} with negative di_{GQ1}/dt determined by V_{RG1}/L_1 is increased from the cathode to the gate by extracting excess carriers at P_2 and N_2 layers. At that time, i_{GQ2} with negative di_{GQ2}/dt determined by V_{RG2}/L_2 is also increased from the anode to the gate by extracting excess carriers N_1 and P_2 layers. After all, (i_{GQ}, di_{GQ}/dt) of the new turn-off gate drive circuit becoms (i_{GQ1}, di_{GQ1}/dt) plus (i_{GQ2}, di_{GQ2}/dt), respectively. Therefore the new turn-off gate drive circuit can turn off the GTO more rapidly than the only conventional turn-off circuit because the former extracts excess carriers more rapidly than the latter does.

After the excess carriers are sufficiently extracted during the t_{gs}, V_{AK} which has a V_{DP} (spike voltage) at its initial rising phase begins to rise with dV_{AK}/dt determined by snubber capacitor. If V_{AK} is equal or larger than V_{RG2}, the added turn-

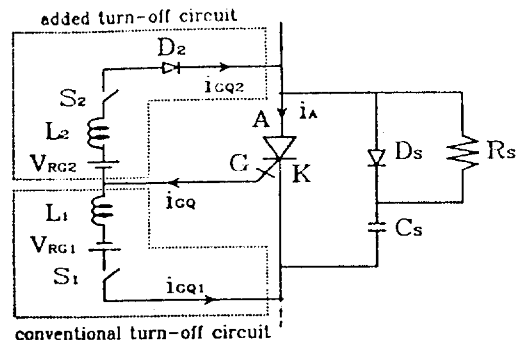


Fig. 4 New turn-off gate dirve circuit

off circuit becomes reverse-biased due to D_2. Therefore the added turn-off circuit operates during the only turn-off time and helps the new turn-off gate drive circuit to shorten turn-off time. In addition, the new turn-off gate drive circuit can be free from the constraints of V_{RGM} and stray inductances of the turn-off gate drive circuit.

3.2 Analysis Using Two-Transistor Model

Two-transistor model composed of Q_1(pnp transistor) and Q_2 (npn transistor) is shown in Fig. 5.

In the equivalent circuit both Q_1 and Q_2 are saturated in the on-state. However, if the base current to Q_2 could briefly be made less than the value needed to maintain saturation($I_{B2}<I_{C2}/\beta_2$), then Q_2 would go active and the GTO would begin to turn off because of the regenerative action present in the circuit when one or both of the transistors is active. If we turned off GTO by the new turn-off gate drive circuit, Q_2 would go active by i_{GQ1} and Q_1 would also go active by i_{GQ1} and i_{GQ2}. Therefore, the new turn-off gate drive technique can speed up the regenerative action by adding another turn-off circuit between the anode(emitter of Q_1) and the gate(collector of Q_1).

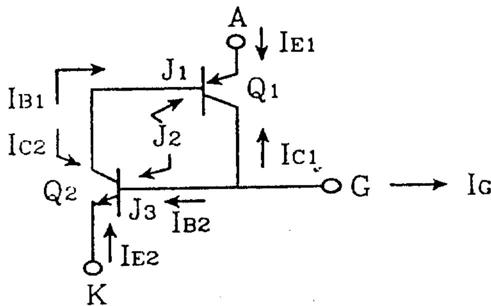


Fig. 5 Two-transistor model

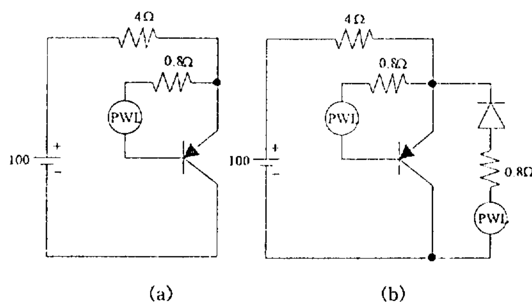


Fig. 6 (a) Conventional
(b) New turn-off circuit of Q.

4. Simulation of GTO Turn-off Transient

First, we simulated turn-off characteristics of Q_1 with SABER simulator to confirm that Q_1 would have a shorter turn-off time by adding another turn-off circuit.

Fig. 6 shows the conventional and new turn-off circuit of Q_1. We decreased forward bias base current of Q_1 from the on-state value to zero because reverse bias current can not exist at Q_1 of the GTO. The added turn-off circuit of fig.6 (b) helps the transient time from saturation to active to be decreased. Fig. 7 shows that the new turn-off circuit can turn off Q_1 more repidly them the conventional tum-off circuit.

For the convenience of GTO simulation we used a macro-model which is composed of two-transistor and three-resistor(2T-3R)[7]. We modified the parameters of two transistors in order to model the I_{TAIL}, which is based on the idea that each transistor has different intrinsic structure and doping density. But we have some problems with how to get parameters and obtained them by trial-and-error method. Fig. 8, 9 show V_{AK}, i_A, I_{GQ} of 2T-3R model operating in chopper circuit by the conventional and the new turn-off gate drive circuits. Increasing anode current during tgs shown in Fig. 9 shows that i_{GQ2} is added to the on-state value of anode current during tgs. Fig. 9

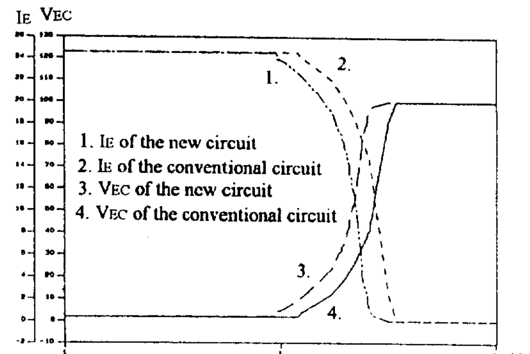
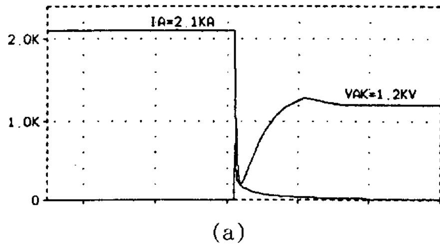
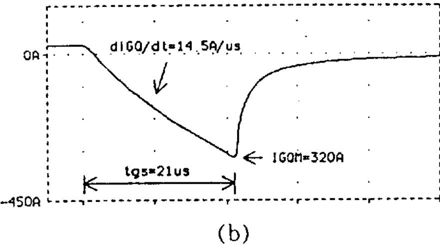


Fig. 7 Turn-off comparison between the conventional and new turn-off circuits

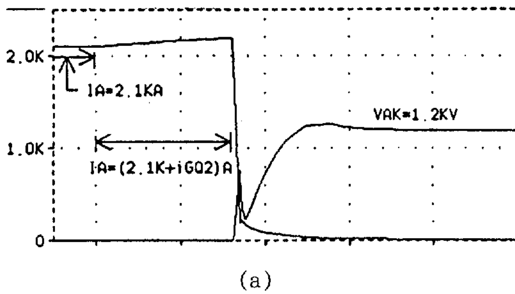


(a)

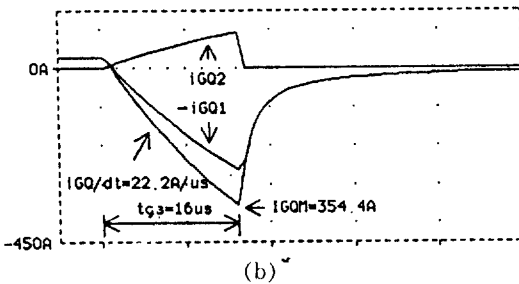


(b)

Fig. 8 (a) V_{AK}, I_A (b) i_{GQ} by the conventional turn-off circuit



(a)



(b)

Fig. 9 (a) V_{AK}, I_A
(b) i_{GQ1}, i_{GQ2} and i_{GQ} by the new turn-off circuit

shows that (i_{GQ}, di_{GQ}/dt) is (i_{GQ1}, di_{GQ1}/dt) plus (I_{GQ2}, di_{GQ2}/dt), respectively.

The comparison between the conventional and new turn–off gate drive techniques shows that turn–off time of the new turn–off gate drive circuit is less about 21% than that of the conventional turn–off gate dirve circuit.

5. Experimental Results and Discussion

The new gate drive circuit was tested with a Hitachi GFF90B12, used in the simple chopper circuit shown in Fig. 10, with an associated snubber circuit for the device. The data for the GTO is given in the Appendix.

We didn't use an inductance component in the conventional and the new turn-off gate drive circuits and tried to reduce stray inductances of the turn-off gate drive circuits. These efforts were to make large negative di_{GQ}/dt. And we used two gate terminal wires to prevent turn-off stray inductances from being common in both the added and the conventional turn-off circuit. We controlled negative di_{GQ}/dt by varying V_{RG}.

Fig. 11 shows the magnified initial phase of rising voltage across gate and anode. It shows that initial derivative of V_{AG} of the new turn-off gate drive technique is larger than that of the conventional technique.

From this we know that turn-off transient time of Q_1 by the new technique is shorter than that by the conventional technique.

Fig. 12 shows i_{GQ} and P_{off} by the conventional turn-off gate drive technique. It shows that the

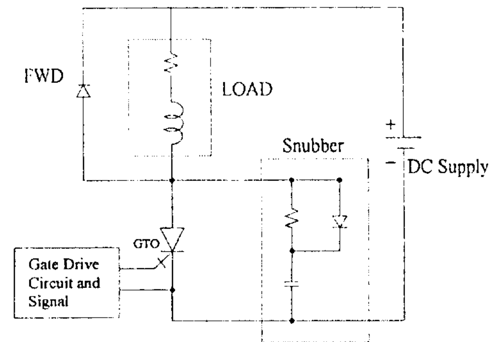


Fig. 10 Experimental setup for testing of dirve circuit

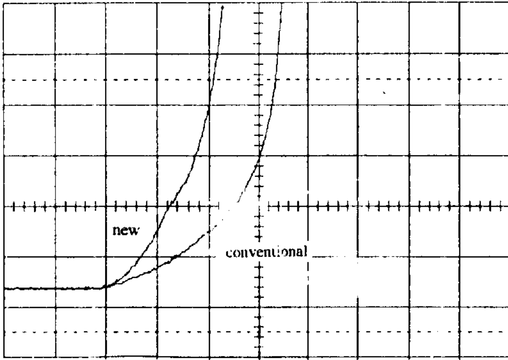
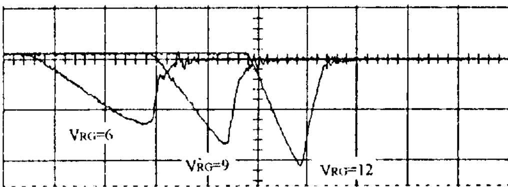
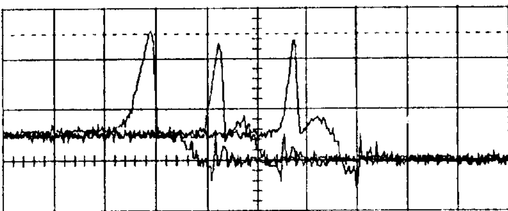


Fig. 11 Magnified rising V_{AG} by the conventional and the new turn-off circuits(0.5V/div, 1 μsec/div)



(a)



(b)

Fig. 12 i_{GQ}(10 A/div, 5μsec/div)
(b) P_{off}(2 KW/div, 2μsec/div)
by the conventional turn-off gate drive circuit

negative di_{GQ}/dt is increased and there is a little increase of P_{off} as V_{RG} increases from 6V to rating 12V.

When we increased V_{RG2} from 15V to 30V with V_{RG1}=12V, V_{AK}, I_A, i_{GQ} and P_{off} by the new turn-off gate drive technique are shown in Fig. 13, 14, 15, 16. Fig. 17 shows that i_{GQ} is made in two different circuits. One is i_{GQ1} by the conventional turn-off circuit and the other is i_{GQ2} by the added turn-off circuit. That is $i_{GQ}=i_{GQ1}+i_{GQ2}$, which means that i_{GQ} is increased as much as i_{GQ2} and turn-off time is decreased.

Fig. 13, 14 show that the derivatives of I_A and V_{AK} were changed during t_{gf}. This phnomena happen because Q_1 and Q_2 transistors have different turn-off transient time in the new turn-off gate drive circuit. If V_{RG2} is too large rather than V_{RG1}, there will remain a lot of excess carriers at Q_2 after the turn-off of Q_1. In that case, there would be large tail current shown in Fig. 18. It is diffi-

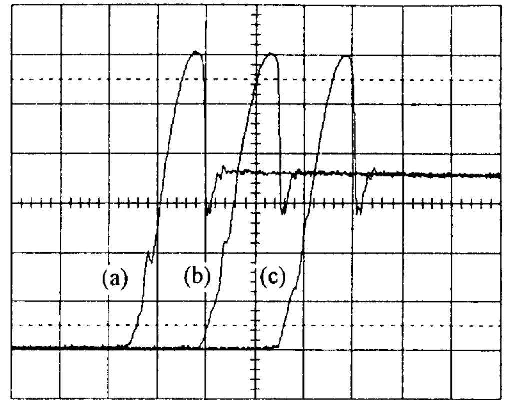


Fig. 13 V_{AK} when $_{RG1}$=12V and V_{RG2}=(a) 15V, (b) 22V, (c) 20V(100V/div, 2μsec/div)

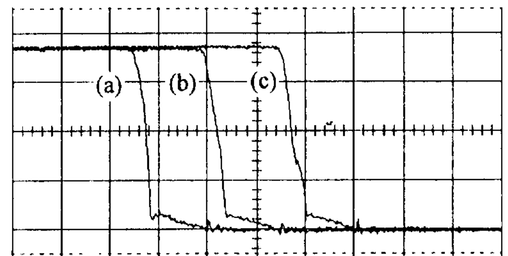


Fig. 14 I_A when V_{RG1}=12V and V_{RG2}=(a) 15V, (b) 22V, (c) 30v(20A/div, 2μsec/div)

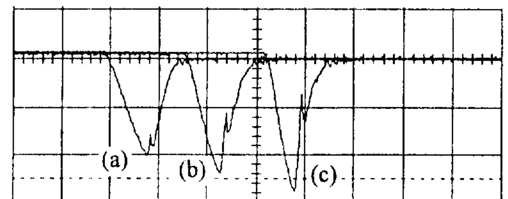


Fig. 15 I_{GQ} when $_{RG1}$=12V and V_{RG2}=(a) 15V, (b) 22V, (c) 30V(10A/div, eμsec/div)

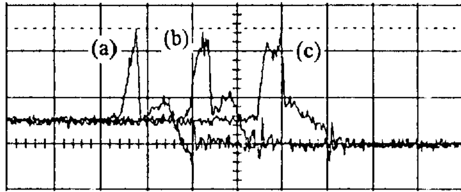


Fig. 16 P_{off} when $V_{RG1}=12V$ and $V_{RG2}=$(a) 15V, (b) 22V, (c) 30V(2KW/div, 2μsec/div)

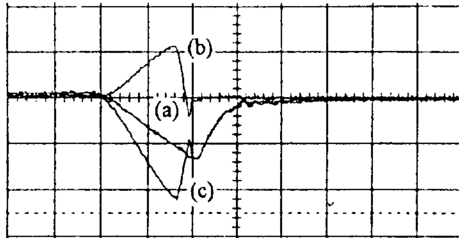


Fig. 17 (a)$-i_{GQ1}$, (b) i_{GQ2} and (c)$-i_{GQ}$;($i_{GQ}=i_{GQ1}+i_{GQ2}$) (10A/div, 2μsec/div)

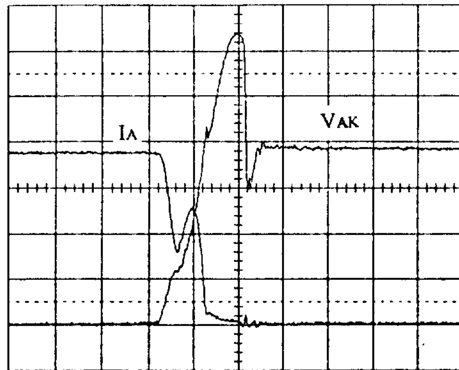


Fig. 18 V_{AK}(100V/div, 2μsec/div, I_A(20 A/div, 2 μsec/div)when $V_{RG1}=6$v and $V_{RG2}=30$V

cult to decide a optimal V_{RG2} with calculation because Q_1 and Q_2 have different doping densities and intrinsic structure. From the experiment, we knew that V_{RG2} two or three times of V_{RG1} can shorten the turn-off time without a lot of increase of P_{off}. Fig. 15 shows that turn-off time by the new turn-off gate drive technique is decreased because negative di_{GQ}/dt of the new turn-off gate drive technique is increased more than that of the conventional turn-off gate drive technique. Fig. 16 shows that there is a little increase of P_{off} by the new turn-off gate drive technique, which happens

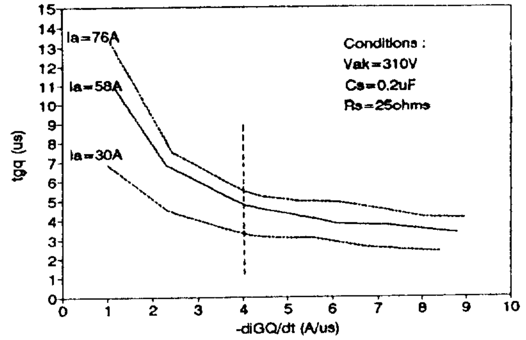


Fig. 19 Turn-off time in dependency of the negative di_{GQ}/dt at varying anode current to be turned off

because of the change of dV_{AK}/dt and dI_A/dt during t_{gf} and a little increase of I_{TAIL}. Fig. 19 shows the relationship of the turn-off time and negative di_{GQ}/dt.

Vertically dashed line shown in Fig. 19 indicate maximum negative di_{GQ}/dt with rating $V_{RG1}=12V$ and $V_{RG2}=0V$ at each load condition. It shows that the turn-off time of the new turn-off gate drive technique can be less than minimum turn-off time by the conventional turn-off gate drive technique.

6. Conclusion

The conventional turn-off mechanism and gate drive technique for GTO thyristor have been reviewed and the new turn-off technique for faster turn-off switching with a little increase of P_{off} has been presented. The new turn-off gate drive circuit could make the negative di_{GQ}/dt larger than the maximum of the negative di_{GQ}/dt of the conventional turn-off gate drive circuit. The new technique could be free from the constraints of V_{RGM} and stray inductances of turn-off gate drive circuit. The simulation and experimental results were compared and showed the validity of the new turn-off gate drive technique. Afterhere, a research on a compact gate driver and low gate drive power must be done in the new turn-off gate drive circuit.

Appendix

Electrical characteristics of Hitachi GFF90B12 GTO thyristor:

- Repetitive Peak Off-State Voltage=1,200V;
- RMS On-State Current=30A;
- Repetitive Controllable On-State Current=90A;
- Non-Repetitive Controllable On-State Current=180A;
- Surge(Non-Repetitive) On-State Current=400A;
- dv/dt=1,000 V/μsec;
- Critical Rate of Rise of On-State Current=200 A/μsec;
- Repetitive Peak Reverse Gate Voltage=13V;
- Storage Time(T_{gs})=4.0μsec(Typ);
- Fail Time(T_{gf})=0.5μsec(Typ);
- Turn-on Time=3.0μsec(Typ);

REFERENCES

[1] Ned Mohan et al., "Power Electronics: Converters, Application and Design," John Wiley & Sons, pp. 455-638, 1989.

[2] Dr. Roger Bassett et al., "A GTO Tutorial," PCIM Magazine, July-September, 1989.

[3] Reinhard Sievers, "The Influence of Gate Drive Circuits on The Switching Behaviour of Large Gate Turn-Off Thyristors," EPE, Aachen, pp.701-706, 1989.

[4] H.A.Kojori et al., "An optimum gate drive for high power GTO Thyrister," APEC, pp. 439-444, 1992.

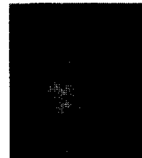
[5] Theodor Salzmann et al., "GTO Driving and Protection Technique with Status Monitoring," IEEE Trans. Ind. Appl., vol.24, no.1, Jan/Feb, pp. 115-120, 1988.

[6] Sujit K. Biswas et al., "An autoprotecting gate drive circuit for GTO thyristors", IEEE Trans. Ind. Appl., vol.24, no.1, Jan/Feb, pp. 121-126, 1988.

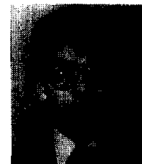
[7] Tsay et al., "A High Power Circuit Model for The Gate Turn-Off Thyristor," PESC,pp. 390-397, 1990.

저 자 소 개

김영석(金永錫)
1968년 1월 30일생. 1992년 한양대공대 전기공학과 졸업. 현재 한양대 대학원 전기공학과 석사과정.



서범석(徐範錫)
1966년 10월 5일생. 1989년 한양대 공대 전기공학과 졸업. 1991년 한양대 대학원 전기공학과 졸업(석사). 현재 한양대 대학원 전기공학과 박사과정.



이택기(李宅基)
1963년 9월 4일생. 1987년 한양대공대 전기공학과 졸업. 1989년 한양대 대학원 전기공학과 졸업(석사). 1993년 한양대 대학원 전기공학과 졸업(공박).

현동석(玄東石)
1950년 4월 8일생. 1973년 한양대공대 전기공학과 졸업. 1978년 한양대 대학원 전기공학과 졸업(석사). 1986년 서울대 대학원 전기공학과 졸업(공박). 1984~85년 미국 토레도 대학 교환교수. 1988~89년 뮌헨공과 대학 교환교수. 현재 한양대 공대 전기공학과 교수. 당학회 평의원.