Journal of the Korean Vacuum Society
Vol. 2, No. 2, June 1993, pp. 161-165

〈연구논문〉

Epitaxial Growth of Ge on Si(100) and Si(111) Surfaces†

Yun Ho Khang and Young Kuk*

Department of Physics, Seoul National University
**Also with ISRC, Seoul National University*
(Received May 11, 1993)

Si(100)와 Si(111) 표면의 Ge 에피 성장 연구

강윤호 · 국 양*

서울대학교 자연과학대학 물리학과
및 서울대학교 반도체공동연구소
(1993 5월 11일 접수)

Abstract – The geometrical and electronic structure of epitaxially grown Ge on Si(100) and Si(111) surfaces has been studied by scanning tunneling microscopy. Since Ge atoms could be distinguished from Si atoms by scanning tunneling spectroscopy and voltage dependent STM images, the growth mode of the added layer could be studied. On the (100) surface with a (2×1) reconstruction, Ge overlayer grow preferentially on the **B** type step edges at 720 K. On the (111) surface, Ge overlayer also grow on the step edges with (7×7) and (5×5) structure depending on their coverage and annealing temperature.

요 약 – Si(100)와 Si(111) 표면에 에피 성장시킨 Ge의 기하학적, 전기적 구조가 scanning tunneling microscope로 연구되었다. Ge 원자는 scanning tunneling spectroscopy와 bias 전압을 달리한 STM 상에서 Si 원자와 구별되었다. 이것을 이용하여 Ge의 성장 형태를 연구하였다. (2×1) 재배열 구조를 가진 (100) 표면에서 Ge 성장층은 720 K에서 **B**형의 step edge로부터 주로 성장하였다. (111) 표면에서도 주로 step edge에서 성장하였으며, Ge의 양과 annealing 온도에 따라 (5×5)와 (7×7) 구조가 보였다.

1. Introduction

Silicon is the most widely used material for semiconductor devices. It has nearly all properties necessary for the semiconductor fabrication, such as low defect, reproducibility, low cost for fabrication, simple impurity control, and easy patterning. As it is believed that conventional Si devices reach the ultimate limit of the size and speed, new semiconducting materials and structures are demanded. GaAs has been regarded as one of the solutions because of its high mobility and light emission. *Band-gap Engineering* is regarded as another solution. Among group IV semiconductors, Ge-Si multilayers or their alloy have drawn much attention due to the prediction of band-gap engineering and possible high speed devices.

The studies of epitaxial growth of Ge on Si have carried out on various Si substrates, (111)[1, 2], (110)[3], (113)[4], and (100)[5-7]. The previous reports have found that Ge grows with Stranski-Krastanow mode on various surfaces[1]. The overlayer Ge often maintains the reconstruction of (2×1) on the Si(100) substrate and (7×7) on the Si

†이 연구는 한국과학재단 '91 목적기초연구비의 지원을 받아 수행되었음

(111) substrate. The growth kinetics and level of disorder are strong functions of the substrate temperature and deposition rate. Pure Ge films reveals the critical thickness of 5 monolayer and dislocations with higher coverage. The lattice constants of Si and Ge are 5.43 Å and 5.65 Å, respectively, therefore the lattice mismatch is about 4%. The surface of Si(111) is reconstructed to (7×7) in order to lower surface energy for dimer, adatom and stacking fault (DAS model)[8]. In order to accommodate the DAS model, (5×5), (2×2) and (9×9) can be formed on the (111) surface. These non-(7×7) DAS surfaces only appear metastably on rapidly quenched surface, revealing the slight different of the surface energy. Similarly, c(2×8) structure is formed for Ge(111) surface, but this structure does not have stacking fault.

On (100) surfaces of Si and Ge, the surface energy is reduced by forming dimers from two dangling bonds, resulting a (2×1) structure. On (2×1) structures of Ge(100) and Si(100), there are two types of steps, type **A** and type **B**[9]. Type **A** step is parallel to the upper-terrace dimer rows. Type **B** step is perpendicular to the upper-terrace dimer rows. Science there is a slight difference of the step energies between these two steps, **A** step is straight, while **B** step is rough. In well ordered (100) surface of Ge and Si with small miscut, the two types of step are appeared alternatively.

The homoepitaxy on Si(100) surface and the heteroepitaxy Ge on Si(100) have been widely studied, because of the possible use in devices. It is known Si/Si(100) and Ge/Si(100) grow preferentially from type **B** step edge, and covered the type **A** terrace, by earlier STM studies[6].

In this study, we confirm the growth mechanism under 1 ml by STM and the chemical identification of Ge by STM and STS, for the first time. The model for the relationship between the Ge growth shape and the annealing temperature is proposed.

2. Experimental

In this experiment, A UHV STM was used, of which the detailed design can be found elsewhere [10]. Si sample was cut from Arsenic doped (1~4 Ω-cm) wafer with miscut <0.4°. The sample was prepared *ex situ Shiraki* cleaning process and *in situ* annealing by resistive heating. The sample annealing was done by heating at 500~700℃ for 12 hours or more, followed by flash at 1,250℃ for 20 sec and slow cooling down. The Ge K cell was made of a W-filament and a Ge holder. Ge source was outgassed at 700~800℃ for several hours before deposition. The source was deposited by rate of 0.5 ML/min. When the source was deposited, the chamber pressure was less than 5×10^{-10} torr. The source deposition was done after sample flash and cooling down. After deposition, the sample was annealed at 500~700℃ for 10~30 min in order to have on ordered structure.

3. Results and Discussion

3.1. Ge/Si(100)

The surface topography was taken sequentially with increasing Ge coverage. When the Si(100) surface was imaged before Ge deposition, the STM images reveals a sharp (2×1) dimer row with average step size of ~100 Å terminated by type **A** and type **B** steps, alternatively.

At low Ge coverage of about 0.1 ML, as shown in Fig. 1, nearly all Ge atoms are sticked to the step edge, especially to type **B** step edge. This is rather different from earlier results by STM[5, 6]; the Ge islands are formed on Si terrace. In previous work, the substrate was annealed at 750 K or below, while in this experiment it was annealed at about 750~970 K. At the higher annealing temperature, Ge adatoms diffuse more easily and it can be relieved from the nucleation sites on the terraces (mainly defects). Therefore, they aggregate on the step edges. Near the step edges, Ge can fall down to the lower terrace, but they cannot climb up to the upper terraces. Once Ge atoms reaches type **A** steps, they have to break a dimer to form a new dimer. But, on the **B** steps, any two Ge atoms can be added to the end of Si dimer row. For this reason, the Ge adatoms energetically prefers to grow as dimer rows on the **B** steps. For earlier experiment, at lower annealing temperature, below 750 K, the Ge island is formed at terrace,

Fig. 1. 300×300 Å^2 image of a Ge on Si(100) surface. The coverage of Ge is about 0.1 ml.

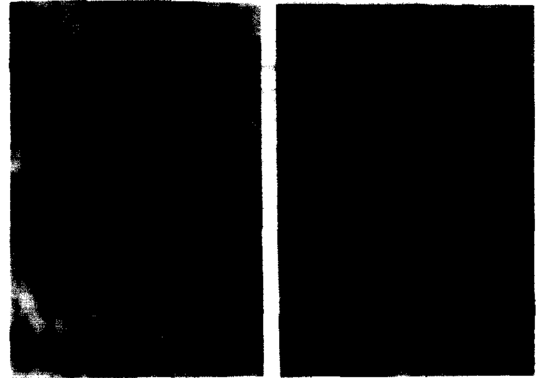

Fig. 2. (a) 240×240 Å^2 image. −0.9 V sample bias voltage image of Ge on Si(100) surface, with Ge coverage of 0.3 ml. (b) +0.9 V sample bias voltage image taken with (a) simultaneously.

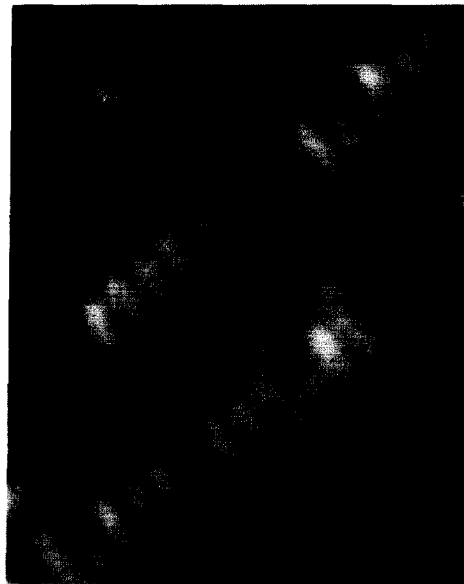

Fig. 3. 150×150 Å^2 image of Ge on Si(100) surface, with Ge coverage of about 0.5 ml.

and the longer direction of island is perpendicular to the dimer row direction. It is due to low kinetic energy, compared with the sticking energy. In this case, the sticking to step edge is not preferable.

As shown at Fig. 1, Ge adatoms have very different brightness as Si substrate, though they have the same height as Si. This suggests the electronic structure of Ge overlayer is different from that of Si substrate. The difference can be due to the different band structure of Ge layer and the effect of the Ge-Si interface.

Fig. 2 shows an STM image at 0.3~0.4 ML coverage. At this coverage, the Ge growth at Si substrate step edge is evident. The **A** type terrace is nearly covered by the Ge overlayer grown at **B** type step edge of Si substrate. This is consistent with the result at low coverage. The Ge overlayer also appears brighter than the Si substrate. This brighter images at various voltages suggest more states at Ge adatoms at these voltages. The dual bias voltage image, obtained at ±0.9 V bias voltages simultaneously, shows different shapes at the bias voltages. At −0.9 V sample bias voltage, Ge adatoms are much brighter than Si atoms. But, at +0.9 V image, Ge adatoms and Si substrate are not distinguishable. Voltage dependent ATM image can be understood easily on the scanning tunneling spectroscopy.

At the Ge coverage of 0.5 ML, as shown in Fig. 3, the type **A** Si steps are disappeared completely, remaining only type **B** step edges. The step shown in Fig. 3 has the double atomic height, the half of each terrace is covered with Ge. Since the half of terrace consist of Ge, if the surface can be cap-

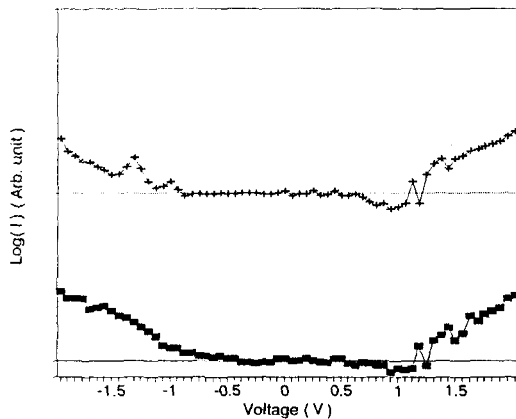

Fig. 4. Log I (V) taken at (a) the spot (+) near to the upper-stairs step edge and (b) and spot (■) near to the down-stairs step edge on the same terrace of Ge/Si(100) surface, with the Ge coverage of about 0.5 *ml*.

ped with other material, this surface will reveal a quantum wire structure at low temperature because of the lower bandgap of Ge.

In order to confirm the chemical identity of the part of these terraces, spatially resolved scanning tunneling spectroscopy was performed. The STS shows the different band-gap between at epitaxially grown region of terrace (the terrace edge near to the down-stairs) and at substrate (the terrace edge near to the upper-stairs). Fig. 4 shows I-V at two typical sites. At the terrace edge near to the down-stairs, the I(V) has smaller band gap, suggesting the area is covered with Ge. To the contrary, at the terrace edge near to the upper-stairs, the band-gap reveals that of Si.

3.2. Ge/Si(111)

The epitaxially grown Ge on Si(111) shows various structures with varying Ge coverage and annealing temperature. Ge adlayers grow preferentially at step edges, similar at Ge on Si(100) surface.

The structure on Si(111) can be well explained 'DAS model'. There are three types of DAS model, (5×5), (7×7) and (9×9). For each structure, the ratio of adatom and dimer per surface atoms are different. For (7×7) structure, 38.8% of surface atoms have dangling bonds. There are 36.6% and 40.7% dangling bonds of surface atoms for (5×5) and (9×9) structure, respectively. For number of dimers per unit cell, there are 6, 9 and 12 for (5×5), (7×7) and (9×9) structure, respectively. As the number of dangling bands decrease, the surface energy increase. Therefore, (5×5) is preferred if the number of dangling bonds is only concerned. However, the (7×7) structure is more stable in well ordered surface by high temperature annealing followed by slow quenching. Therefore, we can imagine the dimerization also lower the surface energy. In order to analyze the surface structure on Si(111), the relationship of dimer and dangling bond have to be analyzed quantitatively. The *ab initio* total energy calculation shows (7×7) structure has the lowest surface energy among three DAS model structure, but the energy difference is only about 10 mV per surface atom[11]. It means the metastable structure of (5×5) and (9×9) can be appeared for the slightly different condition, such as high quenching speed or in the presence of defect. If Si and Ge atoms form the alloy, the surface structure shows mainly (5×5) or c(2×8) structure, but no (7×7) structure[12], showing that the small difference of growth condition changes the surface structure.

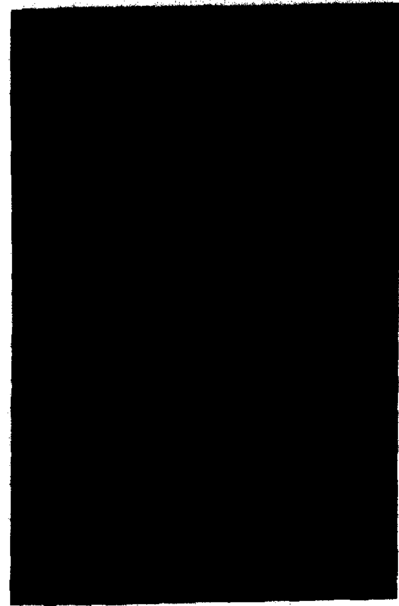

Fig. 5. 250×300 Å^2 image of Ge-(7×7) structure on Si(111), with Ge coverage of about 1 *ml*.

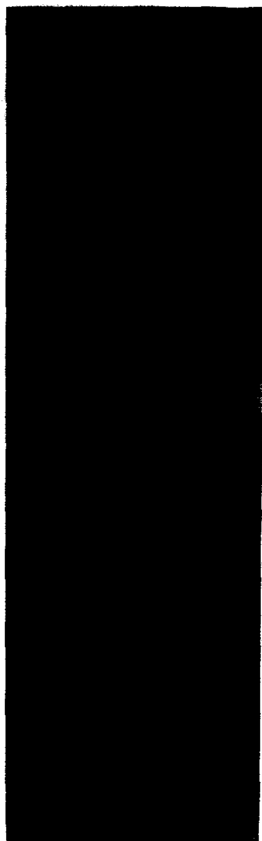

Fig. 6. 120×250 Å^2 image of Ge-(5×5) structure on Si(111) with Ge coverage of about 2 *ml*.

The epitaxial growth of Ge on Si(111) shows several different structure as the growth condition is varied. At small coverage of 1 ML or less and high temperature annealing, above 770 K, Ge-(7×7) reconstruction structure appears. This Ge-(7×7) on Si(111) image is shown in Fig. 5. At ligher coverage of 2~3 ML and the same annealing temperature, Ge-(5×5) reconstruction structure appeared, as shown in Fig. 6. And, at the coverage above 5 *ml*, the 3 dimensional island formation appeared. If the sample deposited is not annealed, the amorphous phase occurred. It is believed that the Ge overlayer reveal the character of Si when the coverage is low. But with increasing coverage, the Ge return to its own bulk character through (5×5) phase to eventual c(2×8) phase. It will be worthwhile to complete the phase diagram with the annealing temperature and coverage.

4. Summary

The initial states of Ge on Si(100) and Si(111) surface were studied using a UHV STM. The Ge overlayer on Si(100) substrate grew preferentially at type **B** step edge. With increasing annealing temperature, the Ge migrates to step edges and lowers the step energy by adsorbing at **B** type step edges. These kinetics are well studied with the different electronic structure of Ge from that of Si.

On the Ge/Si(111) system, (5×5) and (7×7) phases were observed with varying coverage.

References

1. U. Köhler, O. Jusko, G. Pietsch, B. Müller and M. Henzler, *Surf. Sci.* **248**, 321 (1991).
2. R. S. Becker, J. A. Golovchenko and B. S. Swartzentruber, *Phys. Rev.* **B32**, 8455 (1985).
3. W. T. Pike, R. W. Fathauer and M. S. Anderson, *J. Vac. Sci. Technol.* **B10**, 1990 (1992).
4. J. Knall and J. B. Pethica, *Surf. Sci.* **265**, 156 (1992).
5. Y.-W. Mo and M. G. Lagally, *Surf. Sci.* **248**, 313 (1991).
6. A. J. Hoeven, D. Dijkkamp, E. J. van Leonen, J. M. Lenssinck and J. Dieleman, *J. Vac. Sci. Technol.* **A8**, 207 (1990).
7. F. Iwawaki, M. Tomitori and O. Nishikawa, *Surf. Sci.* **266**, 285 (1990).
8. K. Takayanagi, Y. Tanishiro, M. Takahashi and S. Takahashi, *J. Vac. Sci. Technol.* **A3**, 1502 (1985).
9. D. J. Chadi, *Phys. Rev. Lett.* **59**, 1691 (1989).
10. Y. Kuk and P. J. Silverman, *Rev. Sci. Instrum.* **60**, 165 (1989).
11. I. Stich, M. C. Payne, R. D. King-Smith and J.-S. Lin, *Phys. Rev. Lett.* **68**, 1351 (1992).
12. M. A. Lamin, O. P. Pchelyakov, L. V. Sokolov, S. I. Stenin and A. I. Toropov, *Surf. Sci.* **207**, 418 (1989).